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Programmable Clock Generator
AK8142

Features

- **Supply Voltage:**
  3.0 – 3.6V(Main)
  1.8 – 3.3V(Interface)
- **Low Current Consumption:**
  5.0mA (Typ.)
- **Crystal Unit Oscillation:**
  16.0MHz – 32.0MHz
- **Input Frequency:**
  2.0MHz – 67.0MHz
- **Output Frequency:**
  4.0MHz – 200MHz
- **Low Jitter Performance:**
  15 ps (Typ.) Period 1s
- **Operating Temperature Range:**
  -30 to +85℃
- **I2C Interface:**
- **Package:**
  16-pin TSSOP

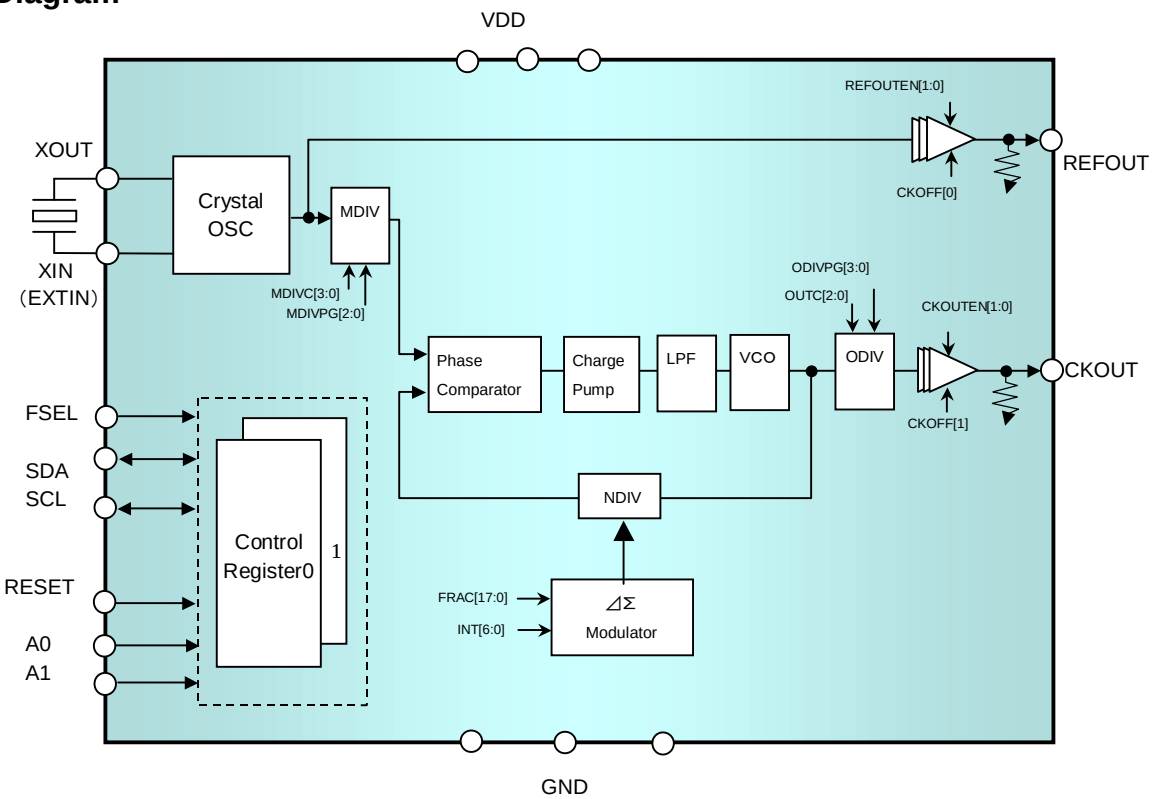
Description

The AK8142 is a programmable clock generator IC with an integrated Fractional N PLL. Highly accurate clocks can be output from an external master clock or a crystal unit.

Applications

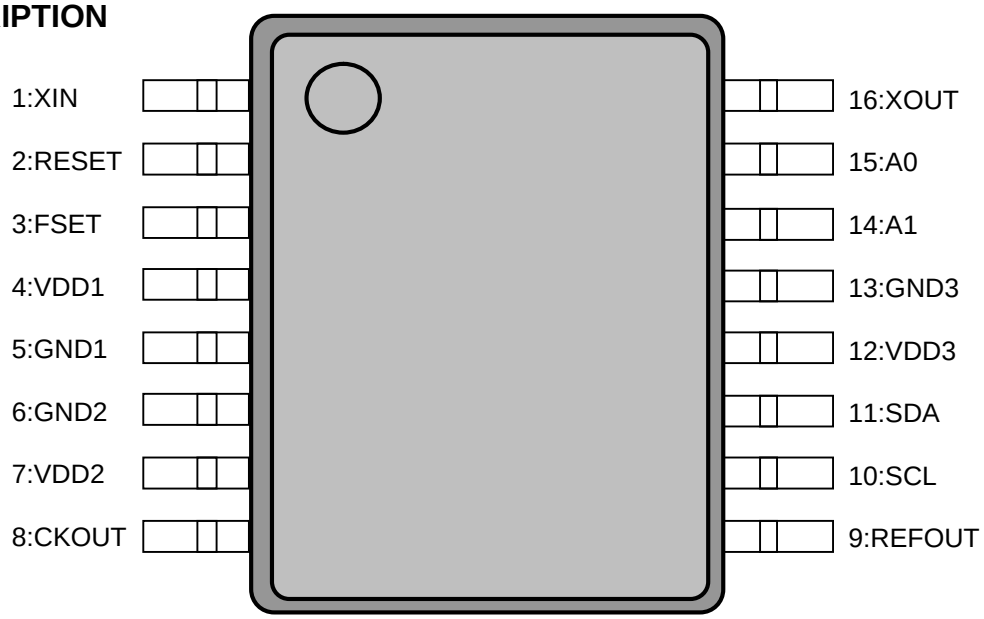
- General purpose clock generator

Block Diagram



AK8142 Register Programmable Clock Generator

PIN DESCRIPTION



Package: 16-Pin TSSOP (Top View)

Pin No.	Pin Name	Pin Type	Description
1	XIN	IN	Crystal connection. Please input external clock to XIN when the external clock is used.
2	RESET	IN	Reset signal input pin. High pulse reset the register and digital part of PLL. Hi: Reset Lo: Normal operation
3	FSEL	IN	Frequency setting register bank selection pin. Hi: Register bank1 Lo: Register bank0 Valid when CTLFSEL="1" of Register F7.
4	VDD1	--	3.3V power supply for PLL core.
5	GND1	--	Ground 1.
6	GND2	--	Ground 2.
7	VDD2	--	Power supply for clock output buffer. 1.8V or 3.3V can be used.
8	CKOUT	OUT	Clock output.
9	REFOUT	OUT	PLL reference clock output.
10	SCL	IN	Serial interface clock input.
11	SDA	IN / OUT	Serial data input and output pin. Open drain.
12	VDD3	--	Power supply for serial interface. 1.8V or 3.3V can be used.
13	GND3	--	Ground 3.
14	A1	IN	Device address setting pin.
15	A0	IN	Device address setting pin.
16	XOUT	IN	Crystal connection. Please keep this pin open if the external clock is input to XIN pin.

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8142	8142	Tape and Reel	16-pin TSSOP	-30 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 to 4.6	V
Input Voltage	Vin	VSS-0.3 to VDD+0.3	V
Input Current (any pins except supplies)	I_{IN}	±10	mA
Storage Temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKEMD recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature	Ta		-30		85	°C
Supply Voltage	VDD1		3.0	3.3	3.6	V
	VDD2 VDD3		1.7	1.8	VDD1	V
Input Clock Frequency1	Fin1	Quartz Oscillator input	16.0	24.0	32.0	MHz
Input Clock Frequency2	Fin2	External input, >0.8Vpp	2.0		67.0	MHz
Input Clock Duty Cycle		External input	30	50	70	%
Output Load Capacitance	Cp1	Pin: CKOUT 4MHz – 100MHz 100MHz – 150MHz 150MHz – 200MHz			 15 10 8	pF
	Cp2	Pin: REFOUT 2MHz – 67.0MHz			25	pF

DC Characteristics

All specifications at VDD1: 3.3V, VDD2/VDD3: 1.8V, Ta: -30 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage1	$V_{IH}1$	Pin: A0, A1, FSEL, RESET	0.7VDD1			V
Low level input voltage1	$V_{IL}1$				0.3VDD1	V
High level input voltage2 (1)	$V_{IH}2$	Pin: SCL, SDA	0.7VDD3			V
Low level input voltage2 (1)	$V_{IL}2$				0.3VDD3	V
Input Current	I_L	Pin: A0, A1, FSEL, RESET	-10		+10	μA
High level output voltage1	$V_{OH}1$	REFOUT, CLKOUT IOH= -4mA	0.8VDD2			V
Low level output voltage1	$V_{OL}1$	REFOUT, CLKOUT IOL = +4mA			0.2VDD2	V
Low level output voltage2	$V_{OL}2$	Pin: SDA IOL = +3mA, Open Drain			0.4	V
Current Consumption (2), (3)	$I_{DD}1$	No load, VDD1		3.5		mA
	$I_{DD}2$	No load, VDD2		0.95		mA
	$I_{DD}3$	No load, VDD3		0.05		mA
Power down current	I_{pd}	OE="L" FSEL="L" or open		0	10	μA

(1) Do not exceed the voltage VDD3.

(2) External clock mode.(SCL=H, SDA=H), No load.

(3) XIN = 16MHz, CKOUT = 24.5759989MHz.

Register: FF=03hex, FE=74hex, FD=BChex, FC=25hex, FB=32hex, FA=61hex

AC Characteristics

All specifications at VDD1: 3.3V, VDD2/VDD3: 1.8V, Ta: -30 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Phase Comparison Period (1)			2		4	MHz
VCO Frequency (2)		CKOUT	100			MHz
Output Clock Frequency (3)		CKOUT, Divided	4.0		100	MHz
		CKOUT, not Divided	100		200	MHz
Output Clock Duty Cycle (4)(7)		REFOUT (5)	40	50	60	%
		CKOUT, Divided	45	50	55	
		CKOUT, not Divided	30	50	70	
Output Clock Rise Time (4)(7)	t_{rise}	REFOUT, 0.2VDD to 0.8VDD 2MHz – 66.0MHz			3.0	ns
		CKOUT, 0.2VDD to 0.8VDD 4MHz – 100MHz			3.0	ns
		CKOUT, 0.2VDD to 0.8VDD 100MHz – 150MHz			2.5	ns
		CKOUT, 0.2VDD to 0.8VDD 150MHz – 200MHz			2.0	Ns
Output Clock Fall Time (4)(7)	t_{fall}	REFOUT, 0.2VDD to 0.8VDD 2MHz – 66.0MHz			3.0	Ns
		CKOUT, 0.2VDD to 0.8VDD 4MHz – 100MHz			3.0	Ns
		CKOUT, 0.2VDD to 0.8VDD 100MHz – 150MHz			2.5	ns
		CKOUT, 0.2VDD to 0.8VDD 150MHz – 200MHz			2.0	ns
Output Clock Jitter (4)(7)	Jit	CKOUT, Period, 1σ		15		ps
Output Lock Time (6)	t_{lock}	CKOUT, Power-up		1		ms

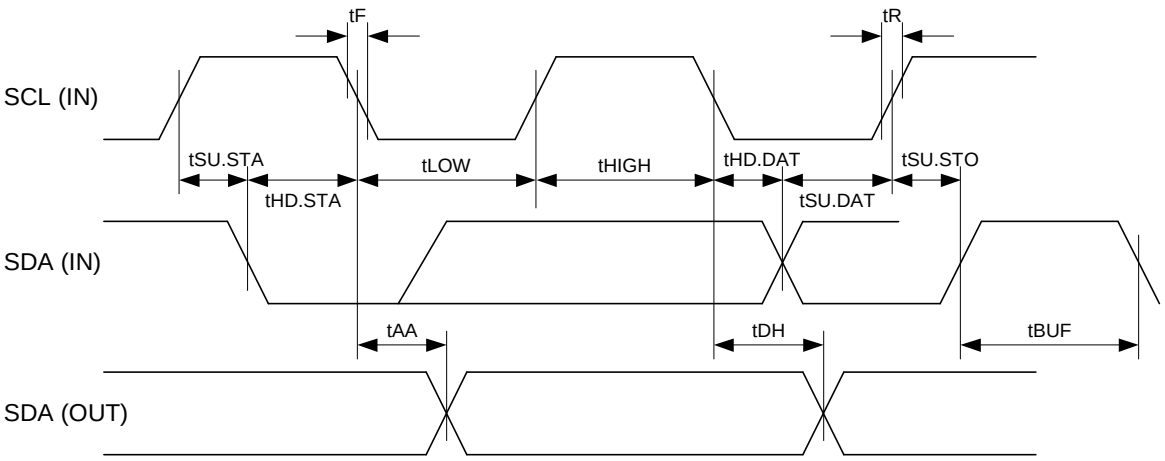
(1) Phase Comparison Frequency = Input frequency / MDIV value. Refer to register address FA.
(2) VCO Frequency = Phase Comparison Frequency x NDIV value. Refer to register address FC.
(3) Refer to register address FB.
(4) With the load capacitance specified by the recommended operation conditions.
(5) Quartz oscillator input or external clock input with 50% duty.
(6) The time that output reaches the target frequency within accuracy of ±0.1% from the point that the FSEL is switched.
(7) Design value

Serial interface（I2C：slave mode）AC Characteristics

All specifications at VDD1: 3.3V, VDD2/VDD3: 1.8V, Ta: -30 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	MAX	Unit
SCL clock frequency	fSCL			400	kHz
SCL Clock Low Period	tLOW		4.7		us
SCL Clock High Period	tHIGH		4.0		us
Pulse width of spikes which must be suppressed	tI			100	ns
SLC Low to SDA Data Out	tAA		0.1	3.5	us
Bus free time between a STOP and START condition	tBUF		4.7		us
Start Condition Hold Time	tHD.STA		4.0		us
Start Condition Setup Time (for a Repeated Start condition)	tSU.STA		4.7		ms
Data in Hold Time	tHD.DAT		0		us
Data in Setup Time	tSU.DAT		200		ns
SDA and SCL Rise Time	tR	(*)		1.0	us
SDA and SCL Fall Time	tF	(*]		0.3	us
Stop Condition Setup Time	tSU.STO		4.0		us
Data Out Hold Time	tDH		100		ns

(*) Design value.

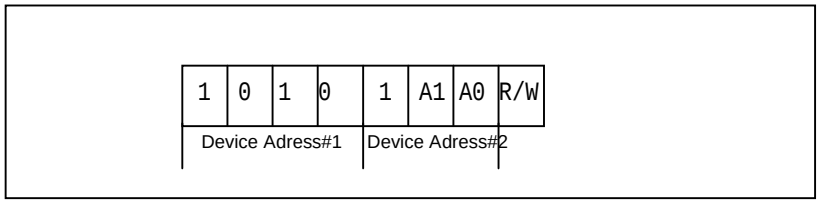


Function Description

I2C interface

Read/Write performance of I2C interface is expressed below. The device address #1 of AK8142 is fixed as ”1010”. The device address #2 is set by A0, A1 pins.

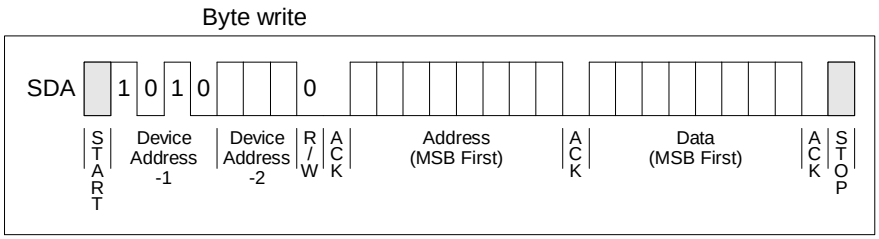
Device address of AK8142



Byte wtire operation

Byte write operation is described below. Data must be sent after sending 8 bits address and receiving ACK.

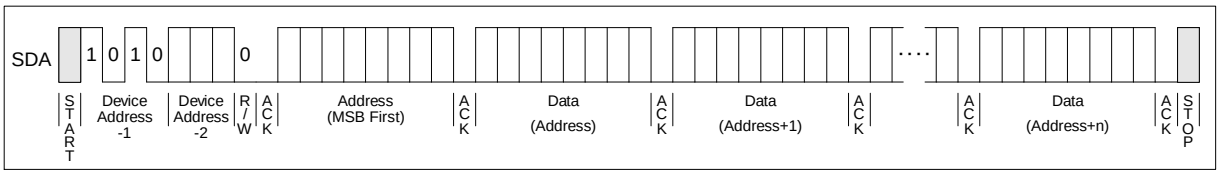
Byte write



Page write operation

Page write operation is described below. Only lower 4 bits of address are valid. Upper 4 bits are fixed as “1111”. Therefore the address which is written after “1111 1111” becomes “1111 0000”.

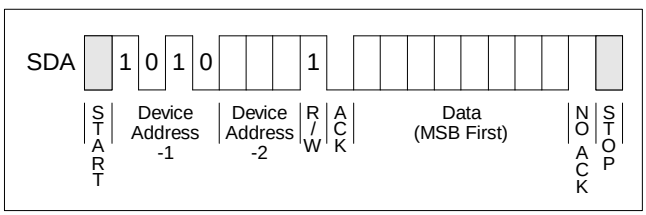
Page write



Current address read

Current address read operation is described below. The data that is read by this operation is obtained as “last accessed address + 1”. Therefore, It is consequent to return “0000 0000” after accessing the address “0000 1111”.

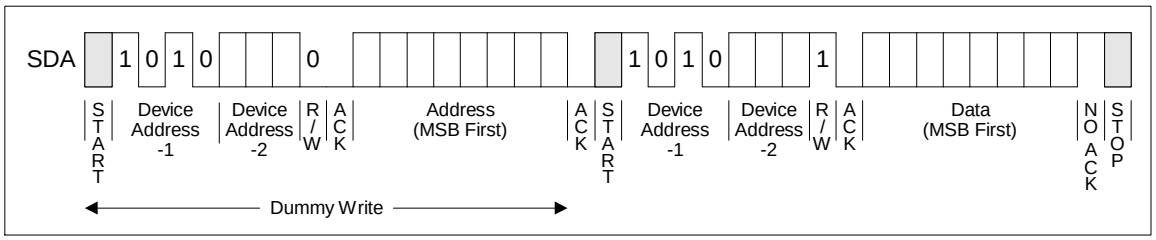
Current address read



Random read

Random read operation is described below. It is necessary to operate “dummy write” before sending read command. Dummy write is to send the address to read.

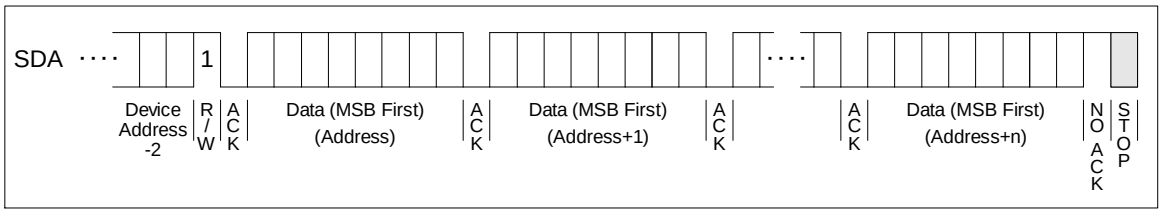
Random read



Sequential read

Sequential read operation is described below. It is possible to read next address sequentially by sending ACK instead of stop condition.

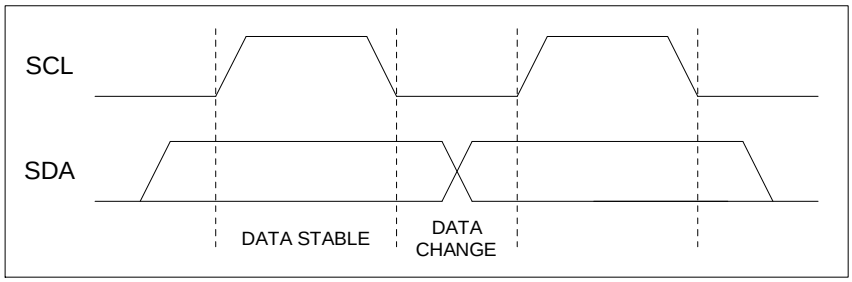
Sequential read



Change data

Change data operation is described below. It is available when SCL is Low.

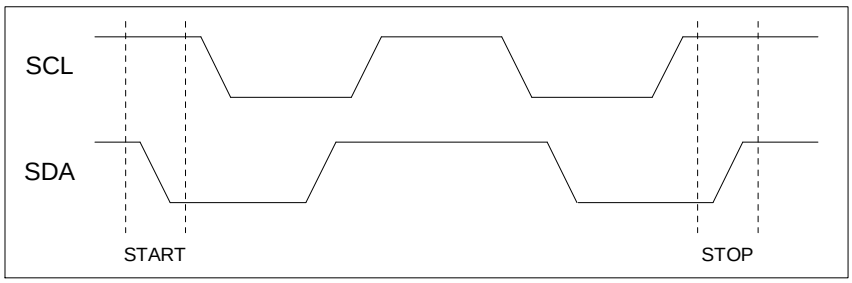
Change data



Start / Stop timing

Start / Stop timing is described below. The sequence is started when SDA goes from high to low during SCL is high. The sequence is stopped when SDA goes from low to high during SCL is high.

Start / Stop timing



Register map

FA – FF has 2 dimensions which are selectable by BANK bit. Zero is returned when "– " bits are read.
Bottom part: Reset value
*note The power-on-reset does not reset "SFTRST" of register F7.

Address	D7	D6	D5	D4	D3	D2	D1	D0	Note
FF	–	–	–	–	–	–	FRAC[17]	FRAC[16]	Sigma-Delta fraction
							0	0	
FE	FRAC[15]	FRAC[14]	FRAC[13]	FRAC[12]	FRAC[11]	FRAC[10]	FRAC[9]	FRAC[8]	
	0	0	0	0	0	0	0	0	
FD	FRAC[7]	FRAC[6]	FRAC[5]	FRAC[4]	FRAC[3]	FRAC[2]	FRAC[1]	FRAC[0]	
	0	0	0	0	0	0	0	0	
FC	–	INT[6]	INT[5]	INT[4]	INT[3]	INT[2]	INT[1]	INT[0]	Sigma-Delta integer
		0	1	0	0	0	0	0	
FB	–	OUTC[2]	OUTC[1]	OUTC[0]	ODIVPG[3]	ODIVPG[2]	ODIVPG[1]	ODIVPG[0]	OUTDIV
		1	1	1	0	1	1	1	
FA	MDIVC[3]	MDIVC[2]	MDIVC[1]	MDIVC[0]	MDIVP[3]	MDIVP[2]	MDIVP[1]	MDIVP[0]	MDIV
	0	1	1	0	0	0	0	1	
F9	–	–	–	–	RSRV	RSRV	RSRV	RSRV	Reserve
					0	1	0	1	
F8	–	–	–	–	RSRV	RSRV	RSRV	RSRV	Reserve
					0	0	0	0	
F7	BANK	BANKWR	CTLFSEL	CKOFF[1]	CKOFF[0]	RSRV	PD	SFTRST	RESET BANK
	0	0	0	0	0	0	0	0	
F6	–	–	–	–	CKOUTEN[1]	REFOTEN[0]	REFOTEN[1]	REFOTEN[0]	OUTBUF
					0	0	0	0	
F5	–	–	–	–	–	–	DUMON	DITHER	Sigma-Delta
							0	1	
F4	–	–	–	–	–	–	–	–	Test
～	–	–	–	–	–	–	–	–	Test
F1	–	–	–	–	–	–	–	–	Test

Registers F1 to F4 are for test purpose only. Do not access these registers.

Register definitions

Refer “Frequency setting procedure” on page 15 for details.

Address FF, FE, FD

Address	D7	D6	D5	D4	D3	D2	D1	D0
FF							FRAC[17]	FRAC[16]
FE	FRAC[15]	FRAC[14]	FRAC[13]	FRAC[12]	FRAC[11]	FRAC[10]	FRAC[9]	FRAC[8]
FD	FRAC[7]	FRAC[6]	FRAC[5]	FRAC[4]	FRAC[3]	FRAC[2]	FRAC[1]	FRAC[0]

FRAC[17:0] FRACTIONAL N fractional part settings

FRAC[17:0]	A value	Decimal fraction
01 1111 1111 1111 1111	+131071	0.49999619..
01 1111 1111 1111 1110	+131070	
01 0000 0000 0000 0000	+65536	0.25
00 0000 0000 0000 0001	+1	0.00000381..
00 0000 0000 0000 0000	0	0
11 1111 1111 1111 1111	-1	-0.00000381..
11 1111 1111 1111 1110	-2	
11 0000 0000 0000 0000	-65536	-0.25
10 0000 0000 0000 0001	-131071	-0.49999619..
10 0000 0000 0000 0000	-131072	-0.5

Fractional part of N is expressed by $A/2^{18}$. Here, the numerator A is defined by FRAC bits. FRAC is treated as 2’s Complement which is able to set from -2^{17} up to $+2^{17}$. Consequently, it is possible to set from -0.5 to +0.5 for fractional part of N.

FRAC[17:0] settings are updated after writing register FF. Setting procedure should be 1.FD, 2.FE and then 3.FF.

Address FC

Address	D7	D6	D5	D4	D3	D2	D1	D0
FC	−	INT[6]	INT[5]	INT[4]	INT[3]	INT[2]	INT[1]	INT[0]

INT[5:0] FRACTIONAL N integral part settings

INT[6:0]	Integral value
000 0000 - 001 1000	Prohibited
001 1001	25
001 1010	26
110 0011	99
110 0100	100
110 0101 - 111 1111	Prohibited

*note Do not set any value except ”25” - ”100”.

Address FB

Address	D7	D6	D5	D4	D3	D2	D1	D0
FB	–	OUTC[2]	OUTC[1]	OUTC[0]	ODIVPG[3]	ODIVPG[2]	ODIVPG[1]	ODIVPG[0]

OUTC[2] Programmable divider input select

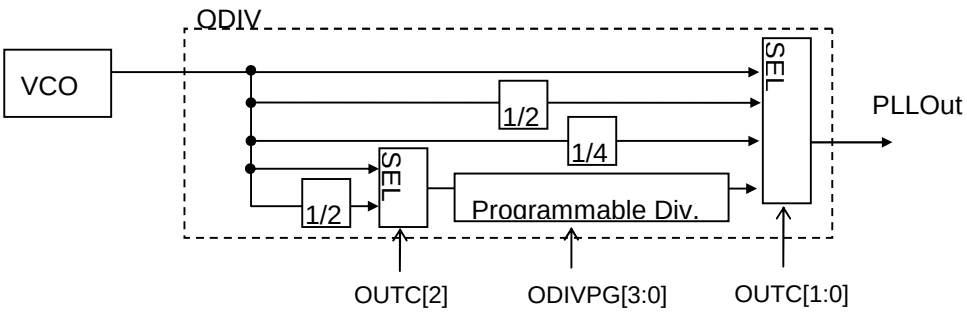
0	VCO output (not divided)
1	VCO 1/2 output

OUTC[1:0] PLL output select

OUTC[1:0]	
0 0	VCO output (not divided)
0 1	VCO 1/2 output
1 0	VCO 1/4 output
1 1	VCO programmable divider output

ODIVPG[3:0] Programmable divider control

ODIVPG[3:0]	Dividing value
0 0 0 0	(Fixed output)
0 0 0 1	4
0 0 1 0	6
0 0 1 1	8
0 1 0 0	10
0 1 0 1	12
0 1 1 0	14
0 1 1 1	16
1 0 0 0	18
1 0 0 1	20
1 0 1 0	22
1 0 1 1	24
1 1 0 0	26
1 1 0 1	28
1 1 1 0	30
1 1 1 1	(Fixed output)



Address FA

Address	D7	D6	D5	D4	D3	D2	D1	D0
FA	MDIVC[3]	MDIVC[2]	MDIVC[1]	MDIVC[0]	MDIVP[3]	MDIVP[2]	MDIVP[1]	MDIVP[0]

MDIVC[3] Programmable divider input select

0	CLKIN
1	CLKIN 1/2

MDIVC[2] 3or4 divider select

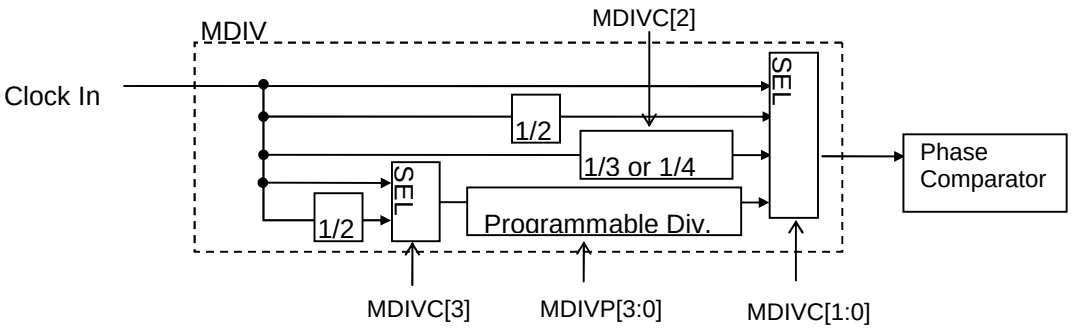
0	3 divider
1	4 divider

MDIVC[1:0] M divider dividing value settings

MDIVC[1:0]	Dividing value
0 0	1
0 1	2
1 0	3or4
1 1	programmable

MDIVP[3:0] Programmable divider control

MDIVP[3:0]	Dividing value
0 0 0 0	Prohibited
0 0 0 1	2
0 0 1 0	3
0 0 1 1	4
0 1 0 0	5
0 1 0 1	6
0 1 1 0	7
0 1 1 1	8
1 0 0 0	9
1 0 0 1	10
1 0 1 0	11
1 0 1 1	12
1 1 0 0	13
1 1 0 1	14
1 1 1 0	15
1 1 1 1	Prohibited



Address F9, F8

Address	D7	D6	D5	D4	D3	D2	D1	D0
F9	–	–	–	–	Reserved	Reserved	Reserved	Reserved
F8	–	–	–	–	Reserved	Reserved	Reserved	Reserved

These registers are reserved. Set 05hex and 00hex to F9 and F8, respectively.

Address F7

Address	D7	D6	D5	D4	D3	D2	D1	D0
F7	BANK	BANKWR	CTLFSEL	CKOFF[1]	CKOFF[0]	Reserved	PD	SFTRST

BANK — Access register select for frequency settings

0	BANK0 Valid when CTLFSEL="0"
1	BANK1 Valid when CTLFSEL="0"

BANKWR — Select the BANK to write

0	BANK0
1	BANK1

CTLFSEL — Select function for the FSEL pin

0	Invalid Set invalid when register is set.
1	Valid Frequency selection BANK is selectable with FSEL pin.

CKOFF[1] — Control REFOUT output buffer

0	Output enable
1	Output disenable (500k-ohm Pull Down)

CKOFF[0] — Control PLL output buffer

0	Output enable
1	Output disenable (500k-ohm Pull Down)

Reserved — This bit is reserved. Set to "0".

PD — Power down control

0	Power up
1	Power down (PLL analog part) Output turns to "H".

SFTRST — Software reset control

0	Reset cancel
1	Reset (PLL digital part and Register)

Set to "0" to cancel the software reset.

Address F6

Address	D7	D6	D5	D4	D3	D2	D1	D0
F6	—	—	—	—	CKOUTEN[1]	CKOUTEN[0]	REFOUTEN[1]	REFOUTEN[0]

CKOUTEN[1:0] Control CKOUT buffer drivability

CKOUTEN[1:0]	
0 0	High (x3)
0 1	Middle (x2)
1 0	Middle (x2)
1 1	Low (x1)

REFOUTEN[1:0] Control REFOUT buffer drivability

REFOUTEN[1:0]	
0 0	High (x3)
0 1	Middle (x2)
1 0	Middle (x2)
1 1	Low (x1)

Address F5

Address	D7	D6	D5	D4	D3	D2	D1	D0
F5	—	—	—	—	—	—	DUMON	DITHER

DUMON Control SDM (Sigma Delta Modulator)

DUMON	
0	Normal mode
1	Bypassing SDM Set this when using PLL with integer only.

DITHER Fractional N divider settings

DITHER	
0	Perform as fractional part is 0. Set this when using PLL with integer only.
1	Normal mode

Address F4 – F1

These registers are test propose only. Do not access these address.

Frequency setting procedure

Output frequency of CKOUT is determined by REFCLK Dividing value (MDIV), OUTPUT Dividing value (ODIV), Fractional N Dividing value (INT,FRAC). These parameters should be set as described below.

Step1. Deciding VCO base frequency.

This frequency (fvco) is decided from Output frequency and Output dividing value (address FB).

Note: Set VCO frequency between 100MHz to 200MHz.
Set ODIV bit to "1" when output frequency exceeds 100MHz.

Step2. Deciding Phase comparison frequency.

Set M divider as this frequency becomes between 2MHz to 4MHz.

Step3. Deciding Feedback dividing value.

This value is decided by VCO frequency (fvco) and Phase comparison frequency (fcmp).
7 bits integral part and 18 bits fractional part (signed 2's complement) is necessary to be set.

Integral part (INT) = round (fvco / fcmp)
Fractional part (FRAC) = round ((fvco / fcmp) – INT) x 2^{18})

Exsample1) input 27MHz, output 123.75MHz

1.	VCO frequency:	123.75MHz	ODIV = 1
2.	Phase comparison frequency:	3MHz 27MHz / 9 = 3MHz	MDIV = 9
3.	Feedback dividing value:	41.25 INT = round (123.75 / 3) = round (41.25) = 41d FRAC = round ((41.25 – 41) x 2^{18}) = 65536d Output frequency error: 0ppm	INT = 41d, FRAC = 65536d

Register settings of exsample1)

[Address]	[Value]	[Contents]
0xF7	0x08	Clear SFTRST, BANK0, FSEL=Invalid, REFOUT=OFF
0xFA	0x38	MDIV=9d
0xFB	0x00	ODIV=1d
0xFC	0x29	INT =41d
0xFD	0x00	FRAC(Lower 8bits)
0xFE	0x00	FRAC(Medium 8bits)
0xFF	0x01	FRAC(Upper 2bits) FRAC=655536d

Exsample2) input 16MHz, output 24.576MHz

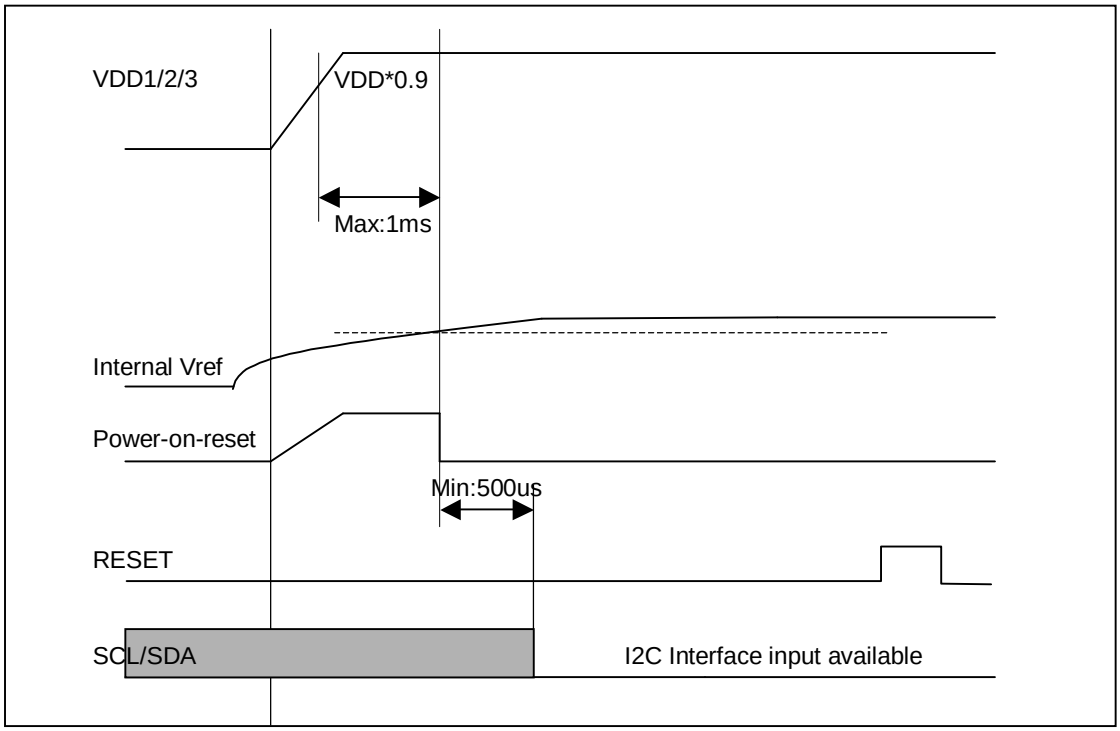
1.	VCO frequency:	147.456MHz	ODIV = 6
2.	Phase comparison frequency:	4MHz 16MHz / 4 = 4MHz	MDIV = 4
3.	Feedback dividing value:	36.864 INT = round (147.456 / 4) = round (36.864) = 37d FRAC = round (36.864 – 37) x 2^{18}) = -35652d Output frequency error: 0.043ppm (1.06Hz)	INT = 37d, FRAC = -35652d

Register settings of example2)

[Address]	[Value]	[Contents]
0xF7	0x08	Clear SFTRST, BANK0, FSEL=Invalid, REFOUT=OFF
0xFA	0x06	MDIV=4d
0xFB	0x32	ODIV=6d
0xFC	0x25	INT =37d
0xFD	0xBC	FRAC(Lower 8bits)
0xFE	0x74	FRAC(Medium 8bits)
0xFF	0x03	FRAC(Upper 2bits) FRAC=-35652d

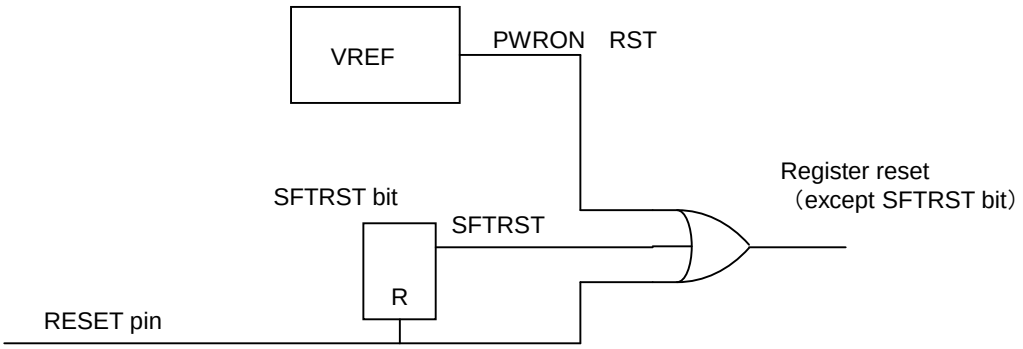
Power up sequence

Supplying proper voltage to the power pins.
*Note: VDD1, VDD2, VDD3 must be supplied simultaneously.
Power-on-reset is executed by setting RESET = “L” during start up.
SCL / SDA are acceptable 1ms later.
*Note: When using RESET signal, It takes 500us after releasing the RESET to accept SCL / SDA access.



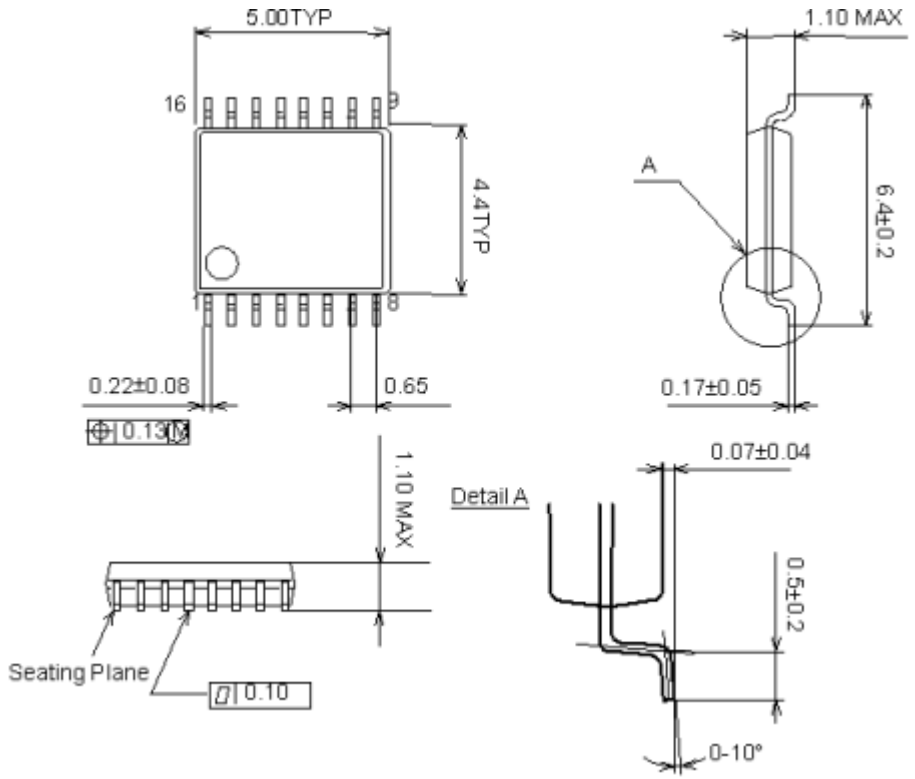
Reset circuit

To reset this IC, these tree methods are available.
1) Internal power-on-reset
2) Hardware reset by RESET pin
3) Software reset by “SFTSRT” of register F7
The “SFTRST” bit is not cleared by power-on-reset. It should be manually set to “0” after power-on-reset if it is necessary.

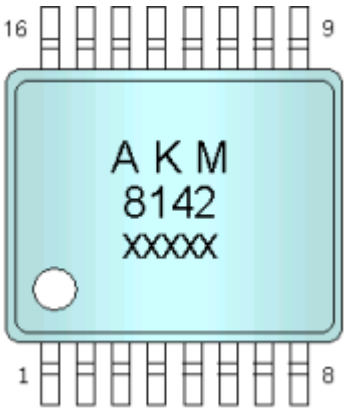


Package Information

Mechanical data (Units:mm)



Marking



a: #1 Pin Index

b: Product Family Logo *)

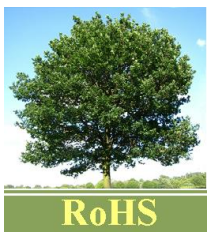
c: Part number

c: Date code (5digits)

*) **AKM** is the brand name of AKEMD's IC's.

AKM and the logo - AKM - are the brand of AKEMD's IC's and identify that AKEMD continues to offer the best choice for high performance mixed-signal solution under this brand.

RoHS Compliance



All integrated circuits form Asahi Kasei EMD Corporation (AKEMD) assembled in "lead-free" packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKEMD are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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