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PCS3P7303A

General Purpose Peak EMI Reduction IC

General Features

- 1x, LVCMOS Peak EMI Reduction
- Input frequency:
  - 10MHz - 70MHz @ 2.5V
  - 10MHz - 80MHz @ 3.3V
- Output frequency:
  - 10MHz - 70MHz @ 2.5V
  - 10MHz - 80MHz @ 3.3V
- Analog Deviation Selection
- ModRate selection option
- Supply Voltage: 2.5V ± 0.2V
  - 3.3V ± 0.3V
- 8-pin TSSOP, 8L 2mmX2mm WDFN(TDFN) Packages
- The First True Drop-in Solution

Functional Description

PCS3P7303A is a versatile, 3.3V/2.5V Peak EMI reduction IC based on Timing-Safe™ technology. PCS3P7303A accepts an input clock either from a Crystal or from an external reference (AC or DC coupled to XIN / CLKIN) and locks on to it delivering a 1x modulated clock output. PCS3P7303A has a Frequency Selection (FS) control that facilitates selecting one of the two frequency ranges within the operating frequency range. Refer to the *Frequency Selection* Table for details.

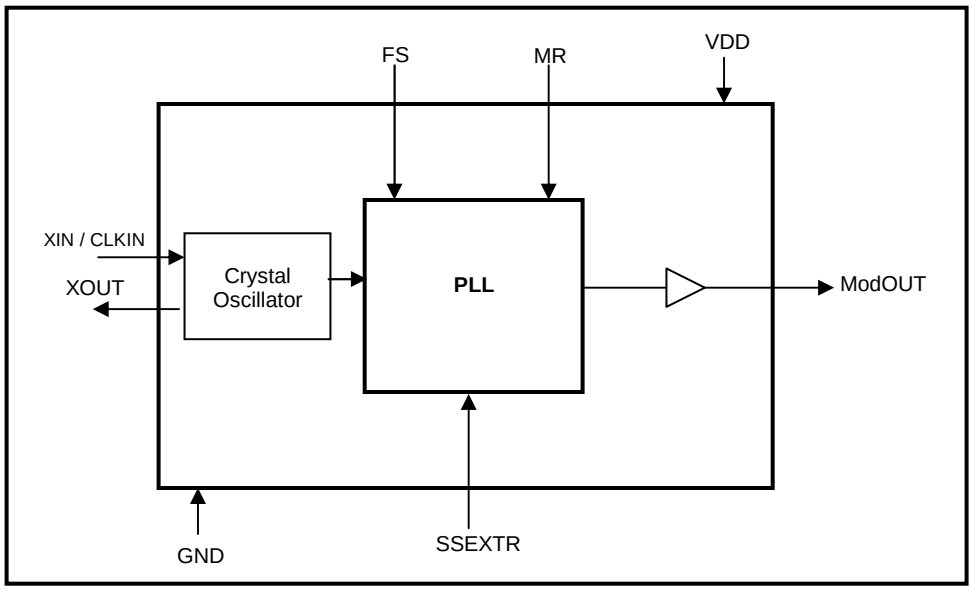
PCS3P7303A has an SSEXTR pin to select different deviations depending upon the value of an external resistor connected between SSEXTR and GND. Modulation Rate (MR) control selects two different Modulation Rates.

PCS3P7303A operates from a 3.3V/2.5V supply and is available in an 8-pin TSSOP and 8L 2mmX2mm WDFN packages.

Application

PCS3P7303A is targeted for many applications including USB and SATA.

Block Diagram



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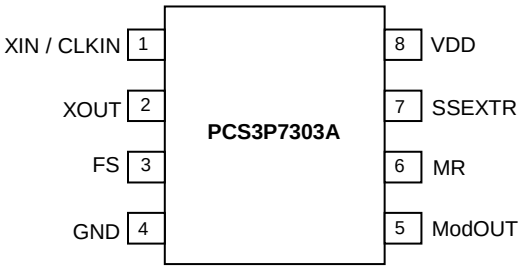
Publication Order Number:
PCS3P7303/D

Pin Configuration



Pin Description

Pin #	Pin Name	Pin Type	Description
1	XIN / CLKIN	I	Crystal connection or External reference clock input.
2	XOUT	O	Crystal connection. If using an external reference, this pin should be left open.
3	FS	I	Frequency Select. Pull LOW to select Low Frequency range. Selects High Frequency range when pulled HIGH. Has an internal pull-up resistor. (See *Frequency Selection table* for details.)
4	GND	P	Ground.
5	ModOUT	O	Buffered Modulated clock output.
6	MR	I	Modulation Rate Select. When LOW selects Low Modulation Rate. Selects High Modulation Rate when pulled HIGH. Has an internal pull-down resistor.
7	SSEXTR	I	Analog Deviation Selection through external resistor to GND.
8	VDD	P	2.5V / 3.3V supply Voltage.

Frequency Selection Table

VDD (V)	FS	Frequency (MHz)
2.5	0	10-35
	1	30-70
3.3	0	10-40
	1	30-80

Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any input pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	2.3	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-25	+85	℃
C_L	Load Capacitance		10	pF
C_{IN}	Input Capacitance		7	pF

DC Electrical Characteristics for 2.5V

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
VDD	Supply Voltage			2.3	2.5	2.7	V
V_{IL}	Input LOW Voltage					0.7	V
V_{IH}	Input HIGH Voltage			1.7			V
I_{IL}	Input LOW Current	V_{IN} = 0V				-50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				50	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA				0.6	V
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		1.8			V
I_{CC}	Static Supply Current	XIN / CLKIN pulled low				500	µA
I_{DD}	Dynamic Supply Current	Unloaded Output	FS=0; @ 10MHz			5	mA
			FS=1; @ 70MHz			12	
Z_o	Output Impedance				45		Ω

Switching Characteristics for 2.5V

Parameter	Test Conditions			Min	Typ	Max	Unit
Input Frequency[1] /	FS=0			10		35	MHz
ModoUT	FS=1			30		70	
Duty Cycle [2, 3]	Measured at V_{DD} /2			45	50	55	%
Output Rise Time [2, 3]	Measured between 20% to 80%				1.75	2.5	nS
Output Fall Time [2,3]	Measured between 80% to 20%				1.0	1.6	nS
Cycle-to-Cycle Jitter [3]	Unloaded output	FS=0	10MHz		±450	±600	pS
			35MHz		±125	±250	
		FS=1	30MHz		±225	±350	
			70MHz		±150	±300	
PLL Lock Time [3]	Stable power supply, valid clock presented on XIN / CLKIN					3	mS

Notes: 1. Functionality with Crystal is guaranteed by design and characterization. Not 100% tested in production.
2. All parameters are specified with 10pF loaded outputs.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

DC Electrical Characteristics for 3.3V

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
VDD	Supply Voltage			3.0	3.3	3.6	V
V_{IL}	Input LOW Voltage					0.8	V
V_{IH}	Input HIGH Voltage			2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V				-50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				50	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA				0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		2.4			V
I_{CC}	Static Supply Current	XIN / CLKIN pulled low				700	µA
I_{DD}	Dynamic Supply Current	Unloaded Output	FS=0; @ 10MHz			7	mA
			FS=1; @ 80MHz			20	
Z_o	Output Impedance				35		Ω

Switching Characteristics for 3.3V

Parameter	Test Conditions			Min	Typ	Max	Unit
Input Frequency[1] / ModOUT	FS=0			10		40	MHz
	FS=1			30		80	
Duty Cycle [2, 3]	Measured at V_{DD} /2			45	50	55	%
Output Rise Time [2, 3]	Measured between 20% to 80%				1.3	2	nS
Output Fall Time [2, 3]	Measured between 80% to 20%				0.9	1.3	nS
Cycle-to-Cycle Jitter [3]	Unloaded output	FS=0	10MHz		±450	±600	pS
			40MHz		±125	±250	
		FS=1	30MHz		±225	±350	
			80MHz		±125	±250	
PLL Lock Time [3]	Stable power supply, valid clock presented on XIN / CLKIN					3	mS

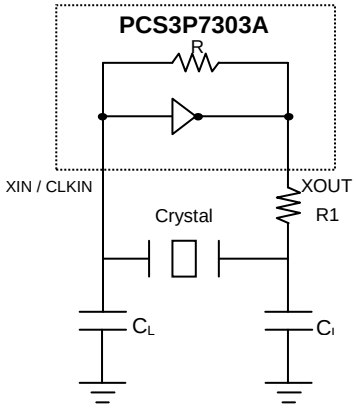
Notes: 1. Functionality with Crystal is guaranteed by design and characterization. Not 100% tested in production.
2. All parameters are specified with10pF loaded outputs.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	25MHz
Frequency tolerance	±50ppm or better at 25℃
Operating temperature range	-25℃ to +85℃
Storage temperature	-40℃ to +85℃
Load capacitance(C_P)	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

Note: C_L is the Load Capacitance and R1 is used to prevent oscillations at overtone frequency of the Fundamental frequency.

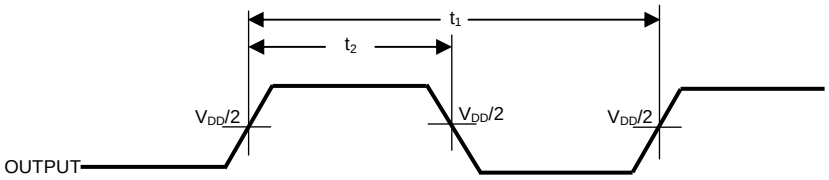
Typical Crystal Interface Circuit



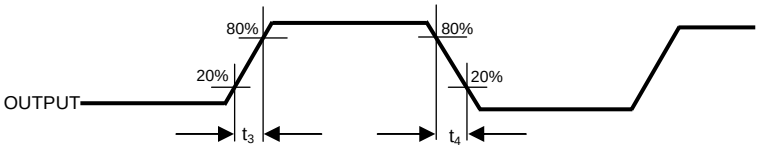
$C_L = 2*(C_P – C_S)$,
Where C_P = Load capacitance of crystal from crystal vendor datasheet.
C_S = Stray capacitance due to $C_{IN,}$ PCB, Trace, etc.

Switching Waveforms

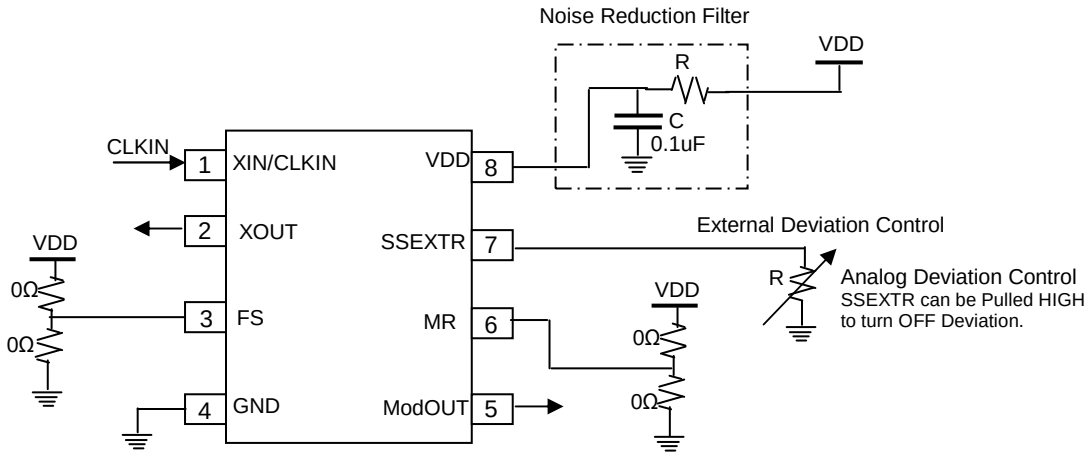
Duty Cycle Timing



Output Rise/Fall Time

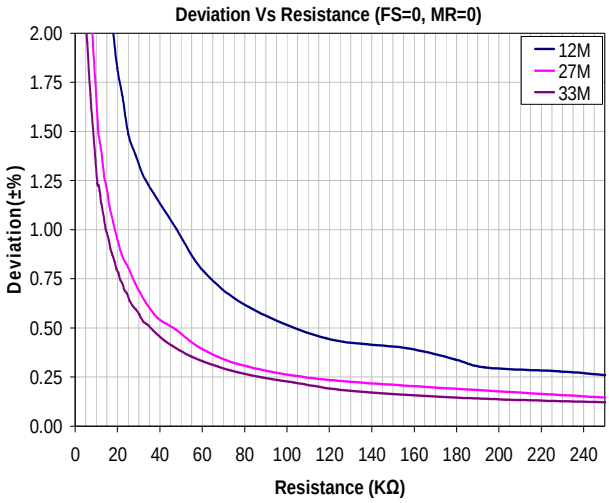


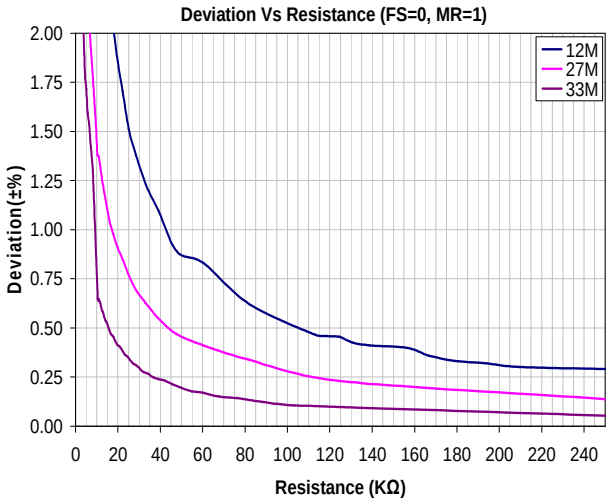
Application Schematic

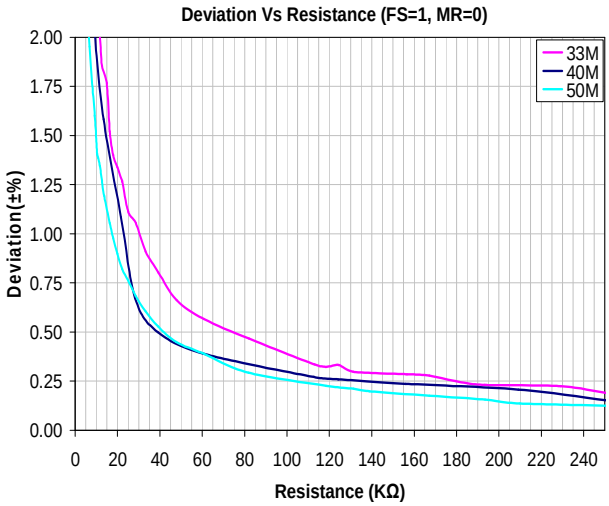


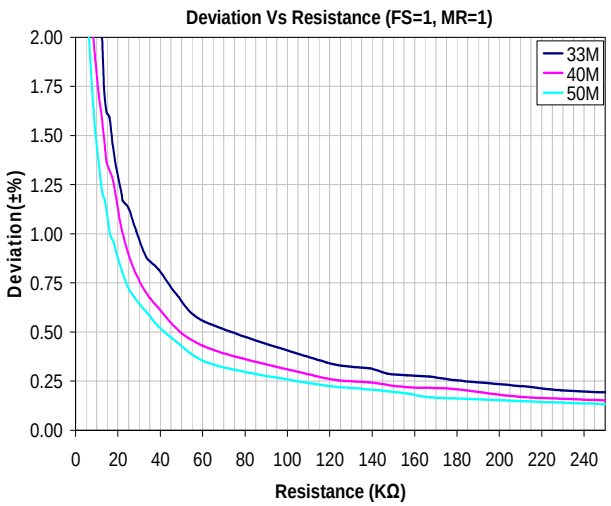
Note: FS (Pin#3) MR (Pin#6): Connect to VDD or GND
Refer to Pin Description table for Functionality details.

Charts





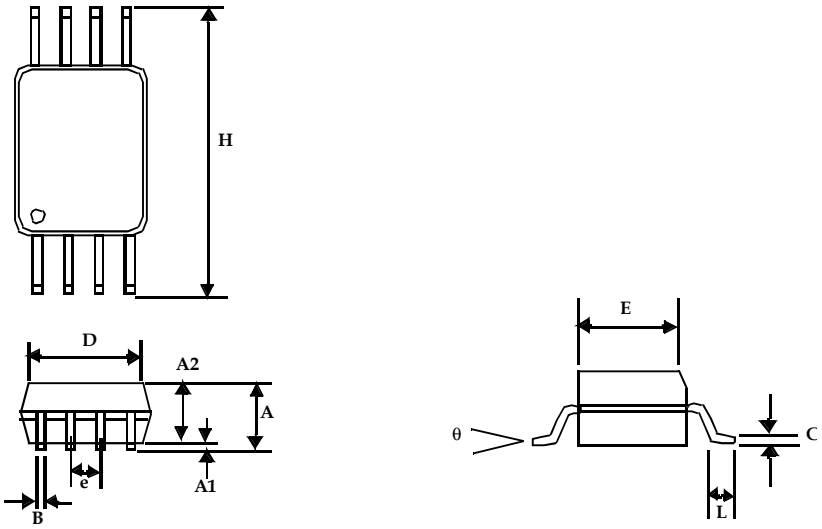




Note: Device to Device variation of Deviation is ±10% (0℃ to +70℃) and ±25% (-25℃ to +85℃)

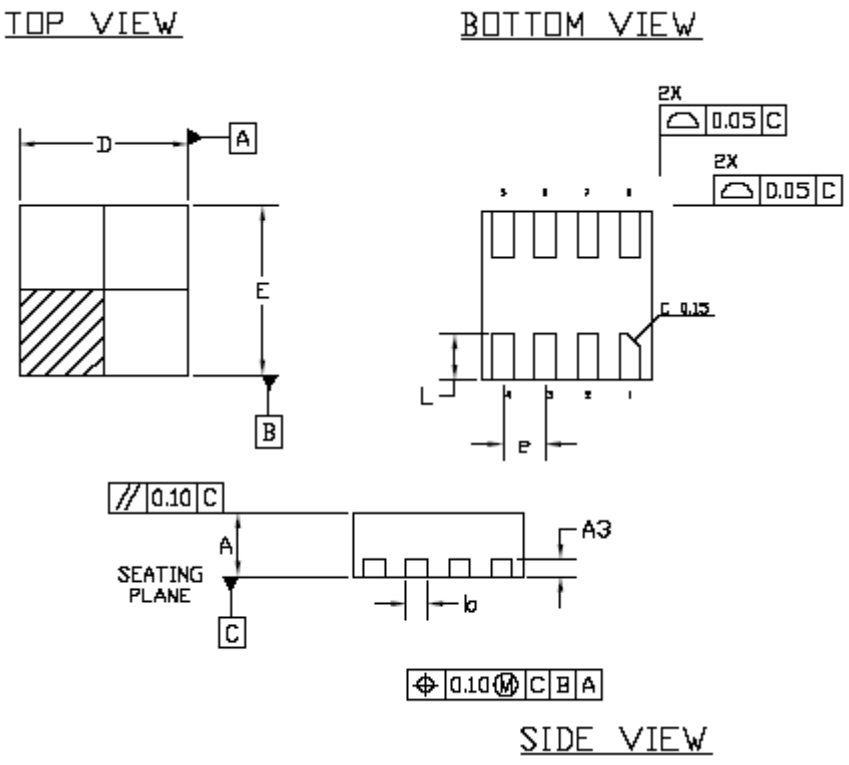
Package Information

8-lead TSSOP Package (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

8L 2mmX2mm WDFN package Outline drawing



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.027	0.0315	0.70	0.80
A3	0.008 BSC		0.203 BSC	
b	0.008	0.012	0.20	0.30
D	0.079 BSC		2.00 BSC	
E	0.078 BSC		2.00 BSC	
e	0.020 BSC		0.50 BSC	
L	0.020	0.024	0.50	0.60

Ordering Code

Part Number	Marking	Package	Temperature
PCS3P7303AG-08TR	BKL	8-pin TSSOP, TAPE AND REEL, Green	-25℃ to +85℃
PCS3P7303AG-08TT	BKL	8-pin TSSOP, TUBE, Green	-25℃ to +85℃
PCS3P7303AG-08CR	BK	8L WDFN (2mmX2mm), TAPE & REEL, Green	-25℃ to +85℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

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