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PCS3PS550A

General Purpose Peak EMI Reduction IC

ON Semiconductor®

www.onsemi.com

Product Description

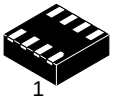
The PCS3PS550A is a versatile 2.3 V to 3.6 V, Timing−Safe™, spectrum frequency modulator designed specifically for a wide range of clock frequencies. The PCS3PS550A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The PCS3PS550A allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding that are traditionally required to pass EMI regulations.

Features

- LVCMOS Peak EMI reduction IC
- Input Clock Frequency: 18 MHz − 40 MHz
- Output Clock Frequency: 18 MHz − 40 MHz
- Eight different selectable Spread options
- Power Down option for power save
- Supply Voltage: 2.3 V − 3.6 V
- 8−pin WDFN , 2 mm x 2 mm (TDFN) Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

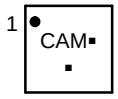
Applications

- The PCS3PS550A is targeted towards consumer electronic applications.



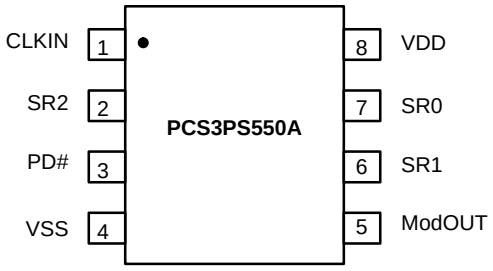
WDFN8
CASE 511AQ

MARKING DIAGRAMS



CA = Specific Device Code
M = Date Code
▪ = Pb−Free Device

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

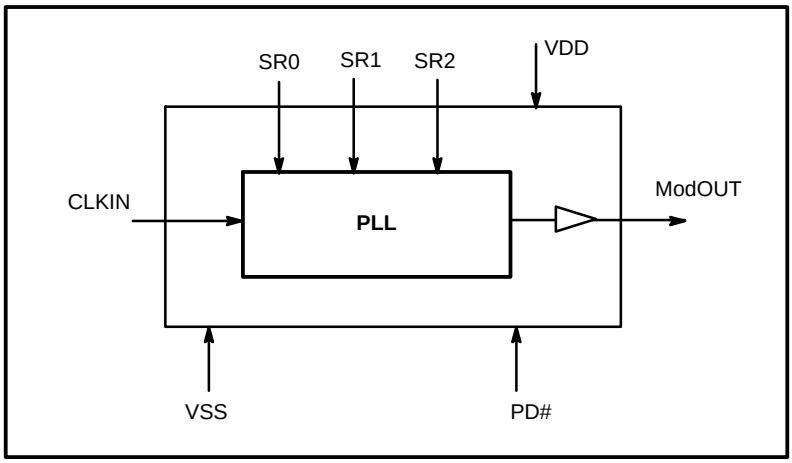


Figure 1. Block Diagram

PCS3PS550A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

PCS3PS550A accepts an input from an external reference clock and locks to a 1x modulated clock output. SR0, SR1 and SR2 pins enable selecting one of the eight different frequency deviations (Refer *Frequency Deviation Selection table).* PCS3PS550A also features power down option for power save. PCS3PS550A operates over a supply voltage range of 2.3 V to 3.6 V. PCS3PS550A is available in an 8 Pin WDFN, (2 mm x 2 mm) Package.

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference clock input.
2	SR2	I	Digital logic input used to select Spreading Range. There is NO default state. Refer Frequency Deviation Selection Table.
3	PD#	I	Power−down control pin. Powers down the entire chip. There is NO default state. Pull low to enable power−down mode. Connect to VDD to disable Power Down. Output Clock will be LOW when power down is enabled
4	VSS	P	Ground connection.
5	ModOUT	O	Spread Spectrum Clock Output.
6	SR1	I	Digital logic input used to select Spreading Range. This pin has an internal pull−up resistor. *Refer Modulation Selection Table.*
7	SR0	I	Digital logic input used to select Spreading Range. There is NO default state. Refer Frequency Deviation Selection Table.
8	VDD	P	Power supply for the entire chip

Table 2. FREQUENCY DEVIATION SELECTION TABLE

SR2	SR1	SR0	Spreading Range (±%) (@ 24 MHz)
0	0	0	1
0	0	1	2.5
0	1	0	1.25
0	1	1	1.5
1	0	0	0.4
1	0	1	0.75
1	1	0	1.75
1	1	1	2

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage with respect to V_{SS}	2.3	3.6	V
T_A	Operating temperature	−20	+85	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Table 4. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any input pin with respect to VSS	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_A	Operating temperature	−40 to +85	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22−A114−B)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

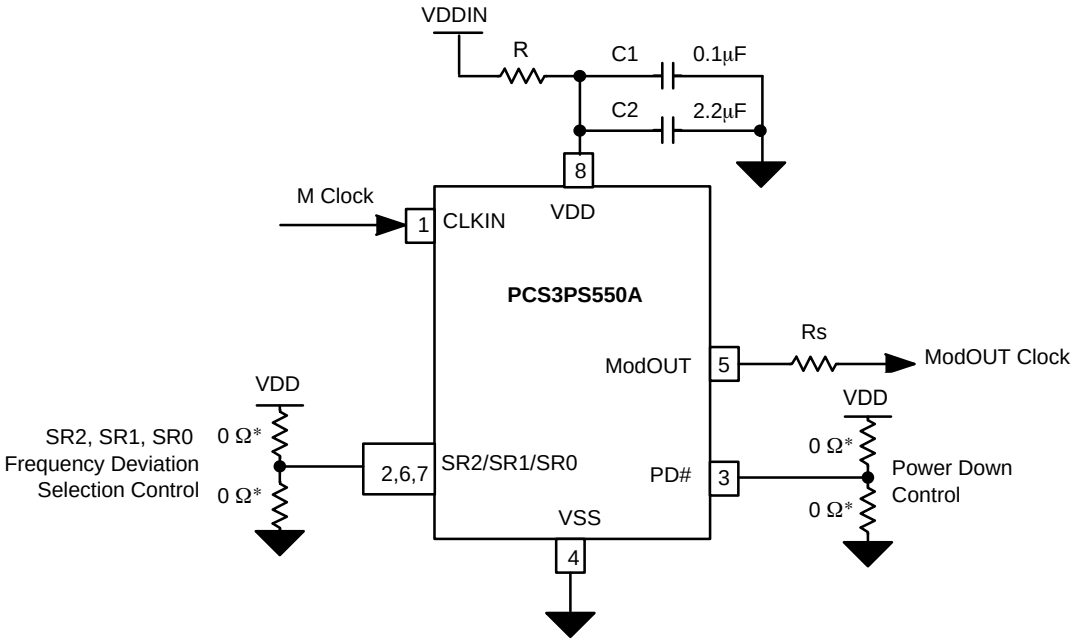
Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage with respect to V_{SS}	2.3	2.8	3.6	V
V_{IH}	Input high voltage	0.65 * V_{DD}			V
V_{IL}	Input low voltage			0.3 * V_{DD}	V
I_{IH}	Input high current (SR1 control pin)			50	μA
I_{IL}	Input low current (SR1 control pin)			50	μA
V_{OH}	Output high voltage (I_{OH} = −8 mA)	0.75 * V_{DD}			V
V_{OL}	Output low voltage (I_{OL} = 8 mA)			0.2 * V_{DD}	V
I_{CC}	Static supply current (PD# pulled to V_{SS})			1	μA
I_{DD}	Dynamic supply current (Unloaded Output @ 24 MHz)		6	9	mA
Z_{OUT}	Output impedance		40		Ω

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN	Input Clock frequency		18	24	40	MHz
ModOUT	Output Clock frequency		18	24	40	MHz
t_{LH} (Note 1)	Output rise time (Measured between 20% to 80%)	Unloaded Output		0.8	1.2	ns
		CL = 15 pF		2.4	3	
t_{HL} (Note 1)	Output fall time (Measured between 80% to 20%)	Unloaded Output		0.6	1	ns
		CL = 15 pF		1.9	2.8	
t_{JC} (Note 1)	Jitter (cycle to cycle) Unloaded Output			±175	±250	ps
t_D (Note 1)	Output duty cycle		45	50	55	%
t_{ON} (Note 1)	PLL lock Time (Stable power supply, valid clock presented on CLKIN pin, PD# toggled from Low to High)				3	ms
fd_{var}	Frequency Deviation Variation across PVT			±2.5	±5	%

1. Parameter is guaranteed by design and characterization. Not 100% tested in production



NOTE: Refer Pin Description table for Functionality details.

*Choose the 0 Ohms resistor either to VDD or to VSS based on the logic state to be set for the control signal

Figure 2. Typical Application Schematic

PCB Layout Recommendation

For optimum device performance, following guidelines are recommended.

- Dedicated V_{DD} and V_{SS} (GND) planes.
- The device must be isolated from system power supply noise. A 0.1μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the figure

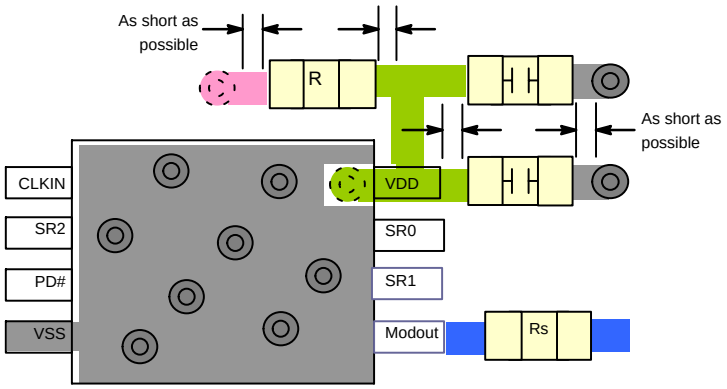


Figure 3.

ORDERING INFORMATION

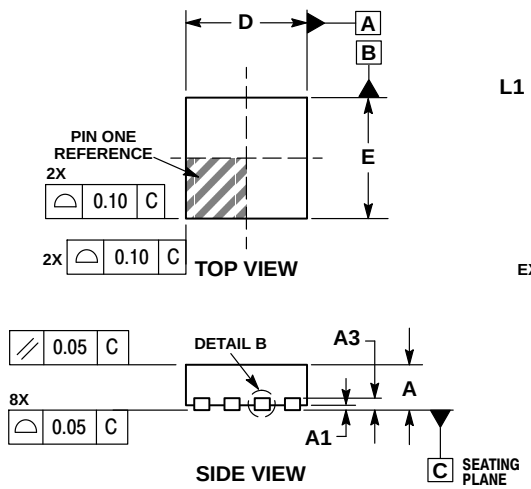
Part Number	Top Marking	Temperature	Package Type	Shipping†
PCS3PS550AG−08CR	CA	−20°C to +85°C	8L− WDFN (TDFN) (Pb−Free)	3000 / Tape & Reel

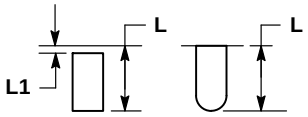
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

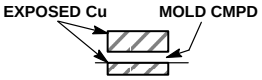
*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P
CASE 511AQ
ISSUE A

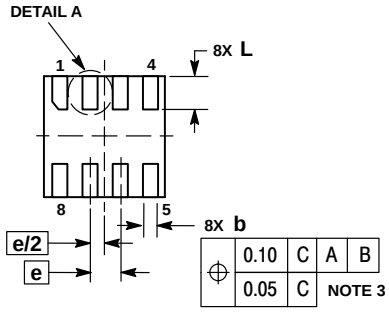




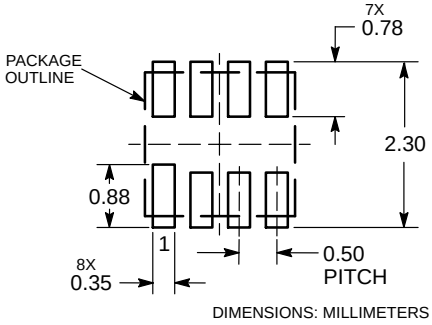


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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