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P3P8203A

General Purpose Peak EMI Reduction Device

Functional Description

P3P8203A is a versatile, 3.3 V LVC MOS Peak EMI reduction device.

P3P8203A accepts an input clock either from a Fundamental Crystal or from an external reference and locks on to it delivering a 1x modulated clock.

P3P8203A has an SSEXTR pin to select different deviations depending upon the value of an external resistor connected between SSEXTR and GND.

P3P8203A operates with 3.3 V ± 0.3 V supply and is available in an 8 Pin, WDFN (2 mm X 2 mm) Package, over a temperature range of 0°C to +70°C.

Features

- 1x, LVC MOS Peak EMI Reduction
- Supports non-continuous input clock applications
- Input / output frequency range: 18 MHz – 36 MHz
- Analog Deviation Selection
- Supply Voltage: 3.3 V ± 0.3 V
- 8 pin, WDFN (2 mm X 2 mm) package
- Operating Temperature range: 0°C to +70°C
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Application

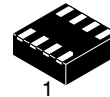
- P3P8203A is targeted for use in a broad range of note book and desktop PCs and consumer electronic applications.



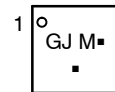
ON Semiconductor®

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MARKING DIAGRAM



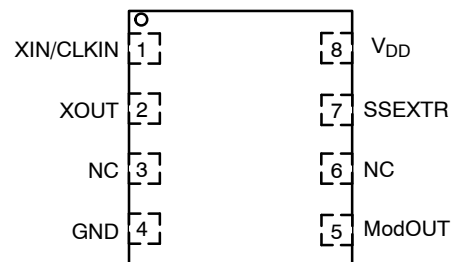
WDFN8
CASE 511AQ



GJ = Specific Device Code
M = Date Code
▪ = Pb-Free Device

(*Note: Microdot may be in either location)

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

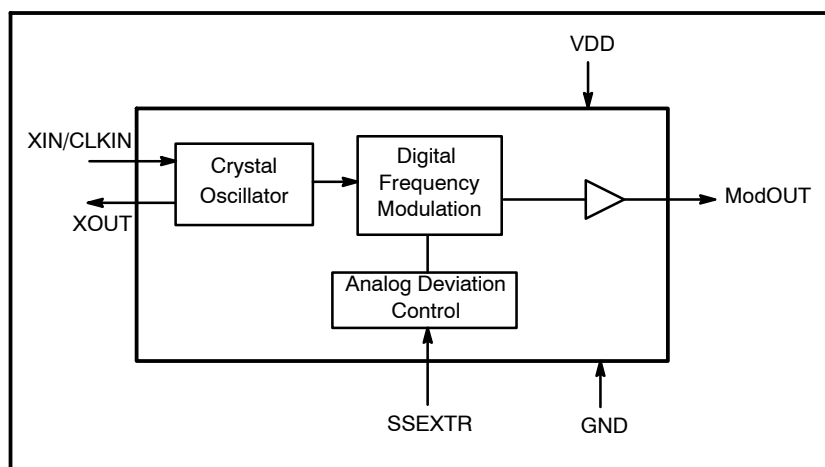


Figure 1. Block Diagram

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Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	XIN/CLKIN	Input	Crystal connection or External reference clock input.
2	XOUT	Output	Crystal connection. If using an external reference, this pin should be left open.
3	NC		No connection
4	GND	Power	Ground
5	ModOUT	Output	Buffered Modulated Clock output.
6	NC		No connection
7	SSEXTR	Input	Analog Deviation Selection through external resistor to GND.
8	VDD	Power	Supply Voltage

Table 2. OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
V _{DD}	Supply Voltage	3.0	3.6	V
T _A	Operating Temperature (Ambient Temperature)	0	70	°C
C _L	Load Capacitance		15	pF
C _{IN}	Input Capacitance		7	pF

Table 3. ABSOLUTE MAXIMUM RATING

Symbol	Description	Rating	Unit
V _{DD} , V _{IN}	Voltage on any input pin with respect to Ground	-0.5 to +4.6	V
T _{STG}	Storage temperature	-65 to +125	°C
T _s	Max. Soldering Temperature (10 sec)	260	°C
T _J	Junction Temperature	150	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22-A114-B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{DD}	Supply Voltage		3.0	3.3	3.6	V
V _{IL}	Input LOW Voltage				0.35 * V _{DD}	V
V _{IH}	Input HIGH Voltage		0.65 * V _{DD}			V
V _{OL}	Output LOW Voltage	I _{OL} = 8 mA			0.25 * V _{DD}	V
V _{OH}	Output HIGH Voltage	I _{OH} = -8 mA	0.75 * V _{DD}			V
I _{CC}	Static Supply Current	CLKIN pulled LOW			1	mA
I _{DD}	Dynamic Supply Current	Unloaded output	18 MHz		5	mA
			24 MHz		6	
			36 MHz		8	
C _L	Load Capacitance				15	pF
Z ₀	Output Impedance			24		Ω

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Table 5. SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Clock Frequency		18		36	MHz
ModOUT		18		36	
Output Rise Time (Notes 1 and 2)	Measured between 20% to 80%		1.0	1.6	nS
Output fall Time (Notes 1 and 2)	Measured between 80% to 20%		1.0	1.6	nS
Output Duty Cycle (Notes 1 and 2)	Measured at 50% (with Input Duty Cycle of 50%)	45	50	55	%
Cycle-to-Cycle Jitter (Note 2)	Unloaded output with SSEXTR pin OPEN		±100		pS
Part-Part Frequency Deviation Variation			±20		%

1. All parameters are measured with 15pF load on ModOUT.
2. Parameter is guaranteed by design and characterization. Not tested in production.

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SWITCHING WAVEFORMS

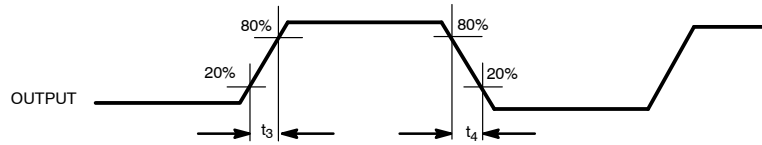


Figure 2. Output Rise/Fall Time

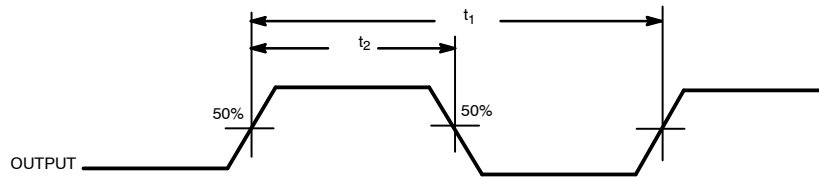


Figure 3. Duty Cycle Timing

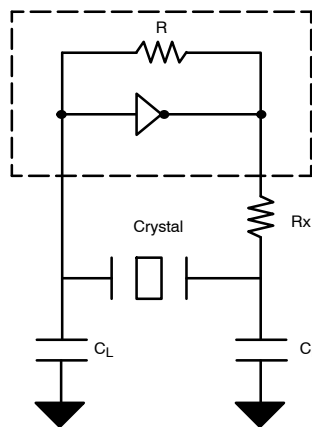


Figure 4. Typical Crystal Interface Circuit

$$C_L = 2 * (C_P - C_S)$$

Where C_P = Load capacitance of crystal specified in a Crystal Datasheet

C_S = Stray capacitance due to CIN, PCB, Trace etc

C_L = Load capacitance to be used

R_x is used to reduce power dissipation in the Crystal

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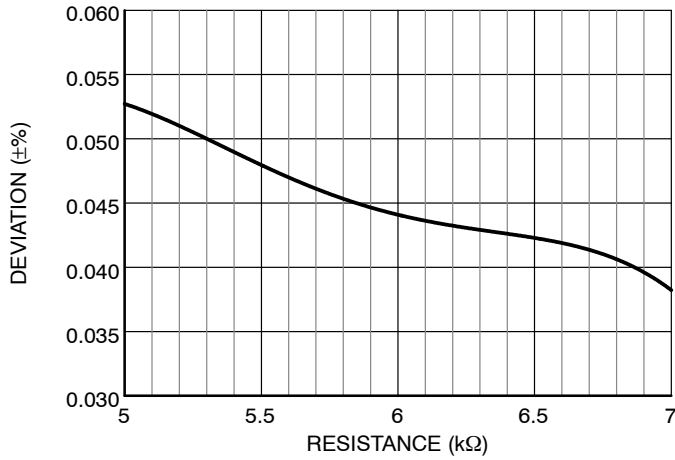
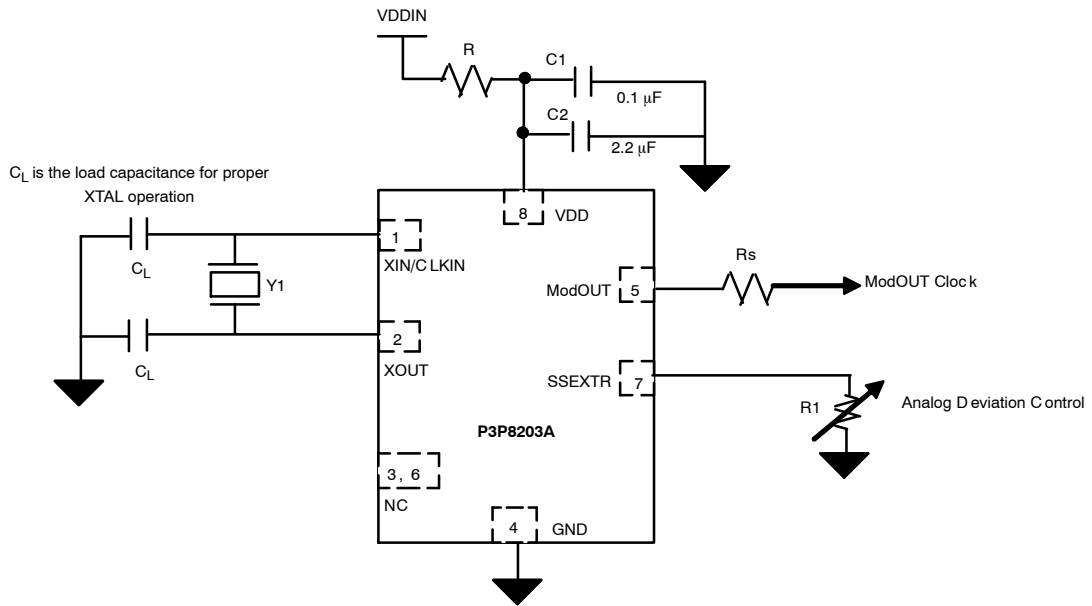


Figure 5. Deviation vs. SSEXTR (@ 27 MHz)

(NOTE: Parameter is guaranteed by design and characterization. Not tested in production.)



Note: Refer Pin Description table for Functionality details

Figure 6. Typical Application Circuit

R_s = Trace Impedance of PCB – Output Impedance of Device (Z_0)

ORDERING INFORMATION

Ordering Code	Marking	Temperature	Package Type	Shipping [†]
P3P8203AMTTBG	GJ	0°C to +70°C	8-pin (2 mm x 2 mm) WDFN (Pb-Free)	3000 / Tape & Reel

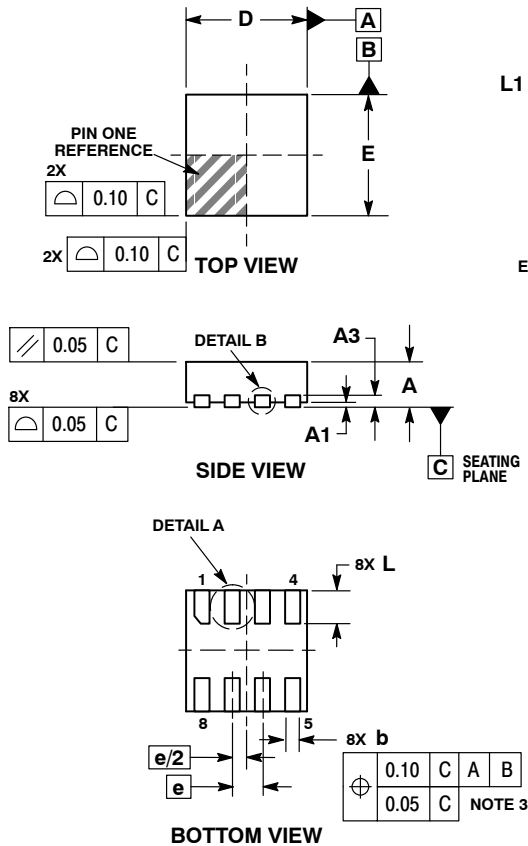
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-Free.

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PACKAGE DIMENSIONS

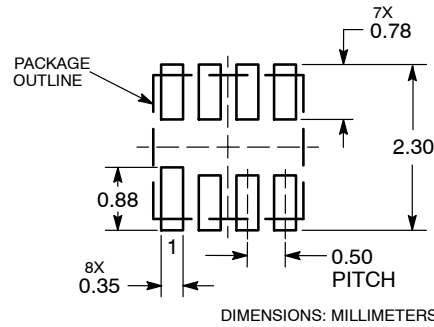
WDFN8 2x2, 0.5P
CASE 511AQ
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

MILLIMETERS		
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
E	2.00	BSC
e	0.50	BSC
L	0.50	0.60
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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