

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NB3N502

14 MHz to 190 MHz PLL Clock Multiplier

Description

The NB3N502 is a clock multiplier device that generates a low jitter, TTL/CMOS level output clock which is a precise multiple of the external input reference clock signal source. The device is a cost efficient replacement for the crystal oscillators commonly used in electronic systems. It accepts a standard fundamental mode crystal or an external reference clock signal. Phase-Locked-Loop (PLL) design techniques are used to produce an output clock up to 190 MHz with a 50% duty cycle. The NB3N502 can be programmed via two select inputs (S0, S1) to provide an output clock (CLKOUT) at one of six different multiples of the input frequency source, and at the same time output the input aligned reference clock signal (REF).

Features

- Clock Output Frequency up to 190 MHz
- Operating Range: $V_{DD} = 3\text{ V to }5.5\text{ V}$
- Low Jitter Output of 15 ps One Sigma (rms)
- Zero ppm Clock Multiplication Error
- 45% – 55% Duty Cycle
- 25 mA TTL-level Drive Outputs
- Crystal Reference Input Range of 5 – 27 MHz
- Input Clock Frequency Range of 2 – 50 MHz
- Available in 8-pin SOIC Package or in Die Form
- Full Industrial Temperature Range $-40^{\circ}\text{C to }85^{\circ}\text{C}$
- These are Pb-Free Devices

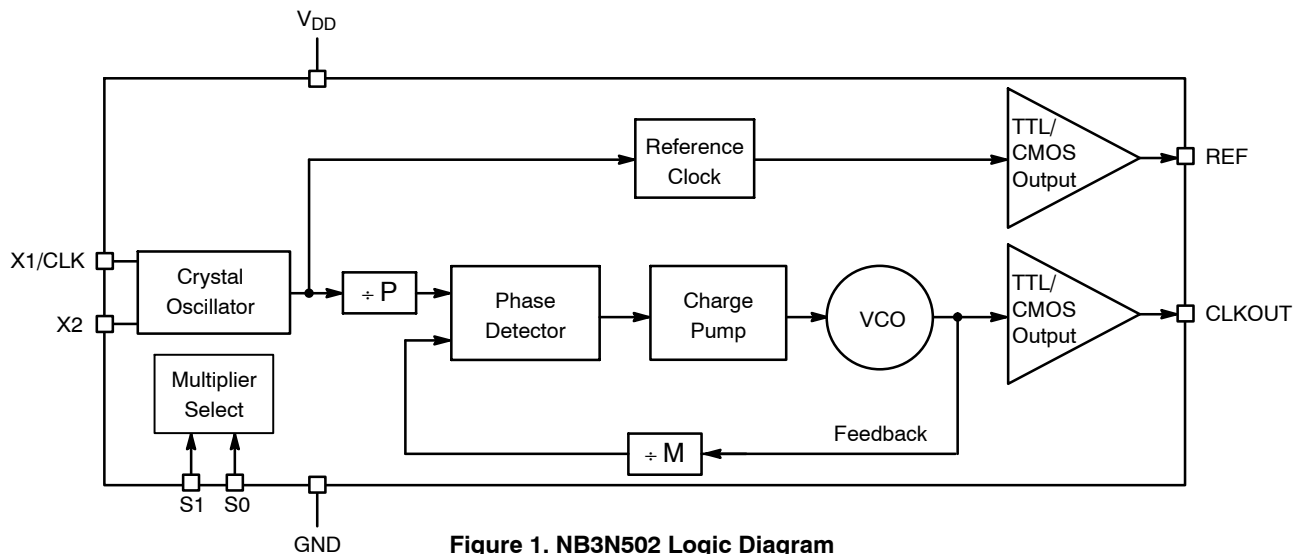


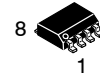
Figure 1. NB3N502 Logic Diagram



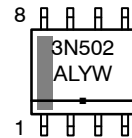
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



SOIC-8
D SUFFIX
CASE 751



3N502 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NB3N502DG	SOIC-8 (Pb-Free)	98 Units / Rail
NB3N502DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NB3N502

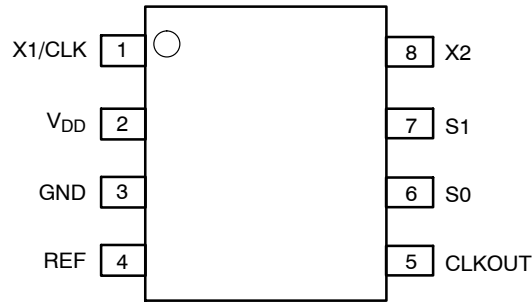


Figure 2. Pin Configuration (Top View)

Table 1. CLOCK MULTIPLIER SELECT TABLE

S1*	S0**	Multiplier
L	L	2X
L	H	5X
M	L	3X
M	H	3.33X
H	L	4X
H	H	2.5X

L = GND
 H = V_{DD}
 M = OPEN (unconnected)
 * Pin S1 defaults to M when left open
 ** Pin S0 defaults to H when left open

Table 2. OUTPUT FREQUENCY EXAMPLES

Output Frequency (MHz)	20	25	33.3	48	50	54	64	66.66	75	100	108	120	135
Input Frequency (MHz)	10	10	10	16	20	13.5	16	20	15	20	27	24	27
S1, S0	0, 0	1, 1	M, 1	M, 0	1, 1	1, 0	1, 0	M, 1	0, 1	0, 1	1, 0	0, 1	0, 1

Table 3. PIN DESCRIPTION

Pin #	Name	I/O	Description
1	X1/CLK	Input	Crystal or External Reference Clock Input
2	V _{DD}	Power Supply	Positive Supply Voltage (3 V to 5.5 V)
3	GND	Power Supply	0 V Ground.
4	REF	CMOS/TTL Output	Buffered Crystal Oscillator Clock Output
5	CLKOUT	CMOS/TTL Output	Clock Output
6	S0	CMOS/TTL Input	Multiplier Select Pin – Connect to V _{DD} or GND. Internal Pull-up Resistor.
7	S1	Three-level Input	Multiplier Select Pin – Connect to V _{DD} , GND or Float to M.
8	X2	Crystal Input	Crystal Input – Do Not Connect when Providing an External Clock Reference

Table 4. ATTRIBUTES

Characteristic	Value
ESD Protection	Human Body Model Machine Model
	> 8 kV > 600 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	6700 Devices
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test	

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

NB3N502

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{DD}	Positive Power Supply	GND = 0 V		7	V
V _I	Input Voltage			GND - 0.5 = V _I = V _{DD} + 0.5	V
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SOIC-8 SOIC-8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 1)	SOIC-8	41 to 44	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS (V_{DD} = 3 V to 5.5 V unless otherwise noted, GND = 0 V, T_A = -40°C to +85°C) (Note 2)

Symbol	Characteristic	Min	Typ	Max	Unit
I _{DD}	Power Supply Current (unloaded CLKOUT operating at 100 MHz with 20 MHz crystal)		20		mA
V _{OH}	Output HIGH Voltage I _{OH} = -25 mA TTL High	2.4			V
V _{OL}	Output LOW Voltage I _{OL} = 25 mA			0.4	V
V _{IH}	Input HIGH Voltage, CLK only (pin 1)	(V _{DD} / 2) + 1	V _{DD} / 2		V
V _{IL}	Input LOW Voltage, CLK only (pin 1)		V _{DD} / 2	(V _{DD} / 2) - 1	V
V _{IH}	Input HIGH Voltage, S0, S1	V _{DD} - 0.5			V
V _{IL}	Input LOW Voltage, S0, S1			0.5	V
V _{IM}	Input level of S1 when open (Input Mid Point)		V _{DD} ÷ 2		V
C _{in}	Input Capacitance, S0, S1		4		pF
I _{SC}	Output Short Circuit Current		± 70		mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Parameters are guaranteed by characterization and design, not tested in production.

Table 7. AC CHARACTERISTICS (V_{DD} = 3 V to 5.5 V unless otherwise noted, GND = 0 V, T_A = -40°C to +85°C) (Note 3)

Symbol	Characteristic	Min	Typ	Max	Unit
f _{Xtal}	Crystal Input Frequency	5		27	MHz
f _{CLK}	Clock Input Frequency	2		50	MHz
f _{OUT}	Output Frequency Range V _{DD} = 4.5 to 5.5 V (5.0 V ± 10%) V _{DD} = 3.0 to 3.6 V (3.3 V ± 10%)	14 14		190 120	MHz MHz
DC	Clock Output Duty Cycle at 1.5 V up to 190 MHz	45	50	55	%
t _{jitter (rms)}	Period Jitter (RMS, 1 σ)		15		ps
t _{jitter (pk-to-pk)}	Total Period Jitter, (peak-to-peak)		±40		ps
t _r /t _f	Output rise/fall time (0.8 V to 2.0 V / 2.0 V to 0.8 V)		1	2	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Parameters are guaranteed by characterization and design, not tested in production.

APPLICATIONS INFORMATION

High Frequency CMOS/TTL Oscillators

The NB3N502, along with a low frequency fundamental mode crystal, can build a high frequency CMOS/TTL output oscillator. For example, a 20 MHz crystal connected to the NB3N502 with the 5X output selected (S1 = L, S0 = H) produces a 100 MHz CMOS/TTL output clock.

External Components

Decoupling Instructions

In order to isolate the NB3N502 from system power supply, noise de-coupling is required. The 0.01 μF decoupling capacitor has to be connected between V_{DD} and GND on pins 2 and 3. It is recommended to place de-coupling capacitors as close as possible to the NB3N502 device to minimize lead inductance. Control input pins can be connected to device pins V_{DD} or GND, or to the V_{DD} and GND planes on the board.

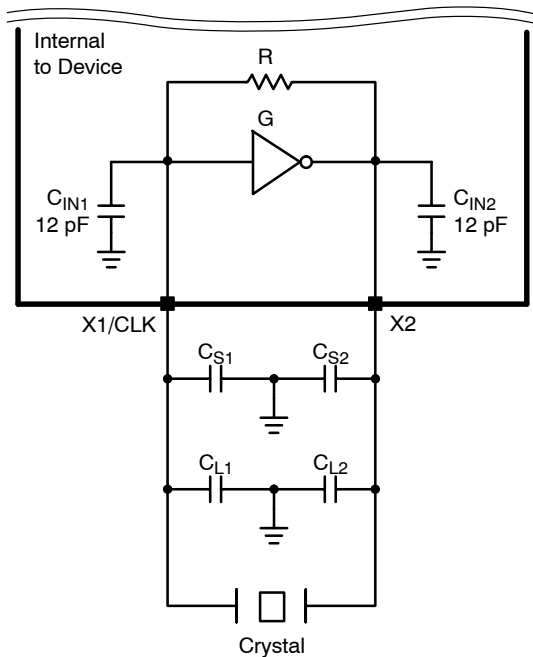
Series Termination Resistor Recommendation

A 33 Ω series terminating resistor can be used on the CLKOUT pin.

Crystal Load Capacitors Selection Guide

The total on-chip capacitance is approximately 12 pF per pin (C_{IN1} and C_{IN2}). A parallel resonant, fundamental mode crystal should be used.

The device crystal connections should include pads for small capacitors from X1/CLK to ground and from X2 to ground. These capacitors, C_{L1} and C_{L2}, are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance (C_{LOAD} (crystal)). Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal load capacitors, if needed, must be connected from each of the pins X1 and X2 to ground. The load capacitance of the crystal (C_{LOAD} (crystal)) must be matched by total load capacitance of the oscillator circuitry network, C_{INX}, C_{SX} and C_{LX}, as seen by the crystal (see Figure 3 and equations below).



$$C_{LOAD1} = C_{IN1} + C_{S1} + C_{L1} \text{ [Total capacitance on X1/CLK]}$$

$$C_{LOAD2} = C_{IN2} + C_{S2} + C_{L2} \text{ [Total capacitance on X2]}$$

$$C_{IN1} \approx C_{IN2} \approx 12 \text{ pF (Typ) [Internal capacitance]}$$

$$C_{S1} \approx C_{S2} \approx 5 \text{ pF (Typ) [External PCB stray capacitance]}$$

$$C_{LOAD1,2} = 2 \cdot C_{LOAD} \text{ (Crystal)}$$

$$C_{L2} = C_{LOAD2} - C_{IN2} - C_{S2} \text{ [External load capacitance on X2]}$$

$$C_{L1} = C_{LOAD1} - C_{IN1} - C_{S1} \text{ [External load capacitance on X1/CLK]}$$

Example 1: Equal stray capacitance on PCB

$$C_{LOAD} \text{ (Crystal)} = 18 \text{ pF (Specified by the crystal manufacturer)}$$

$$C_{LOAD1} = C_{LOAD2} = 36 \text{ pF}$$

$$C_{IN1} = C_{IN2} = 12 \text{ pF}$$

$$C_{S1} = C_{S2} = 6 \text{ pF}$$

$$C_{L1} = 36 - 12 - 6 = 18 \text{ pF}$$

$$C_{L2} = 36 - 12 - 6 = 18 \text{ pF}$$

Example 2: Different stray capacitance on PCB trace X1/CLK vs. X2

$$C_{LOAD} \text{ (Crystal)} = 18 \text{ pF}$$

$$C_{LOAD1} = C_{LOAD2} = 36 \text{ pF}$$

$$C_{IN1} = C_{IN2} = 12 \text{ pF}$$

$$C_{S1} = 4 \text{ pF} \ \& \ C_{S2} = 8 \text{ pF}$$

$$C_{L1} = 36 - 12 - 4 = 20 \text{ pF}$$

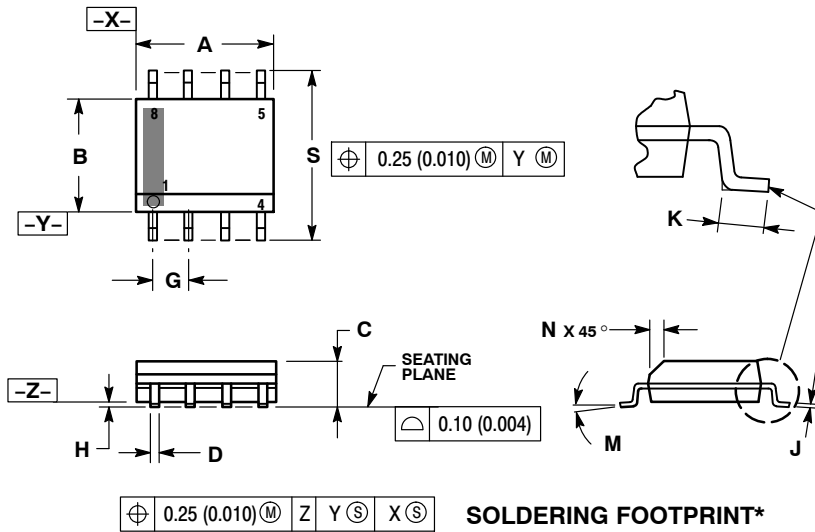
$$C_{L2} = 36 - 12 - 8 = 16 \text{ pF}$$

Figure 3. Using a Crystal as Reference Clock

NB3N502

PACKAGE DIMENSIONS

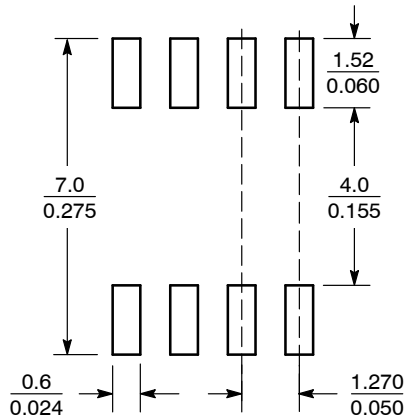
SOIC-8 NB CASE 751-07 ISSUE AK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°		8°	
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative