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SILICON LABS

Timing Solutions

PRODUCT SELECTOR GUIDE

Timing
The industry's broadest portfolio of oscillators, clock buffers, clock generators, PCI Express (PCIe) clocks and jitter attenuators.

Timing Solutions

Silicon Labs offers the industry's broadest portfolio of crystal oscillator, clock generator and clock buffer products and PCI Express (PCIe) clock generators and PCI Express buffers.

Silicon Labs' patented technology reduces system jitter and the number of expensive discrete components, while improving flexibility, customization and performance.

Comprehensive
- Crystal oscillators
- Clock buffers
- Clock generators
- Jitter attenuators

Flexible
- Simplifies clock generation with any-frequency synthesis
- Minimizes BOM cost and complexity

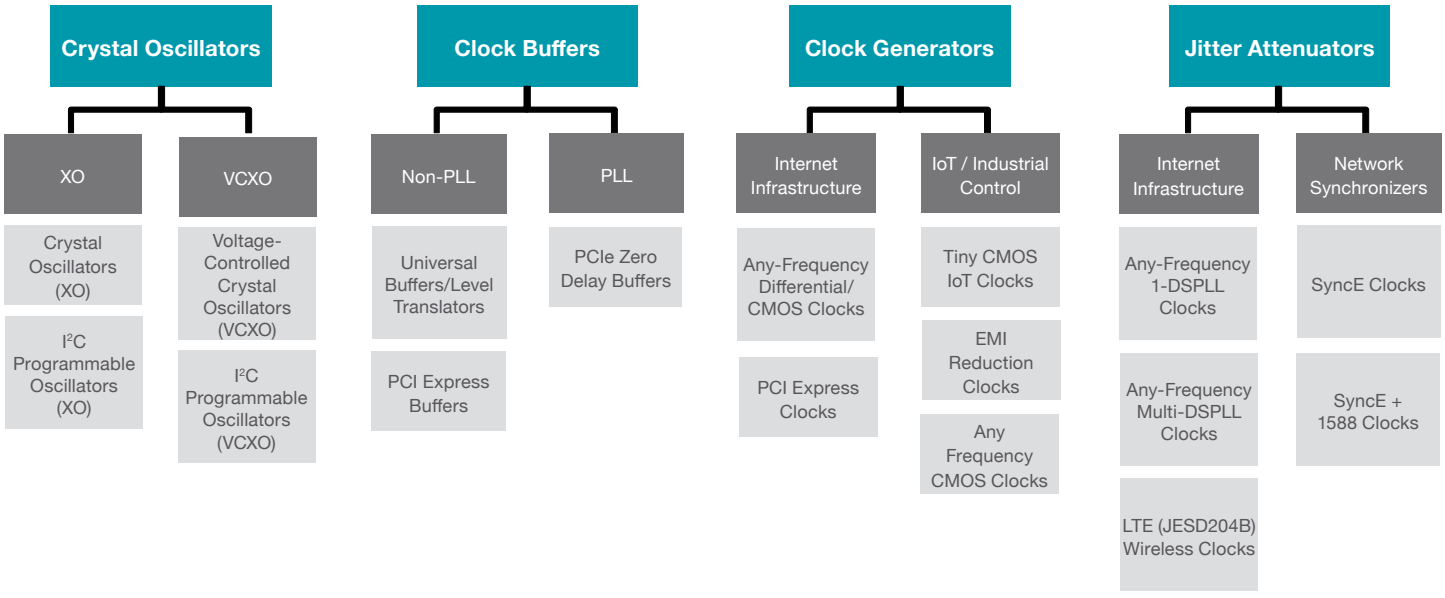
Performance
- Highly integrated to simplify design
- Ultra-low jitter optimizes system performance

Customized
- Web-customizable clocks and oscillators
- Quick-turn samples available in days

Featured Product

Silicon Labs' next-generation Si534x "clock-tree-on-a-chip" portfolio includes high-performance clock generators and highly integrated multi-PLL jitter attenuators. These single-chip, ultra-low-jitter timing devices lead the industry in jitter performance and frequency flexibility. Designed to meet the exacting specifications and high-performance requirements of Internet Infrastructure, these best-in-class, ultra-low-jitter clock devices reduce cost and complexity for a wide range of timing applications.

Timing Products



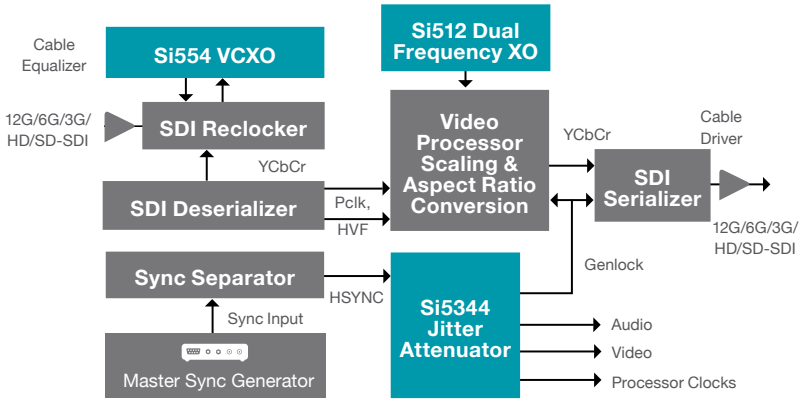
Crystal Oscillators (XO/VCXO)

REQUEST CUSTOM PART NUMBERS AND SAMPLES AT: www.silabs.com/oscillators

Silicon Labs' crystal oscillators and voltage-controlled crystal oscillators (XO/VCXOs) leverage advanced DSPLL® circuitry to provide a low jitter clock at any frequency from 100 kHz to 1.4 GHz. Unlike a traditional XO, where a different crystal is required for each output frequency, Silicon Labs' XO/VCXOs use a fixed frequency crystal and DSPLL clock synthesis IC to generate any output frequency. This IC-based approach delivers exceptional frequency stability and reliability, while providing best-in-class jitter performance and supply noise rejection, simplifying the task of generating low-jitter clocks in noisy environments. All devices are factory configurable for a wide variety of user specifications, including frequency, supply voltage, output format and stability, thereby eliminating long lead times associated with custom oscillators.

XO/VCXO FEATURES

- Wide frequency range: 100 kHz to 1.4 GHz
- Samples of any XO/VCXO available in 2 weeks
- Superior jitter performance: <0.3 ps rms
- Excellent frequency stability, superior initial accuracy and PSRR
- Single, dual, quad, I²C programmable options
- 100% Electrical testing = guaranteed startup
- LVPECL, LVDS, CML, HCSL, CMOS options
- 1.8, 2.5, and 3.3 V options
- 5 x 7 mm, 3.2 x 5 mm options
- -40 to 85 °C operation



VIDEO FORMAT CONVERTER

Crystal Oscillator (XO)

PART NUMBER	NUMBER OF FREQUENCIES	FREQUENCY RANGE	JITTER (ps RMS)	STABILITY/APR (PPM)	FORMAT	VOLTAGE (V)	TEMP (°C)	PACKAGE SIZE (MM)
Si535/36	Single	select freq. 100 - 312 5 MHz	0.2	±20, ±31.5	LVDS, LVPECL	3.3, 2.5	-40 to 85	5 x 7
Si530/31	Single	10 - 1417 MHz	0.3	±20, ±31.5, ±61.5	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7
Si532/33	Dual							
Si534	Quad							
Si570	Any (I²C Prog)							
Si590/91	Single	10 - 810 MHz	0.5	±20, ±30, ±50, ±100	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7
Si598	Any (I²C Prog)							
Si510/11	Single	0.1 - 250 MHz	0.8	±30, ±50, ±100	CMOS, Dual CMOS, LVPECL, LVDS, HCSL	3.3 2.5 1.8	-40 to 85	5 x 7 3.2 x 5
Si512/13	Dual							
Si514	Any (I²C Prog)							

Voltage-Controlled Oscillator (VCXO)

PART NUMBER	NUMBER OF CENTER FREQUENCIES	FREQUENCY RANGE	JITTER (ps RMS)	STABILITY/APR (PPM)	FORMAT	VOLTAGE (V)	TEMP (°C)	PACKAGE SIZE (MM)
Si550	Single	10 - 1417 MHz	0.5	±12 to ±375	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7
Si552	Dual							
Si554	Quad							
Si571	Any (I²C Prog)							
Si595	Single	10 - 810 MHz	0.7	±10 to ±370	CMOS, LVPECL, LVDS, CML	3.3 2.5 1.8	-40 to 85	5 x 7
Si596	Dual							
Si597	Quad							
Si599	Any (I²C Prog)							
Si515	Single	0.1 - 250 MHz	1.0	±30 to ±100	CMOS, Dual CMOS, LVPECL, LVDS, HCSL	3.3 2.5	-40 to 85	5 x 7 3.2 x 5
Si516	Dual							

Clock Buffers / Level Translators

WEB-CONFIGURABLE CUSTOM CLOCK BUFFERS AVAILABLE AT: www.silabs.com/clock-buffer

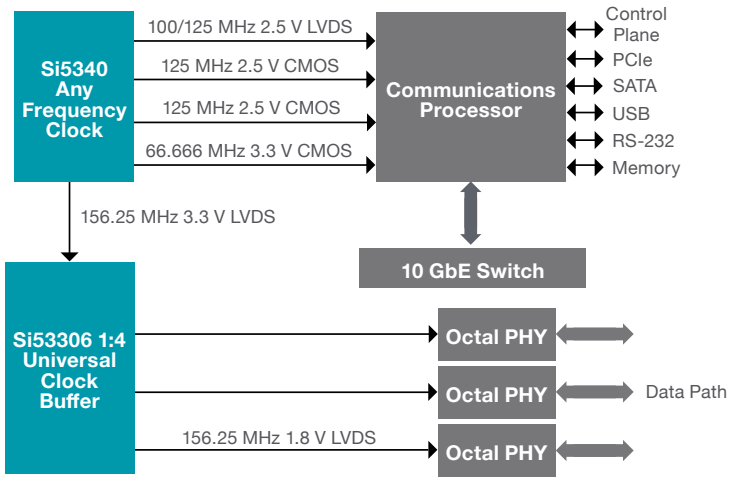
Universal / Any-format Clock Buffers / Level Translators

Silicon Labs' Universal family of low-jitter clock buffers and level translators (Si533XX) delivers multiple output clock formats from any input clock format (supports LVDS, LVPECL, CML, LVCMOS, SSTL, HCSL and HSTL). This flexibility reduces BOM complexity by allowing the same device to be used across multiple projects and platforms.

UNIVERSAL / ANY-FORMAT BUFFER

- Pin-selectable signal format (LVPECL, LVDS, CML, HCSL, LVCMOS)
- Wide operating frequency DC - 1.25 GHz
- 2-10 differential or 4-20 LVCMOS outputs
- Accepts any differential or single-ended input
- Low additive jitter: 45 fs rms (12 kHz - 20 MHz)
- Glitchless clock switching
- Synchronous output enable/Individual output enable
- Integrated voltage level translation
- Selectable drive strength to tailor jitter/EMI performance
- Optional output clock division: div-1, div-2, div-4
- Low output-output skew: <50 ps
- Excellent PSRR
- Independent VDD and VDDO: 1.8, 2.5 or 3.3 V

PART NUMBER	CLOCK INPUT/ OUTPUTS	ADDITIVE JITTER (RMS)	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
Si53306	1/4	45 fs	DC - 725	DC - 725	1.8, 2.5, 3.3	1.2, 1.8, 2.5, 3.3	LVPECL, LVDS, HCSL, LVCMOS, CML	QFN16
Si53307	2/2	45 fs	DC - 725	DC - 725	1.2, 2.5, 3.3	1.2, 1.8, 2.5, 3.3	LVPECL, LVDS, HCSL, LVCMOS, CML	QFN16
Si53301	2/6	45 fs	DC - 725	DC - 725	1.8, 2.5, 3.3	1.2, 1.8, 2.5, 3.3	LVPECL, LVDS, HCSL, LVCMOS, CML	QFN32
Si53302	2/10	45 fs	DC - 725	DC - 725	1.8, 2.5, 3.3	1.2, 1.8, 2.5, 3.3	LVPECL, LVDS, HCSL, LVCMOS, CML	QFN44
Si53320	2/10	45 fs	DC - 725	DC - 725	2.5, 3.3	2.5, 3.3	LVPECL	TSSOP20
Si53321	2/10	45 fs	DC - 1250	DC - 1250	2.5, 3.3	2.5, 3.3	LVPECL	QFN32, QFP32
Si53322	1/2	45 fs	DC - 1250	DC - 1250	2.5, 3.3	2.5, 3.3	LVPECL	QFN16
Si53323	2/4	45 fs	DC - 1250	DC - 1250	2.5, 3.3	2.5, 3.3	LVPECL	QFN16
Si53340	2/4	45 fs	DC - 1250	DC - 1250	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVDS	QFN16
Si53360	1/8	100 fs	DC - 200	1 - 200	1.8, 2.5, 3.3	1.8, 2.5	LVCMOS	TSSOP16
Si5330	1/4	150 fs	5 - 710	5 - 710	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVPECL, LVDS, HCSL, SSTL, HSTL	QFN24
SL18860DC	1/3	—	10 - 52	10 - 52	1.8, 2.5, 3.3	—	LVCMOS (TCXO)	TDFN10



10G ETHERNET SWITCH

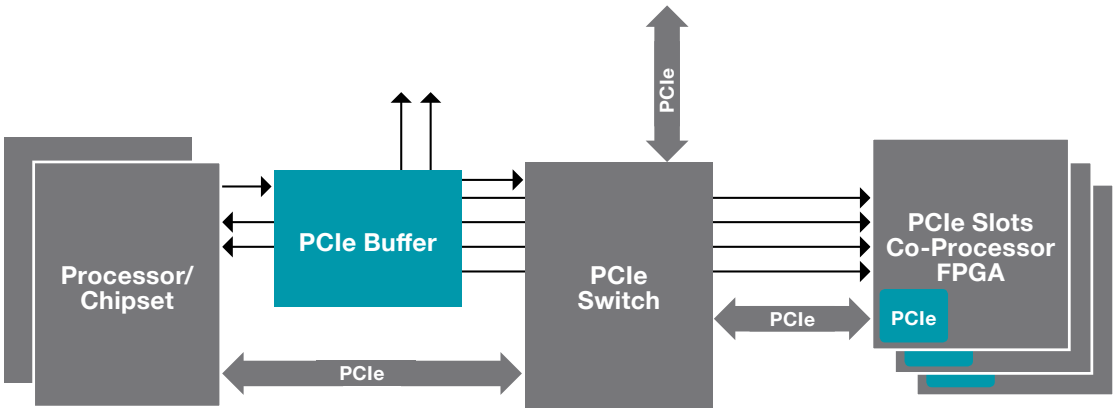
PCI Express (PCIe) Fanout / Zero Delay Buffers

Silicon Labs offers a portfolio of low-power fanout and zero delay buffers meeting PCI-Express Gen1/2/3 specifications. All devices feature low power push-pull output buffer technology, providing benefits of low power consumption, reduced external terminating resistors and small packaging. Devices in this family are ideal for server, storage and data center applications requiring a high number of PCI-Express clocks. The Si53108, Si53112 and Si53019 are fully qualified by Intel for DB800ZL, DB1200ZL and DB1900Z clock specifications respectively.

PCIE CLOCK BUFFER/ZERO DELAY BUFFER FEATURES

- Complete portfolio of PCI Express Gen 1/2/3 fanout/ zero-delay fanout
- Push-pull HCSL output fanout technology
- Integrated termination resistors
- Low power consumption
- I²C/SMBus programmable
- Supports optional LVPECL, LVDS, or CML levels
- -40 to 85 °C operation
- Individual output enable control
- Small form factor QFN packaging
- Intel Qualified

PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PHASE JITTER (RMS)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
Si53106	Pin/I²C	1 / 6	100, 133	100, 133	0.6 ps	—	—	Push-Pull HCSL	QFN40
Si53108	Pin/I²C	1 / 8	100, 133	100, 133	0.45 ps	—	—	Push-Pull HCSL	QFN48
Si53112	Pin/I²C	1 / 12	100, 133	100, 133	0.45 ps	—	—	Push-Pull HCSL	QFN64
Si53115	Pin/I²C	1 / 15	100, 133	100, 133	0.45 ps	—	—	Push-Pull HCSL	QFN64
Si53119	Pin/I²C	1 / 19	100, 133	100, 133	0.5 ps	—	—	Push-Pull HCSL	QFN72
Si53019	Pin/I²C	1 / 19	100, 133	100, 133	0.6 ps	—	—	Constant Current HCSL	QFN72
Si53102	—	1/2	100	100	0.2 ps	2.5, 3.3	—	Push-Pull HCSL	TDFN8
Si53152	Pin/I²C	1/2	100	100	0.1 ps	3.3	3.3	Push-Pull HCSL	QFN24
Si53154	Pin/I²C	1/4	100	100	0.1 ps	3.3	3.3	Push-Pull HCSL	QFN24
Si53156	Pin/I²C	1/6	100	100	0.1 ps	3.3	3.3	Push-Pull HCSL	QFN32
Si53159	Pin/I²C	1/9	100	100	0.1 ps	3.3	3.3	Push-Pull HCSL	QFN48



SERVER

Clock Generation

WEB-CONFIGURABLE FACTORY-CUSTOMIZED CLOCK GENERATORS AVAILABLE AT: www.silabs.com/custom-timing

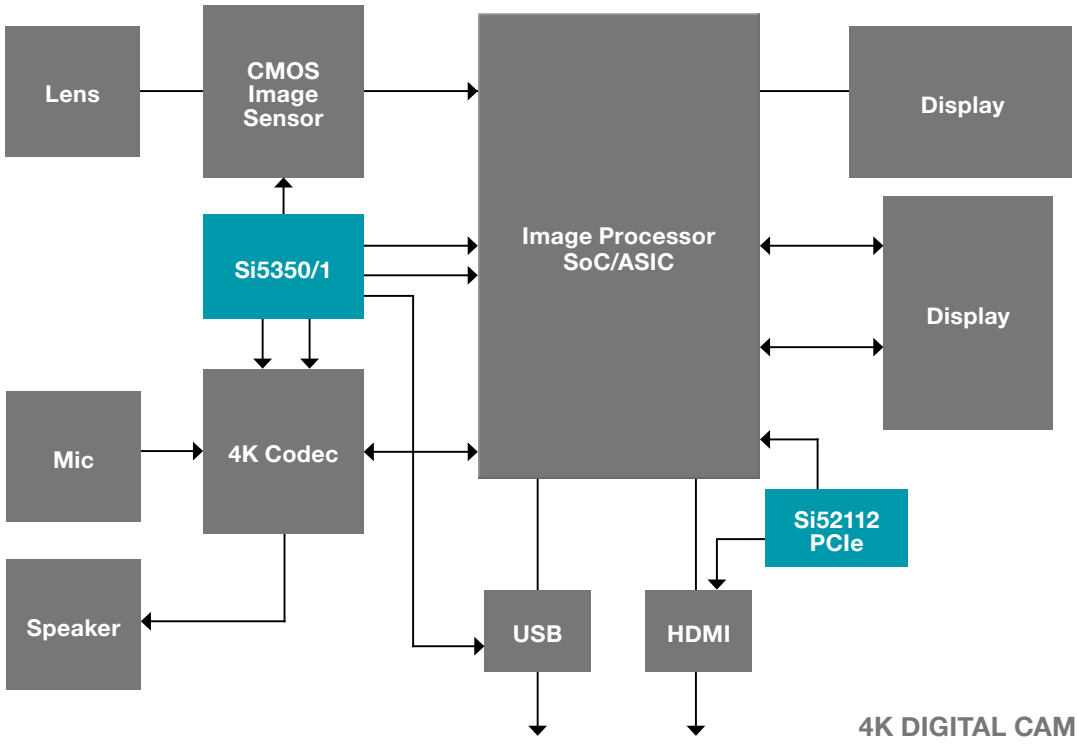
Any-Frequency, Any-Output CMOS Clock Generators (Si5350A/C, Si5351A/C)

Silicon Labs' highly flexible factory and I²C programmable LVCMOS clock generators can be customized to generate multiple, independent non-integer-related frequencies with equivalent frequency synthesis capability of 8 PLLs, with exact frequency synthesis (0 ppm error), significantly lower jitter, lower power and smaller size than competing solutions. Factory customization options are available to minimize EMI, including configurable edge rates, output impedance, output skew and spread spectrum. These flexible devices are perfect for low-cost consumer/embedded applications and can provide a complete clock tree on one chip.

Si5350A/C, Si5351A/C FEATURES

- Generates any frequency on any output, 2.5 kHz to 200 MHz
- Exact clock synthesis: 0 ppm error
- Similar frequency flexibility as 8 independent PLLs
- Crystal and/or clock input
- <70 ps pk-pk period jitter, typical
- Glitchless switching between output frequencies
- I²C programmable (Si5351) or pin-controlled (Si5350)
- Excellent PSRR: no discrete components
- Two-week sample lead time for any custom clock
- Spread spectrum clock generation -0.1 to -2.5% down, ±0.1 to ±1.5% center
- User-definable control pins Powerdown, Output Enable, Spread Enable, Frequency Select control pins
- Small form factor; MSOP10 (3 outputs), QFN20 (8 outputs)
- Now available in ClockBuilder Pro www.silabs.com/CBPro

PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PERIOD JITTER (PP)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
Si5350A	Pin	1/ 3 or 8	25/27 (Xtal)	2.5 kHz - 200 MHz	70 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVCMOS	MSOP10, QFN20
Si5350C	Pin	1/ 3 or 8	10 - 100 (Clock), 25/27 (Xtal)	2.5 kHz - 200 MHz	70 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVCMOS	MSOP10, QFN20
Si5351A	I²C	1/ 3 or 8	25/27 (Xtal)	2.5 kHz - 200 MHz	70 ps	2.5, 3.3	1.8, 2.5, 3.3	LVCMOS	MSOP10, QFN20
Si5351C	I²C	1/ 3 or 8	10 - 100 (Clock), 25/27 (Xtal)	2.5 kHz - 200 MHz	70 ps	2.5, 3.3	1.8, 2.5, 3.3	LVCMOS	MSOP10, QFN20



4K DIGITAL CAMERA

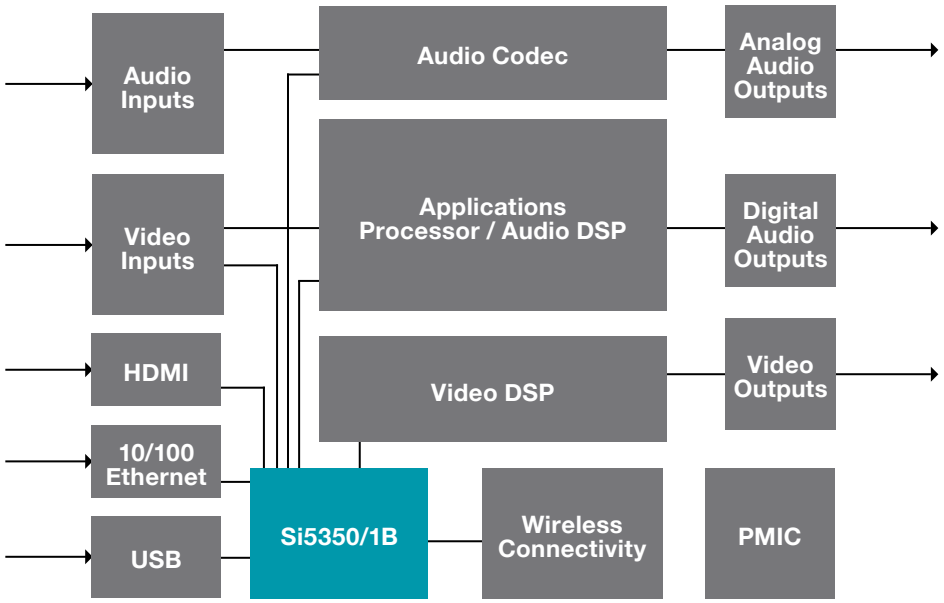
Any-Frequency CMOS Clock Generators with Integrated VCXOs (Si5350B, Si5351B)

These integrated clock generator + VCXO devices feature an integrated voltage controlled oscillator (VCXO), while eliminating the need for custom, pullable crystals. Free-running and VCXO clocks can be generated by one device, making them ideal for cost-sensitive consumer applications.

Si5350B, Si5351B FEATURES

- Generates any frequency on any output, 2.5 kHz to 200 MHz
- Exact clock synthesis: 0 ppm error
- Similar frequency flexibility as 8 independent PLLs
- Accepts crystal and analog control voltage input (VCXO)
- <70 ps pk-pk period jitter for any configuration
- Glitchless switching between output frequencies
- Integrated VCXO uses standard non-pullable crystal
- I²C programmable (Si5351) or pin-controlled (Si5350)
- Excellent PSRR: no discrete components
- Two week sample lead time for any custom clock
- Spread spectrum clock generation -0.5 to -2.5% down, ±0.1 to ±1.5% center
- User-definable control pins Powerdown, Output Enable, Spread Enable or Frequency Select control pins
- Small form factor; MSOP10 (3 outputs), QFN20 (8 outputs)
- Now available in ClockBuilder Pro www.silabs.com/CBPro

PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PERIOD JITTER (PP)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
Si5350B	Pin	1/ 3 or 8	25/27 (Xtal)VCXO	2.5 kHz - 200 MHz	70 ps	2.5, 3.3	1.8, 2.5, 3.3	LVCMOS	MSOP10, QFN20
Si5351B	I²C	1/8	25/27 (Xtal)VCXO	2.5 kHz - 200 MHz	70 ps	2.5, 3.3	1.8, 2.5, 3.3	LVCMOS	QFN20



AV RECEIVER

Any-Frequency, Any-Output Differential/CMOS Clock Generators (Si5340/41 and Si5335/38)

Silicon Labs' differential + LVCMOS clock generators provide any rate, any output frequency synthesis, enabling a single device to replace multiple crystal oscillator and fixed-frequency clock generators. Any combination of output frequencies can be generated exactly with 0 ppm error. Independent signal format and VDDO options provide integrated level translation, supporting LVPECL/LVDS/HCSL/LVCMOS clock generation up to 712.5 MHz with sub 1 ps rms phase jitter.

Si5340/41 FEATURES

- Up to 10 independent clock outputs
- MultiSynth technology delivers any frequency on any output up to 1028 MHz
- SPI or I2C programmable
- Any format, any output: LVPECL, LVDS, HCSL, LVCMOS, HSTL, SSTL and CML
- Clockbuilder Pro simplifies configuration
- Independent Output clock supply pins eliminate external level translator
- Low phase jitter: < 100 fs
- Si5341: 4-input, 10 output in 9x9mm 64-QFN (3.3, 2.5, 1.8 V)
- Si5340: 4-input, 4 output in 7x7mm 74-QFN

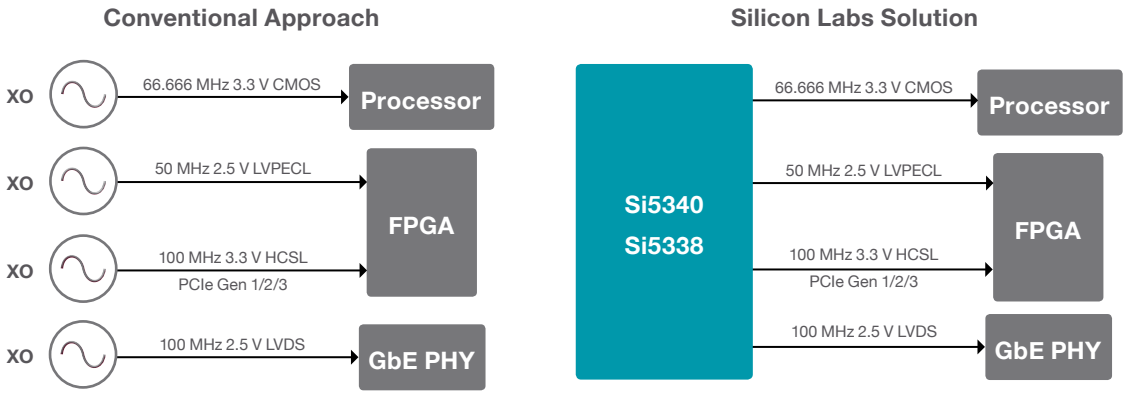
www.silabs.com/custom-timing
www.silabs.com/CBPro

Si5335/38 FEATURES

- Generates any frequency on any output, from 160 kHz to 350 MHz and select frequencies to 710 MHz
- Exact clock synthesis (0 ppm error)
- Crystal or clock input
- 4 differential outputs or 8 single-ended outputs
- Any format, any output: LVPECL, LVDS, HCSL, LVCMOS, HSTL, SSTL and CML
- Independent VDDO per output eliminates external level translators (1.5, 1.8, 2.5, 3.3 V)
- Low phase jitter: 1 ps rms
- I^2C programmable or pin-controlled
- Excellent PSRR, no discrete components
- Spread spectrum clock generation
- User-definable control pins: Powerdown, Output Enable, Frequency Select, Spread Select
- Factory-customizable clocks with two-week lead times

www.silabs.com/custom-timing

PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHZ)	OUTPUT FREQUENCY (MHZ)	PHASE JITTER (RMS)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
Si5340	I²C	1/4	10 - 750 (Clock), 25, 48-54 (Crystal)	100 Hz -1028	0.1 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN44
Si5341	I²C	1/10	10 - 750 (Clock), 25, 48-54 (Crystal)	100 Hz - 1028	0.1 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN64
Si5335	Pin	1/4	10 - 350 (Clock), 25/27 (Xtal)	1 - 350	1.0 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24
Si5338	I²C	1/4	5 - 710 (Clock), 8 - 30 (Xtal)	0.16 - 710 0.16 - 350 0.16 - 200	1.0 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24



CLOCK TREE SIMPLIFIED

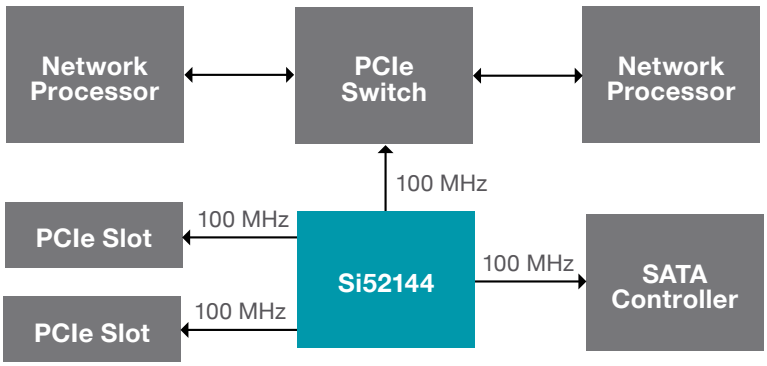
PCI Express Clock Generators (PCIe)

Silicon Labs offers the lowest power, highest performance PCI-Express clock generators on the market. All devices feature low-power push-pull output buffer technology, providing benefits of low power consumption, reduced external terminating resistors and smaller packaging. To optimize performance, the devices support programmable drive strength, rise/fall times and output impedance. Down spread spectrum clock generation is also supported. The devices support the standard PCIe HCSL signaling format and can be externally terminated to support LVPECL, LVDS or CML levels.

PCIe CLOCK GENERATOR FEATURES

- Complete portfolio of PCI Express Gen 1/2/3 clocks/buffers
- Push-pull HCSL output buffer technology
- Fully integrated termination resistors on PCIe outputs
- Low power consumption
- Programmable spread spectrum
- Pin strapping to enable spread spectrum
- I²C/SMBus programmable
- Supports optional LVPECL, LVDS, or CML levels
- -40 to 85 °C operation
- Individual output enable control
- Small form factor QFN and TDFN packaging

PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PHASE JITTER (RMS)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
Si52111	—	1/1	25	100	1.0 ps	3.3	3.3	HCSL	TDFN10
Si52112	—	1/2	25	100	1.0 ps	3.3	3.3	HCSL	TDFN10
Si52142	Pin/I²C	1/3	25	100, 25	1.0 ps	3.3	3.3	HSCL, LVCMOS	QFN24
Si52143	Pin/I²C	1/5	25	100, 25	1.0 ps	3.3	3.3	HSCL, LVCMOS	QFN24
Si52144	Pin/I²C	1/4	25	100	1.0 ps	3.3	3.3	HSCL	QFN24
Si52146	Pin/I²C	1/6	25	100	1.0 ps	3.3	3.3	HSCL	QFN32
Si52147	Pin/I²C	1/9	25	100	1.0 ps	3.3	3.3	HSCL	QFN48
Si5335	Pin	1/4	10 - 350 (Clock), 25/27 (Xtal)	1 - 350	1.0 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24
Si5338	I²C	1/4	5 - 710 (Clock), 8 - 30 (Xtal)	0.16 - 710	1.0 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVPECL, LVDS, LVCMOS, HCSL, SSTL, HSTL	QFN24



IP GATEWAY

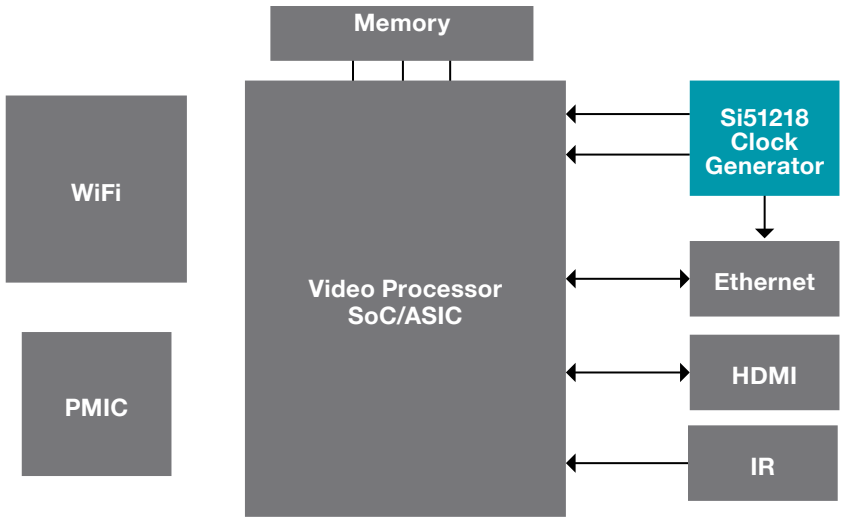
Tiny IoT Clock Generators

Silicon Labs' highly flexible, factory programmable tiny clock LVCMOS generators can be customized to generate multiple frequencies with significantly lower jitter, lower power and smaller size than competing solutions, making them an ideal fit for Internet of Things (IoT) applications. Customization options are available for frequency selection, output enable control or minimizing EMI, including customizable spread percentage, modulation rate, output impedance and rise time/fall time. The Tiny Clock family is now available in ClockBuilder Pro, enabling quick and easy program file development and part number creation.

Si512xx TINY IoT CLOCK GENERATOR FEATURES

- Up to three customizable output frequencies: 3 to 200 MHz
- Accepts 8 to 48 MHz crystal or 3 to 166 MHz reference clock
- Low cycle-to-cycle jitter: <150 ps
- Low power: 2.3 mA (typ) at 48 MHz output, 25 MHz xtal, VDD = 3.3 V
- Center spread modulation from 0.25 to 1.0%, (0.125% resolution)
- 4 custom drive strength options for each output
- Customizable control pins (PD#/OE/SSON#/FS)
- Independent VDD and VDDO — 1.8, 2.5; 3.3 V
- Ultra-compact packages
  - 6-pin TDFN (1.2 mm x 1.4 mm x 0.75 mm)
  - 8-pin TDFN (1.6 mm x 1.4 mm x 0.75 mm)
- Two week sample lead time
- Now available in ClockBuilder Pro www.silabs.com/CBPro

PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PERIOD JITTER (PP)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
Si51210	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 200	—	2.5 to 3.3	—	LVCMOS	TDFN6
Si51211	Pin	1/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 200	—	2.5 to 3.3	1.8, 2.5, 3.3	LVCMOS	TDFN8
Si51214	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 133	—	1.8	—	LVCMOS	TDFN6
Si51218	Pin	1/3	3 - 166 (Clock), 8 - 48 (xtal)	32 kHz to 200 MHz	—	2.5 to 3.3	1.8, 2.5, 3.3	LVCMOS	TDFN8
Si51219	Pin	1/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 to 200	—	2.5 to 3.3	1.8, 2.5, 3.3	LVCMOS	TSSOP8



GATEWAY/IP-STB

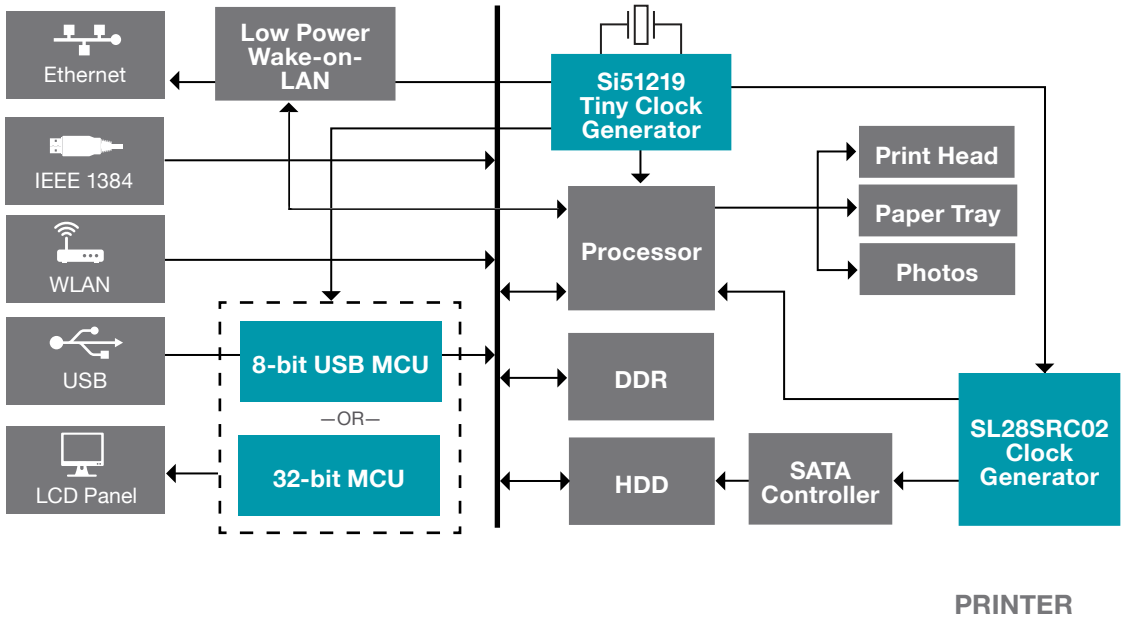
EMI Reduction Clock Generators

Silicon Labs' programmable spread spectrum clock generators feature a wide range of programming options, allowing system designers to minimize EMI at the application level. Configurable parameters include spread spectrum percentage/modulation rate, programmable edge rates, programmable output impedance and programmable skew.

EMI REDUCTION CLOCK GENERATOR FEATURES

- Output frequencies from 1 to 350 MHz
- CLKOUT, REFCLK or SSCLK output options
- CLKIN or XO input options
- 8 to 48 MHz crystal input range
- 1 to 166 MHz clock input range
- Spread percent from 0 to 5.0%
- Down or center spread options
- Spread modulation frequency from 16 to 128 kHz
- On-chip load caps 8 to 20 pF
- User-definable control pins Powerdown, Output Enable, Spread Enable, Frequency Select, Spread Select control pins
- 7 programmable tr/tf options
- Industry's smallest SSCG: 1.2 mm x 1.4 mm

PART NUMBER	CONTROL	CLOCK INPUT/ OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	PHASE JITTER (RMS)	VDD (V)	VDDO (V)	OUTPUT	PACKAGE
SL16020DC	Pin/I²C	1/2	27 (Xtal)	27, 100	—	3.3	—	LVCMOS	TDFN10
Si5335	Pin	1/4	10 - 350 (Clock), 25/27 (Xtal)	1 - 350	1.0 ps	1.8, 2.5, 3.3	1.8, 2.5, 3.3	LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML	QFN24
Si51210	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200	—	2.5 - 3.3	—	LVCMOS	TDFN6
Si51211	Pin	1/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200	—	2.5 - 3.3	1.8, 2.5, 3.3	LVCMOS	TDFN8
Si51214	Pin	1/2	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 133	—	1.8	—	LVCMOS	TDFN6
Si51219	Pin	1/3	3 - 166 (Clock), 8 - 48 (Xtal)	3 - 200	—	2.5 - 3.3	1.8, 2.5, 3.3	LVCMOS	TSSOP8
Si52142	Pin/I²C	1/3	25	100, 25	1.0 ps	3.3	3.3	HSCL, LVCMOS	QFN24
Si52143	Pin/I²C	1/5	25	100, 25	1.0 ps	3.3	3.3	HSCL, LVCMOS	QFN24
Si52144	Pin/I²C	1/4	25	100	1.0 ps	3.3	3.3	HSCL	QFN24
Si52146	Pin/I²C	1/6	25	100	1.0 ps	3.3	3.3	HSCL	QFN32
Si52147	Pin/I²C	1/9	25	100	1.0 ps	3.3	3.3	HSCL	QFN48



Jitter Attenuators

REQUEST SAMPLES AND DOWNLOAD DOCUMENTATION AT: www.silabs.com/clocks

Single / Multi-DSPLL Jitter Attenuators

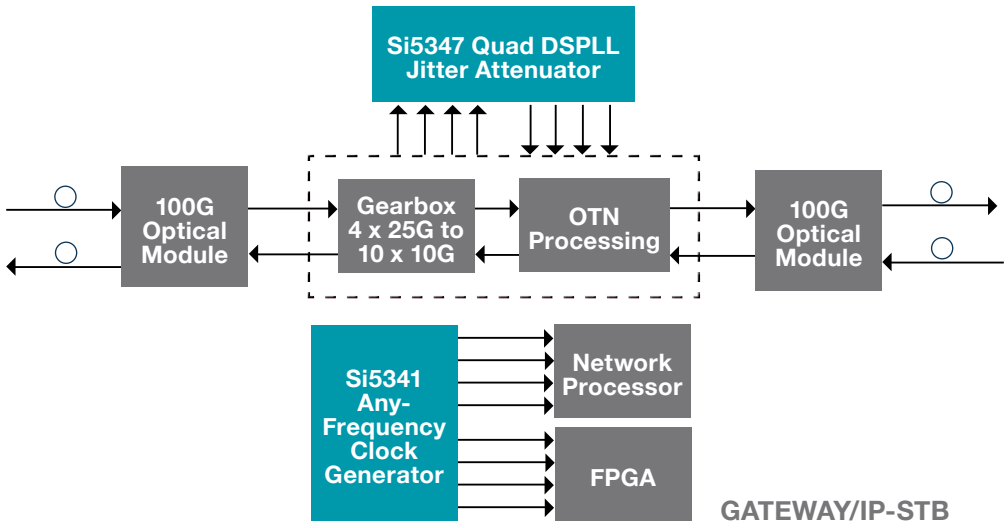
Silicon Labs' jitter attenuators generate any combination of output frequencies from any input frequency with industry-leading jitter performance (100 fs RMS). Based on Silicon Labs' innovative 4th-generation DSPLL architecture, these devices simplify clock tree design by replacing multiple clocks and oscillators, thereby minimizing BOM count and complexity.

JITTER ATTENUATOR FEATURES

- Generates any frequency on any output
- Ultra-low jitter: 100 fs RMS (12 kHz - 20 MHz)
- Integrated loop filter with selectable loop bandwidth
- Hitless switching with phase buildout (auto/manual)
- Synchronous, freerun and holdover modes
- Best-in-class PSRR
- Dynamically reconfigurable output frequency (per output)
- Fast-lock: <100 ms
- Serially programmable via I²C/SPI
- Any format, any output: LVPECL, CML, LVDS, HCSL, LVCMOS
- Independent VDDO
- In-circuit programmable
- Easy-to-use ClockBuilder Pro* configuration software

*see page 19 for more about ClockBuilder Pro

PART NUMBER	# OF PLLS	CONTROL	CLOCK INPUTS / OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	JITTER (PS)	PLL BANDWIDTH	HITLESS SWITCHING	DIGITAL HOLD	SIGNAL FORMAT	PACKAGE
Si5317	1	I²C/SPI	1/1	0.002 - 710	0.002 - 710	0.3	60 Hz - 8 kHz			LVPECL, LVDS, CML, LVCMOS	QFN36
Si5319	1	I²C/SPI	1/1	0.002 - 710	0.002 - 1417	0.3	60 Hz - 8 kHz	√		LVPECL, LVDS, CML, LVCMOS	QFN36
Si5326	1	I²C/SPI	2/2	0.002 - 710	0.002 - 1417	0.3	60 Hz - 8 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN36
Si5342	1	I²C/SPI	4/2	0.002 - 710	0.001 - 1028	0.1	0.1 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN44
Si5342H	1	I²C/SPI	2/2	0.008 - 750	0.001 - 2750	0.1	0.1 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN44
Si5344	1	I²C/SPI	4/4	0.008 - 750	0.001 - 1028	0.1	0.1 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN64
Si5344H	1	I²C/SPI	2/4	0.008 - 750	0.001 - 2750	0.1	0.1 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN44
Si5345	1	I²C/SPI	4/10	0.008 - 750	0.001 - 1028	0.1	0.1 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN64
Si5346	2	I²C/SPI	4/4	0.008 - 750	0.001 - 718.5	0.1	0.1 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN44
Si5347	4	I²C/SPI	4/8 or 4	0.008 - 750	0.001 - 718.5	0.1	60 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN64
Si5375	4	I²C	4/4	0.002 - 710	0.002 - 808	0.4	60 Hz - 8 kHz		√	LVPECL, LVDS, CML, LVCMOS, HCSL	BGA80

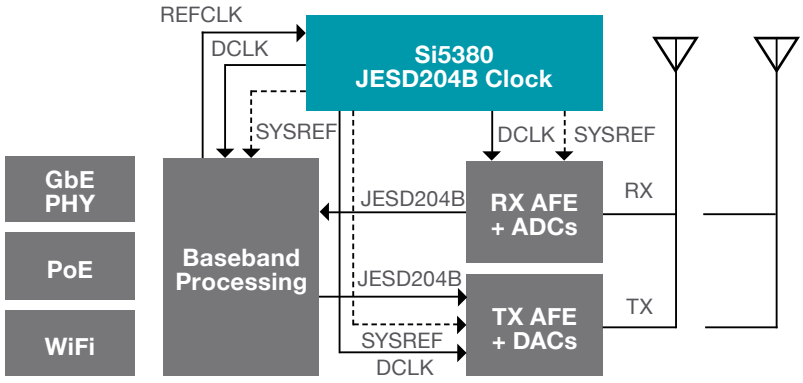


4G/LTE JESD204B-Compliant Jitter Attenuating Clock Multipliers

REQUEST SAMPLES AND DOWNLOAD DOCUMENTATION AT: www.silabs.com/clocks

The Si5380 wireless clock generator leverages Silicon Labs' latest 4th-generation DSPLL technology to address the stringent form factor, power and performance requirements demanded by small cell and remote radio head (RRH) applications. The Si5380 is the industry's first wireless clock generator capable of replacing discrete high-performance VCXO-based clocks with a fully integrated CMOS IC solution. The resulting solution is optimized for small form factor base station designs in terms of integration, size and power while delivering unparalleled performance and ease of use.

PART NUMBER	# OF PLLS	CONTROL	CLOCK INPUTS / OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	JITTER (PS)	PLL BANDWIDTH	HITLESS SWITCHING	DIGITAL HOLD	SIGNAL FORMAT	PACKAGE
Si5380	1	I²C/SPI	4/12	10 - 750	0.480 - 1474	0.07	0.1 Hz - 100 Hz	√	√	LVDS, LVPECL, CML, HCSL, LVCMOS	QFN64



4G/LTE SMALL CELL

Network Synchronizers

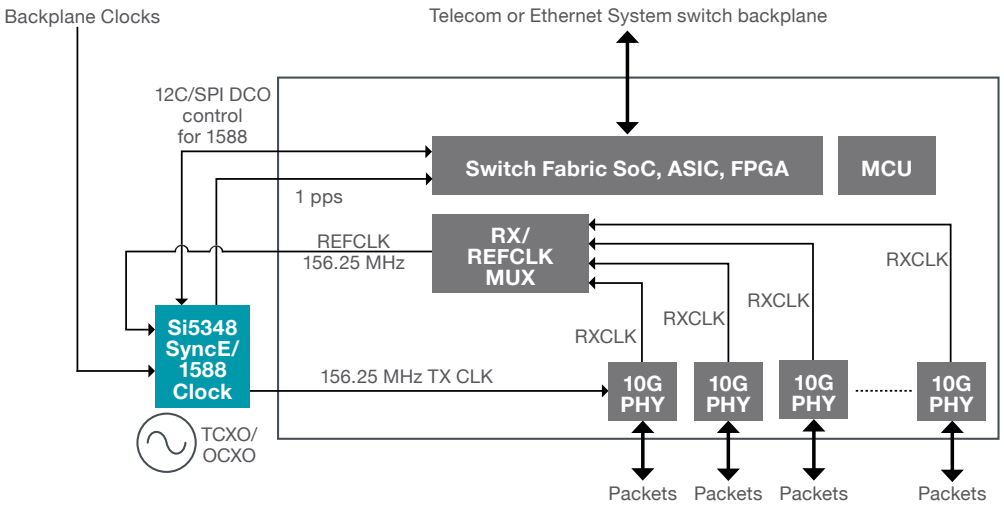
REQUEST SAMPLES AND DOWNLOAD DOCUMENTATION AT: www.silabs.com/clocks

Silicon Labs Synchronous Ethernet (SyncE) jitter attenuating clock synthesizers provide full compliance with SyncE specifications (ITU G.8262 EEC Options 1 & 2) while providing any-frequency synthesis, jitter cleaning and wander filtering down to 0.1 Hz. The Si534x are the industry's lowest jitter SyncE clocks, making them ideal for clocking Ethernet PHYs from GbE to 100 GbE.

SYNCE CLOCK FEATURES

- Fully compliant with SyncE (ITU-T G.8262) clock requirements
- Generates all SyncE rates (25, 125, 156.25 MHz) from any input frequency, as well as 1 PPS
- Integrated loop filter w/ selectable loop bandwidth: 0.1 Hz to 4 kHz
- Up to three high-performance DCOs with 1ppt step resolution
- < 0.1 ps RMS jitter
- In-circuit programmable
- Serially programmable via I²C/SPI
- Ideal for Ethernet PHYs from GbE to 100 GbE

PART NUMBER	# OF PLLS	CONTROL	CLOCK INPUTS / OUTPUTS	INPUT FREQUENCY (MHz)	OUTPUT FREQUENCY (MHz)	JITTER (PS)	PLL BANDWIDTH	HITLESS SWITCHING	DIGITAL HOLDOVER	SIGNAL FORMAT	PACKAGE
Si5315	1	Pin	2/2	0.008 - 644	0.008 - 644	0.23	60 Hz - 8.4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS	QFN36
Si5328	1	I²C/SPI	2/2	0.008 - 710	0.008 - 808	0.3	0.1 Hz - 10 Hz	√	-	LVPECL, LVDS, CML, LVCMOS	QFN36
Si5348	3	I²C/SPI	5/7	0.008 - 750	1PPS, 0.0001 - 718.5	0.1	0.1 Hz - 4 kHz	√	√	LVPECL, LVDS, CML, LVCMOS, HCSL	QFN64



10G SYNCE/IEEE 1588 ETHERNET SWITCH

Silicon Labs Can Help With Every Stage of the Design Process

ACCESS ALL THESE TOOLS ON OUR WEBSITE AT www.silabs.com/timing-tools

Discover

Parametric Search Online and iPad App

Quickly jump between clock and oscillator product families. Filter results using common technical and application requirements. Access data sheets and other documentation directly in the app. Browse product information – features, applications, block diagrams and order samples and development kits, from the app.
www.silabs.com/parametric-search

Available on the App Store

Phase Noise to Jitter Calculator

Need to quickly determine the jitter requirements for a clock? This tool converts phase noise to phase jitter, period jitter and cycle-to-cycle jitter. The resulting jitter values can be used to easily identify clocks and oscillators that meet the requirement.
www.silabs.com/jitter-calculator

Look Up or Customize an Oscillator, Clock or Buffer

Generate new part numbers and look up existing part numbers/device specifications.
www.silabs.com/custom-timing

Custom Clock Trees

Clock Tree Expert is a web-based application that generates a clock tree bill-of-material based on your requirements. Simply enter a list of your clocking requirements and Clock Tree Expert will guide you to a complete timing solution in minutes.
https://design.silabs.com/

Customize and Evaluate

ClockBuilder Pro Software

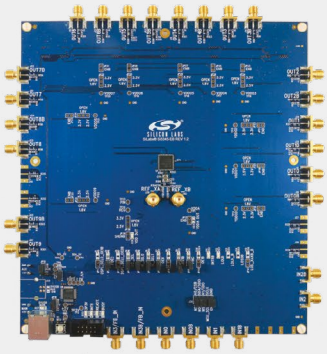
Use ClockBuilder Pro for Si534x and Si538x device configuration, evaluation and generating custom part numbers. ClockBuilder Go is a mobile app that can be used to verify the device settings for a given set of input/output frequencies. ClockBuilder Go provides a great way to jump-start the device configuration process. ClockBuilder Go provides an output file that can be used by ClockBuilder Pro to finish the configuration process.

www.silabs.com/CBPro

SOFTWARE	SUPPORTED DEVICES
ClockBuilder Pro	Si5121x, Si5350/1, Si5340/1/2/4/5/6/7/8, Si5380
ClockBuilder Go App for iOS	Si5340/1/2/4/5/6/7
ClockBuilder Desktop Software	Si5338/56
ClockBuilder Web Utility	Si5335/55
DSPLLsim	Si531x/2x/6x/7x
PCIe Clock Jitter Tool	Si5335/8, Si534x, Si5214x, Si5211x, Si5315x, Si531xx, Si53019
Oscillator Phase Noise Look-up Tool	Si51x, Si53x, Si59x, Si570

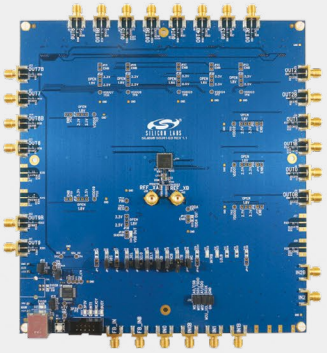
Develop

ACCESS ALL THESE TOOLS ON OUR WEBSITE AT www.silabs.com/timing-devkits

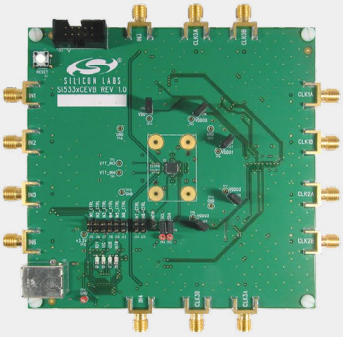


Si5345 1-PLL JITTER ATTENUATING CLOCK EVALUATION BOARD

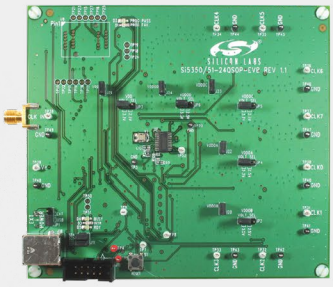
Si5347 MULTI-PLL JITTER ATTENUATING EVALUATION BOARD



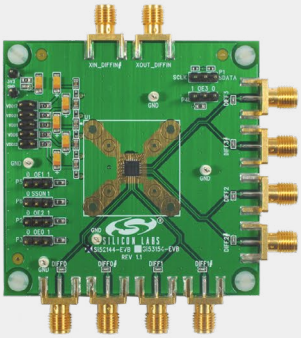
Si5341 CLOCK GENERATOR EVALUATION BOARD



Si5338 CLOCK GENERATOR EVALUATION BOARD

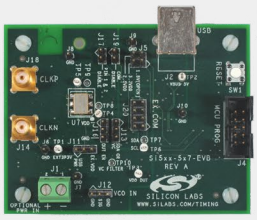


Si5350 CLOCK GENERATOR EVALUATION BOARD



Si52144 PCI EXPRESS BUFFER EVALUATION BOARD

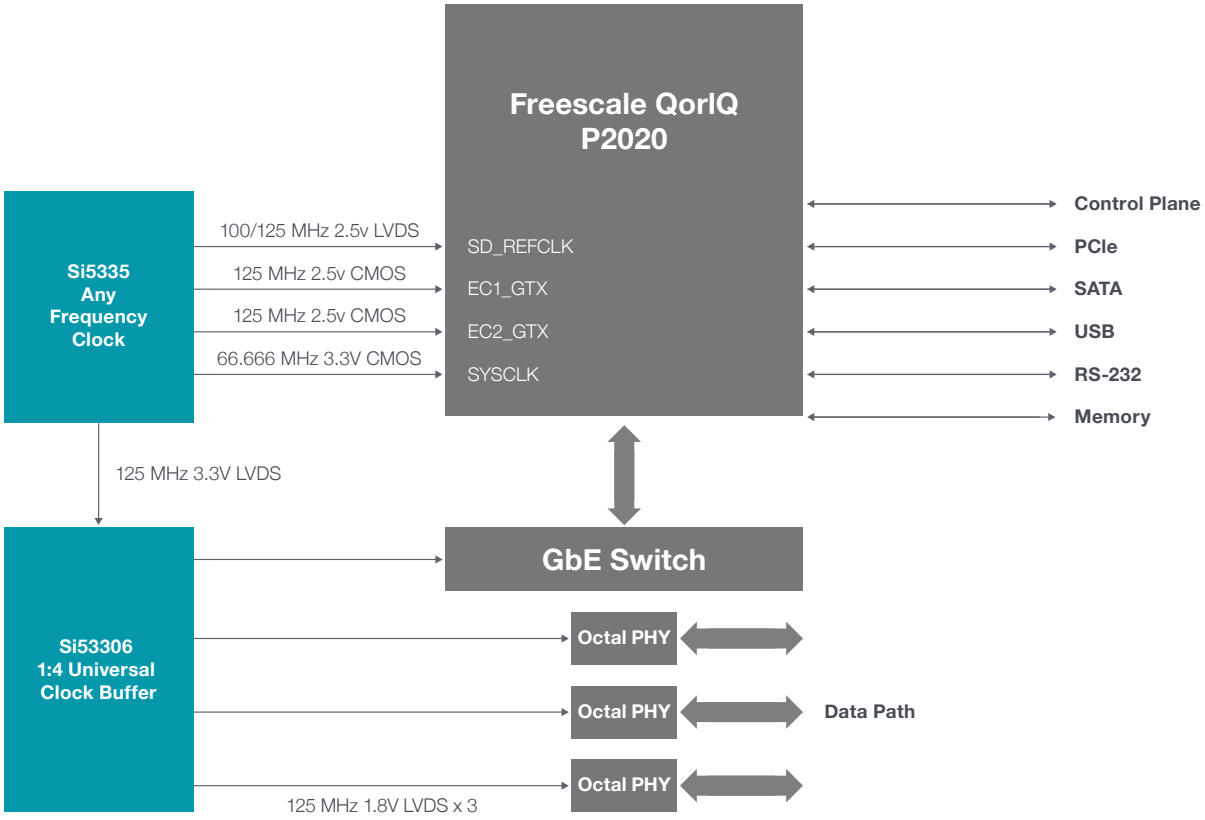
CLOCKBUILDER PRO™ FIELD PROGRAMMER KIT



Si570 I²C OSCILLATOR EVALUATION BOARD

Timing Solutions for Freescale QorIQ

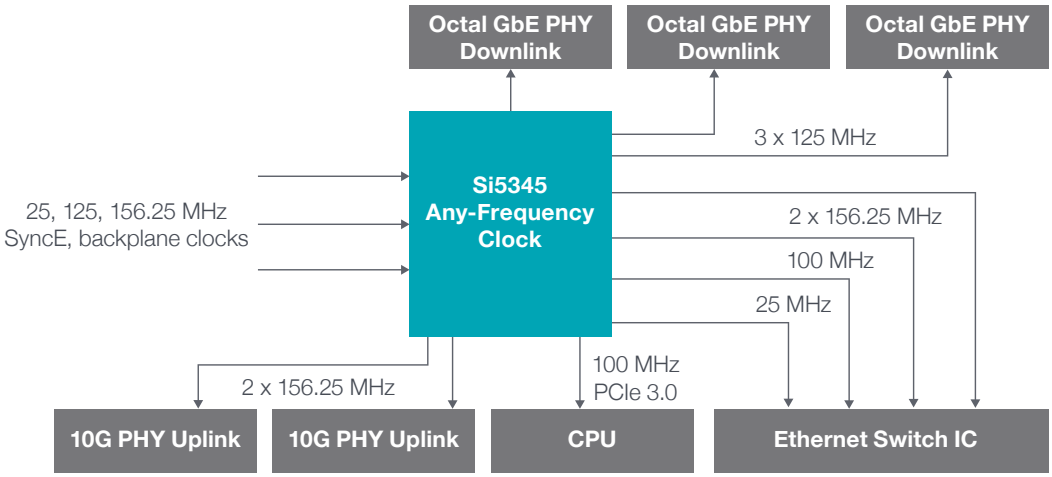
Silicon Labs frequency flexible timing products provide clock-tree-on-a-chip functionality, simplifying interfacing with Freescale PowerQUICC, QorIQ and LayerScape communications processors.



APPLICATION	FREESCALE QorIQ	SILICON LABS TIMING SOLUTIONS
Service Provider • Base stations • Routers, switches	P20xx, P40xx, B4xxx	• Si5345/44/42 Jitter Attenuators • Si5341/40/38/35 Any-Frequency Clock Generators • Si5xx XOs, Si5330x Universal Clock Buffers
Enterprise/Data Center • Routers, switches, WLAN • NAS, security routers • Application delivery controller	P10xx, T10xx, P20xx, T20xx, QorIQ LS1, QorIQ LS2	• Si521xx/Si531xx PCIe Clocks/Buffers • Si5341/40/38/35 Any-Frequency Clock Generators • Si5xx XOs, Si5330x Universal Clock Buffers
Industrial • Single-board computers • Industrial switches, routers • Medical imaging	P10xx, T10xx, P20xx, T20xx	• Si521xx/Si531xx PCIe Clocks/Buffers • Si5335/38 Any-Frequency Clock Generators • Si5xx XOs, Si5330x Universal Clock Buffers

Timing Solutions for Broadcom

The Si5345/44/42 fully support ITU-T G.8262 Synchronous Ethernet clock requirements and meet the stringent jitter requirements of Broadcom switches/PHYs for GbE, 10 GbE, 40 GbE and 100 GbE applications. No additional jitter clean-up PLLs are necessary to achieve these requirements. With industry-leading jitter performance, the Si5345/44/42 are ideal solutions for BCM56xxx, BCM88xxx and BCM53xxx.



	APPLICATION	BROADCOM PRODUCT FAMILY	SILICON LABS TIMING SOLUTIONS		
			SILICON LABS XO	SILICON LABS CLK BUFFER	SILICON LABS CLK GEN
BROADBAND ACCESS	Set-Top Boxes	BCM33xx BCM7xxx	Si500	Si531xx Si5330	Si5121x Si521xx
	DSL/G.fast/PON CPE	BCM63xx BCM63xxx BCM68xx	Si51x	Si531xx Si5330	Si5121x Si521xx
	DSL CO	BCM65xx BCM65xxx	Si51x Si57x	Si5330x	Si533x Si534x
	xPON OLT	BCM68xxxx BCM5553x	Si51x	Si5330x	Si533x Si534x
	CMTS	BCM3xxx	Si51x	Si5330x	Si533x Si534x
ENTERPRISE + NETWORK PROCESSORS	Knowledge-Based Processors	NLxxxx NLSxxx BCM12xxxx	Si51x	Si5330x	Si533x
WIRELESS INFRASTRUCTURE	Small Cells	BCM616xx	Si51x	Si5330x	Si521xx Si534x Si538x
	DFE Processors	BCM510xx	Si53x	Si5330x	Si534x Si538x
	Microwave/ Mobile Backhaul	BCM85xxx	Si53x	Si5330x	Si534x Si538x
ETHERNET COMMUNICATION + SWITCHING	GbE/FE PHY	BCM54xxx	Si51x	Si5330x	Si533x Si534x
	GbE/FE Switch	BCM53xxx	Si51x	Si5330x	Si533x
	10/40GbE PHY	BCM8xxx BCM84xxx	Si53x	Si5330x	Si534x
	10/40/100GbE Switch	BCM56xxx	Si53x	Si5330x	Si534x

Timing Solutions for Altera and Xilinx

	PROTOCOL	ALTERA STRATIX	ALTERA ARRIA	ALTERA CYCLONE	XILINX 7 SERIES	XILINX ULTRASCALE	SILICON LABS TIMING SOLUTIONS		
							SILICON LABS XOS	SILICON LABS CLK BUFFER	SILICON LABS CLK GEN
GENERAL PURPOSE	PCI Express	√	√	√	√	√	Si51x	Si5315x	Si5214x
	QPI	√	-	-	√	√	Si51x	Si5330x	Si533x
	Fibre Channel	√	√	-	√	√	Si51x	Si5330x	Si533x
	SAS/SATA	√	√	√	√	√	Si51x	Si5315x	Si533x
WIRED COMM.	Gigabit Ethernet	√	√	√	√	√	Si51x	Si5330x	Si533x
	10G Ethernet	√	-	-	√	√	Si53x	Si5330x	Si534x
	40G Ethernet	√	-	-	√	√	Si53x	Si5330x	Si534x
	100G Ethernet	√	-	-	√	√	Si53x	Si5330x	Si534x
	OTN	√	-	-	√	√	Si53x	Si5330x	Si534x
	SONET	√	√	√	√	√	Si53x	Si5330x	Si534x
	SFI	√	√	-	√	√	Si53x	Si5330x	Si534x
	Interlaken	√	√	-	√	√	Si53x	Si5330x	Si534x
	CEI	√	√	-	√	√	Si53x	Si5330x	Si534x
	PON	√	√	-	√	√	Si51x	Si5330x	Si533x
WIRELESS	CPRI	√	√	√	√	√	Si53x	Si5330x	Si534x
	SRIO	√	√	√	√	√	Si51x	Si5330x	Si534x
	JESD204B	√	√	-	√	√	Si53x	Si5330x	Si538x
AUDIO & VIDEO	3G-SDI	√	√	√	√	√	Si51x	Si5330x	Si534x
	Display Port	-	√	√	-	-	Si51x	Si5330x	Si535x

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