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Low - Jitter Clock Generator with Integrated VCO

-Preliminary- **AK8185A**

- Features -

- Low Phase Noise PLL
  RMS jitter 0.4ps typ. (12kHz to 20MHz)
- On chip VCO
- 4x Output Available
  Pin-Selectable
  LVPECL, LVDS, or 2-LVCMOS
- LVCMOS Bypass Output Available
- 3.3V for Core
- Operating Temperature Range: -40 to +85℃
- Pin Package: 5mm x 5mm
  32-pin Leadless QFN (Pb-free)

- Description -

- AK8185A is a Low – Jitter Clock Generator with sub pico-second jitter performance.
- Also Low power consumption is the advantage for advanced optimized application.

- Application -

- Ethernet
- SONET
- Fibre Channel
- SAN
- Cost-Effective High-Frequency Crystal Oscillator Replacement

- Block Diagram -

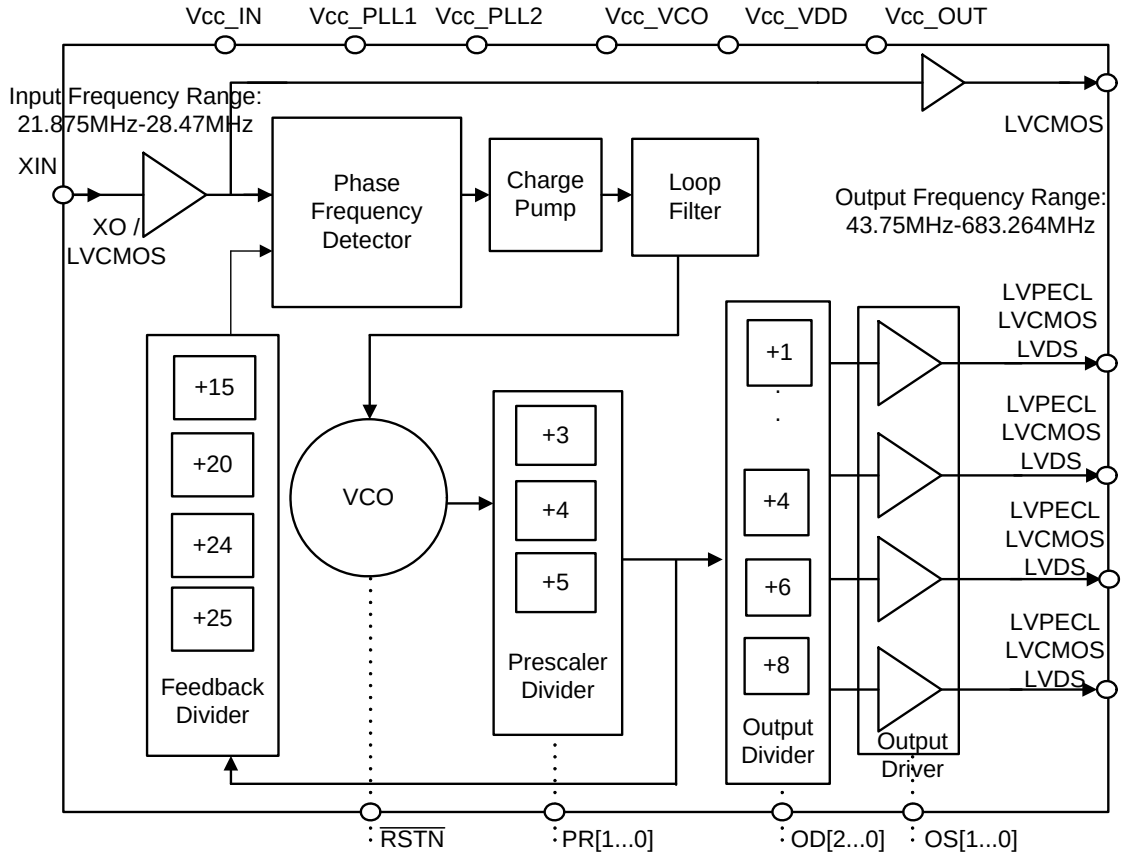


Fig. 1

- Pin Assignments -

(Top view)

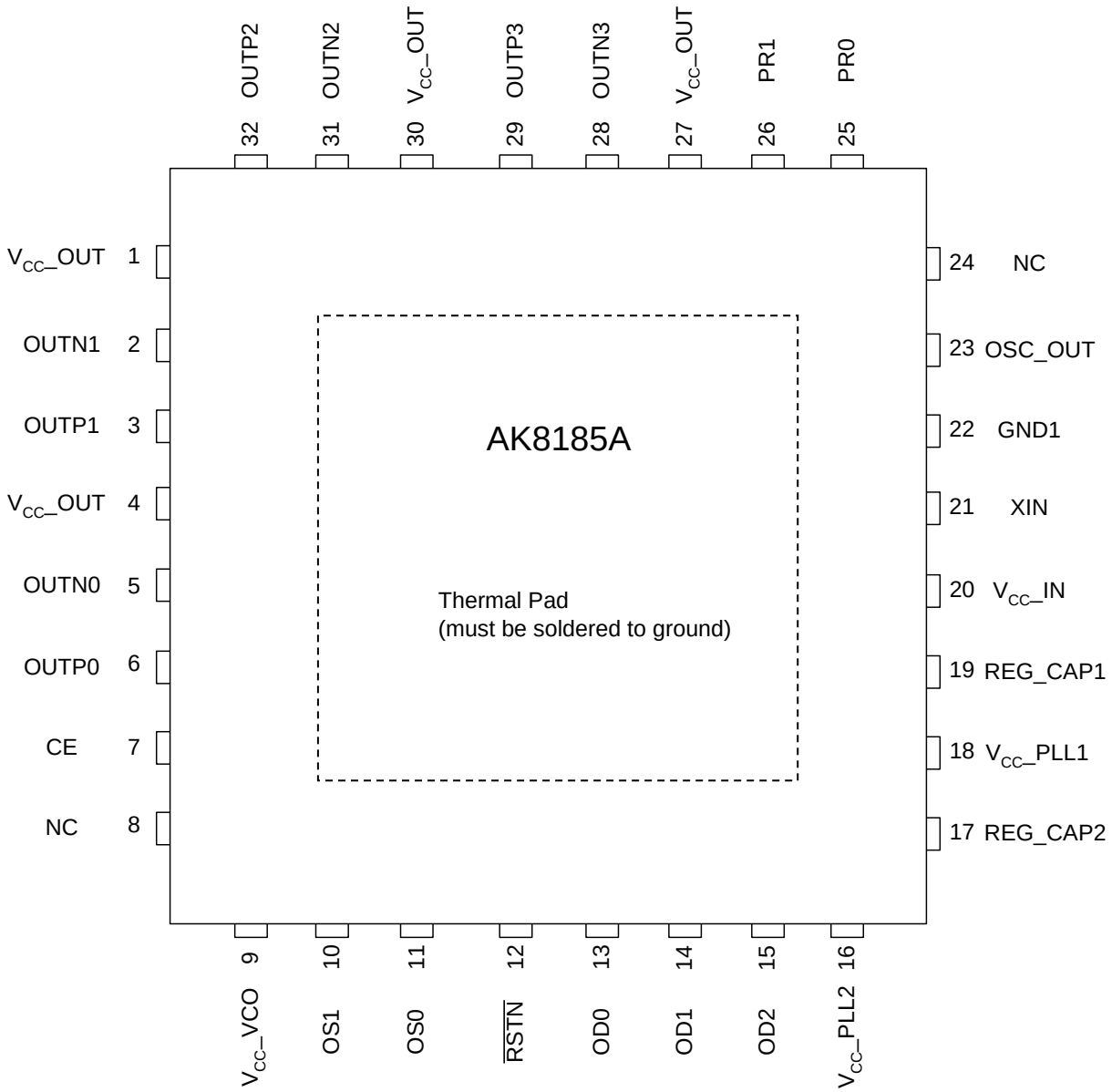


Fig. 2

- Pin Descriptions -

Pin No.	Pin Name	Pin Type	Description
1	V_{CC}_OUT	PWR	3.3V Power Supply for output buffers
2	OUTN1	OUT	Differential output pair or two single-ended outputs
3	OUTP1	OUT	Differential output pair or two single-ended outputs
4	V_{CC}_OUT	PWR	3.3V Power Supply for output buffers
5	OUTN0	OUT	Differential output pair or two single-ended outputs
6	OUTP0	OUT	Differential output pair or two single-ended outputs
7	CE	IN	Chip enable control pin
8	NC		No Connection
9	V_{CC}_VCO	PWR	3.3V Power Supply for internal VCO
10	OS1	IN	Output type select control pin
11	OS0	IN	Output type select control pin
12	RSTN	IN	Device reset (active low)
13	OD0	IN	Output divider control pins
14	OD1	IN	Output divider control pins
15	OD2	IN	Output divider control pins
16	V_{CC}_PLL2	PWR	3.3V Power Supply for PLL circuitry
17	REG_CAP2	OUT	Capacitor for internal regulator (connect to a 10-μF Y5V capacitor to GND)
18	V_{CC}_PLL1	PWR	3.3V Power Supply for PLL circuitry
19	REG_CAP1	OUT	Capacitor for internal regulator (connect to a 10-μF Y5V capacitor to GND)
20	V_{CC}_IN	PWR	3.3V Power Supply for input buffers
21	XIN	IN	Parallel resonant crystal or LVCMOS inputs
22	GND1	Ground	Additional ground for device
23	OSC_OUT	OUT	Bypass LVCMOS output
24	NC		No Connection
25	PR0	IN	Prescaler and Feedback divider control pins
26	PR1	IN	Prescaler and Feedback divider control pins
27	V_{CC}_OUT	PWR	3.3V Power Supply for output buffers
28	OUTN3	OUT	Differential output pair or two single-ended outputs
29	OUTP3	OUT	Differential output pair or two single-ended outputs
30	V_{CC}_OUT	PWR	3.3V Power Supply for output buffers
31	OUTN2	OUT	Differential output pair or two single-ended outputs
32	OUTP2	OUT	Differential output pair or two single-ended outputs
EPAD	GND	Ground	Thermal Pad (Must be soldered to Ground)

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Parameter	Value	Unit
Supply voltage range (Vcc_out, Vcc_{PLL1} ,Vcc_{PLL2}, Vcc_{VCO} , Vcc_{IN})	-0.3 to 4.3V	V
Input voltage range	GND-0.3 to V_{CC}+0.3	V
Input current range	-10 to +10	mA
Storage temperature	-55to 125	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Output supply voltage	Vcc_out	3.0	3.3	3.6	V
PLL supply voltage	Vcc_{PLL1}	3.0	3.3	3.6	V
PLL supply voltage	Vcc_{PLL2}	3.0	3.3	3.6	V
On-chip VCO supply voltage	Vcc_{VCO}	3.0	3.3	3.6	V
Input supply voltage	Vcc_{IN}	3.0	3.3	3.6	V
Ambient temperature	Ta	-40		85	°C

Electrical Characteristics

All specifications at VDD=VDD_LVDS=VCP= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Conditions	MIN	TYP	MAX	Unit
Control Pin LVCMOS Input Characteristics					
Input high voltage (V_{IH})		0.6Vcc			V
Input low voltage (V_{IL})				0.4Vcc	V
Input high current (I_{IH})				200	uA
Input low current (I_{IL})				-200	uA
LVCMOS Output Characteristics					
Bypass output frequency		21.875		28.47	MHz
Output frequency		43.75		250	MHz
Output high voltage		Vcc-0.5			V
Output low voltage				0.3	
RMS phase jitter	250MHZ (10kHz to 20MHz)		0.4		ps, RMS
Output rise/fall slew rate	20% ⇔ 80%	2.4			
Output duty cycle		45		55	%
Skew between outputs			10		ps
LVPECL Output Characteristics					
Output frequency		43.75		683.264	MHz
Output high voltage		Vcc-1.18		Vcc-0.73	V
Output low voltage		Vcc-2		Vcc-1.55	V
Differential output voltage		0.6		1.23	V
RMS phase jitter	625MHZ (10kHz to 20MHz)		0.4		ps, RMS
Output rise/fall slew rate	20% ⇔ 80%			175	ps
Output duty cycle		45		55	%
Skew between outputs			10		ps
LVDS Output Characteristics					
Output frequency		43.75		683.264	MHz
Differential output voltage		0.247		0.454	V
Magnitude change				50	mV
Common-mode voltage		1.125		1.375	V
Magnitude change				50	mV
RMS phase jitter	625MHZ (10kHz to 20MHz)		0.4		ps, RMS
Output rise/fall time	20% ⇔ 80%			255	ps
Output duty cycle		45		55	%
Skew between outputs			10		ps

Typical Output Phase Noise Characteristics

All specifications at VDD=VDD_LVDS=VCP= 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Conditions	MIN	TYP	MAX	Unit
250MHz LVCMOS Input Characteristics					
Phase Noise @ 100Hz offset			-85		dBc/Hz
@ 1kHz offset			-113		dBc/Hz
@ 10kHz offset			-123		dBc/Hz
@ 100kHz offset			-125		dBc/Hz
@ 1MHz offset			-136		dBc/Hz
@ 10MHz offset			-154		dBc/Hz
@ 20MHz offset			-154		dBc/Hz
RMS Phase Jitter	10kHz to 20MHz		384		ps, RMS
625MHz LVPECL Output Characteristics					
Phase Noise @ 100Hz offset			-77		dBc/Hz
@ 1kHz offset			-105		dBc/Hz
@ 10kHz offset			-114		dBc/Hz
@ 100kHz offset			-117		dBc/Hz
@ 1MHz offset			-128		dBc/Hz
@ 10MHz offset			-150		dBc/Hz
@ 20MHz offset			-151		dBc/Hz
RMS Phase Jitter	10kHz to 20MHz		387		ps, RMS
625MHz LVDS Output Characteristics					
Phase Noise @ 100Hz offset			-77		dBc/Hz
@ 1kHz offset			-105		dBc/Hz
@ 10kHz offset			-114		dBc/Hz
@ 100kHz offset			-117		dBc/Hz
@ 1MHz offset			-127		dBc/Hz
@ 10MHz offset			-150		dBc/Hz
@ 20MHz offset			-152		dBc/Hz
RMS Phase Jitter	10kHz to 20MHz		395		ps, RMS

Crystal Characteristics

Parameter	MIN	TYP	MAX	Unit
Frequency	21.875		28.47	MHz
Equivalent series resistance			50	Ω
On-chip load capacitance		8	10	pF
Drive level	0.1		1	mW
Maximum shunt capacitance			7	pF

Device Configuration

Common Configuration

Input [MHz]	Prescaler Divider	Feedback Divider	VCO Frequency [MHz]	Output Divider	Output Frequency [MHz]	Application
25	4	20	2000	8	62.5	GigE
24.75	3	24	1782	8	74.25	HDTV
25	3	24	1800	8	75	SATA
24.8832	3	25	1866.24	8	77.76	SONET
25	3	24	1800	6	100	PCI Express
26.5625	3	24	1912.5	6	106.25	Fiber Channel
25	4	20	2000	4	125	GigE
25	3	24	1800	4	150	SATA
24.8832	3	25	1866.24	4	155.52	SONET
25	3	25	1875	4	156.25	10 GigE
26.5625	3	24	1912.5	4	159.375	10-G Fiber Channel
25	5	15	1875	2	187.5	12 GigE
25	3	24	1800	3	200	PCI Express
26.5625	3	24	1912.5	3	212.5	4-G Fiber Channel
25	4	20	2000	2	250	GigE
24.8832	3	25	1866.24	2	311.04	SONET
25	3	25	1875	2	312.5	XGMII
24.8832	3	25	1866.24	1	622.08	SONET
25	3	25	1875	1	625	10 GigE

Generic Configuration

Input Frequency Range [MHz]	Prescaler Divider	Feedback Divider	VCO Frequency [MHz]	Output Divider	Output Frequency [MHz]
21.875 to 25.62	4	20	1750 to 2050	8	54.6875 to 64.05
21.875 to 25.62	4	20	1750 to 2050	6	72.92 to 85.4
21.875 to 25.62	4	20	1750 to 2050	4	109.375 to 128.1
21.875 to 25.62	4	20	1750 to 2050	3	145.84 to 170.8
21.875 to 25.62	4	20	1750 to 2050	2	218.75 to 256.2
21.875 to 25.62	4	20	1750 to 2050	1	437.5 to 512.4
23.33 to 27.33	3	25	1750 to 2050	8	72.906 to 85.408
23.33 to 27.33	3	25	1750 to 2050	6	97.21 to 113.875
23.33 to 27.33	3	25	1750 to 2050	4	145.821 to 170.816
23.33 to 27.33	3	25	1750 to 2050	3	194.42 to 227.75
23.33 to 27.33	3	25	1750 to 2050	2	291.624 to 341.632
23.33 to 27.33	3	25	1750 to 2050	1	583.248 to 683.264
23.33 to 27.33	5	15	1750 to 2050	8	43.75 to 51.25
23.33 to 27.33	5	15	1750 to 2050	6	58.33 to 68.33
23.33 to 27.33	5	15	1750 to 2050	4	87.5 to 102.5
23.33 to 27.33	5	15	1750 to 2050	3	116.66 to 136.66
23.33 to 27.33	5	15	1750 to 2050	2	175 to 205
23.33 to 27.33	5	15	1750 to 2050	1	350 to 410
24.305 to 28.47	3	24	1750 to 2050	8	72.915 to 85.41
24.305 to 28.47	3	24	1750 to 2050	6	97.22 to 113.88
24.305 to 28.47	3	24	1750 to 2050	4	145.83 to 170.82
24.305 to 28.47	3	24	1750 to 2050	3	194.44 to 227.76
24.305 to 28.47	3	24	1750 to 2050	2	291.66 to 341.64
24.305 to 28.47	3	24	1750 to 2050	1	583.32 to 683.28

Programmable Prescaler and Feedback Divider Settings

Control Inputs		Prescaler Divider	Feedback Divider	PFD Frequency	
PR1	PR0			Minimum	Maximum
0	0	3	24	24.305	28.47
0	1	5	15	23.33	27.33
1	0	3	25	23.33	27.33
1	1	4	20	21.875	25.62

Programmable Output Divider Settings

Control Inputs			Output Divider
OD2	OD1	OD0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	Reserved
1	0	1	6
1	1	0	Reserved
1	1	1	8

Programmable Output Type

Control Inputs		Output Type
OS1	OS0	
0	0	LVCMOS, OSC_OUT Off
0	1	LVDS, OSC_OUT Off
1	0	LVPECL, OSC_OUT Off
1	1	LVPECL, OSC_OUT On

Output Enable

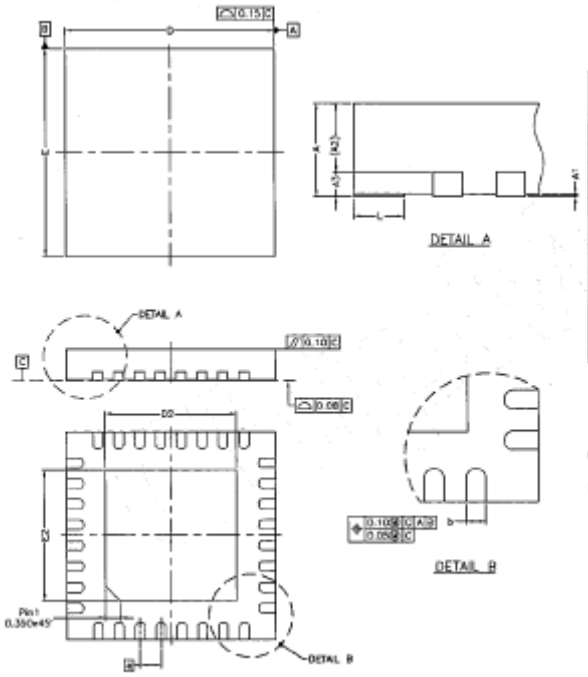
Control Inputs	Operating Condition	Output
CE		
0	Power Down	Hi-Z
1	Normal	Active

Reset

Control Inputs	Operating Condition	Output
$\overline{\text{RSTN}}$		
0	Device Reset	Hi-Z
0 → 1	PLL Recalibration	Hi-Z
1	Normal	Active

Package Information

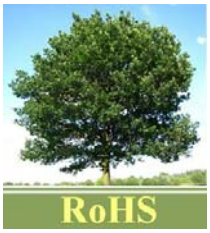
- **Mechanical data**



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	4.90	5.00	5.10	193	197	201
D1		–			–	
D2	3.00	3.15	3.30	118	124	130
E	4.90	5.00	5.10	193	197	201
E1		–			–	
E2	3.00	3.15	3.30	118	124	130
e	0.5 BSC			20 BSC		
L	0.30	0.40	0.50	12	16	20

NOTE :
1. REFER TO JEDEC STD: MO-220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

- **RoHS Compliance**



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