阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

18 GHz Microwave PLL Synthesizer

Data Sheet **ADF41020**

FEATURES

- 18 GHz maximum RF input frequency
- Integrated SiGe prescaler
- Software compatible with the ADF4106/ADF4107/ADF4108 family of PLLs
- 2.85 V to 3.15 V PLL power supply
- Programmable dual-modulus prescaler 8/9, 16/17, 32/33, 64/65
- Programmable charge pump currents
- 3-wire serial interface
- Digital lock detect
- Hardware and software power-down mode
- 4000 V HBM/1500 V CDM ESD performance

APPLICATIONS

- Microwave point-to-point/multipoint radios
- Wireless infrastructure
- VSAT radios
- Test equipment
- Instrumentation

GENERAL DESCRIPTION

The ADF41020 frequency synthesizer can be used to implement local oscillators as high as 18 GHz in the up conversion and down conversion sections of wireless receivers and transmitters. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, and high frequency programmable feedback dividers (A, B, and P). A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). The synthesizer can be used to drive external microwave VCOs via an active loop filter. Its very high bandwidth means a frequency doubler stage can be eliminated, simplifying system architecture and reducing cost. The ADF41020 is software-compatible with the existing ADF4106/ADF4107/ADF4108 family of devices from Analog Devices, Inc. Their pinouts match very closely with the exception of the ADF41020's single-ended RF input pin, meaning only a minor layout change is required when updating current designs.

FUNCTIONAL BLOCK DIAGRAM

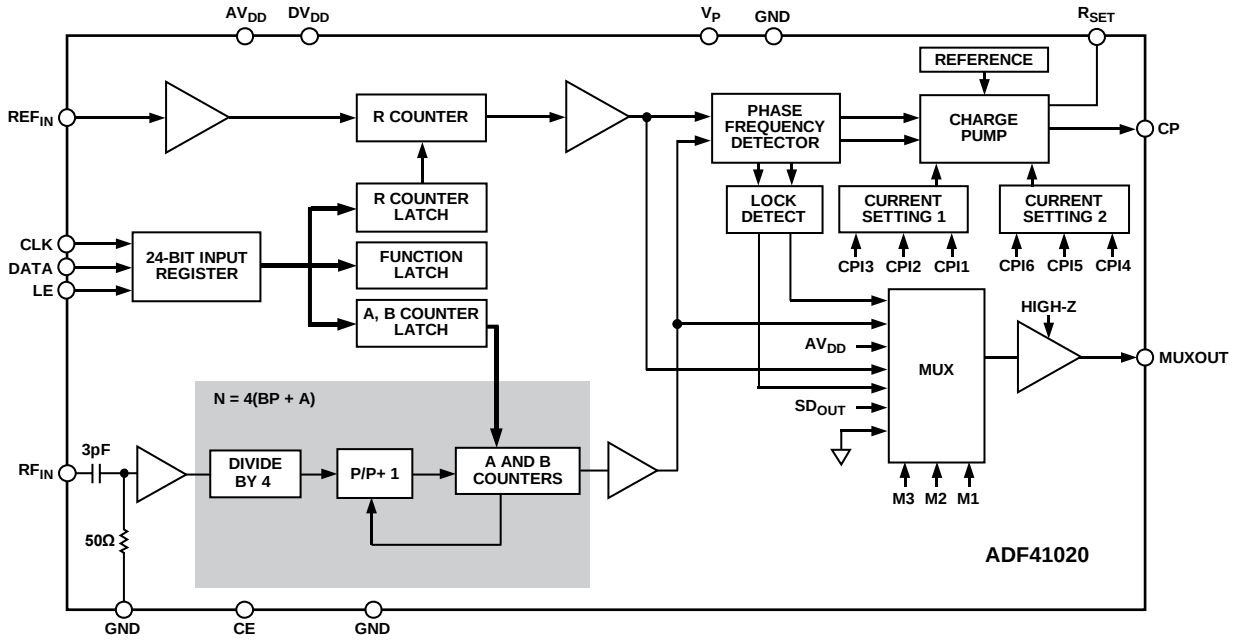

Figure 1.

Rev. C Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

ADF41020* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF41020 Evaluation Board

DOCUMENTATION

Data Sheet

- ADF41020: 18 GHz Microwave PLL Synthesizer Data Sheet

User Guides

- UG-405: Evaluation Board for the ADF41020 PLL Frequency Synthesizer
- UG-476: PLL Software Installation Guide

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADF41020 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADF41020 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

12/14—Rev. B to Rev. C

Changes to Features Section ... 1
Changes to Lock Detect Section ... 9

1/14—Rev. A to Rev. B

Changes to Figure 6 ... 7

11/13—Rev. 0 to Rev. A

Changes to Features Section ... 1
Changes to Absolute Maximum Ratings Section and Table 3 ... 5

10/12—Revision 0: Initial Version

SPECIFICATIONS

DV_{DD} = AV_{DD} = V_P = 3.0 V ± 5%, GND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					See Figure 1 for input circuit
RF Input Frequency (RF_{IN})	4.0		18.0	GHz	
RF Input Sensitivity	−10		+10	dBm	
Maximum Allowable Prescaler Output Frequency[1]			350	MHz	
REF_{IN} CHARACTERISTICS					
REF_{IN} Input Frequency	10		400	MHz	For f < 10 MHz, ensure slew rate > 50 V/µs
REF_{IN} Input Sensitivity	0.8		DV_{DD}	V p-p	Biased at DV_{DD}/2 when input is ac-coupled
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency[2]			100	MHz	
CHARGE PUMP					Programmable, see Figure 17
I_{CP} Sink/Source					
High Value		5.0		mA	With R_{SET} = 5.1 kΩ
Low Value		625		µA	
Absolute Accuracy		3		%	With R_{SET} = 5.1 kΩ
R_{SET}	5.1	5.1	5.1	kΩ	See Figure 17
I_{CP} Three-State Leakage		1	2	nA	T_A = 25°C
Sink and Source Current Matching		2		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. V_{CP}		1		%	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = V_P/2
LOGIC INPUTS					
V_{IH}, Input High Voltage	1.4			V	The SPI interface is 1.8 V and 3 V logic compatible
V_{IL}, Input Low Voltage			0.6	V	
I_{INH}, I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	DV_{DD} − 0.4			V	CMOS output chosen
I_{OH}, Output High Current			500	µA	
V_{OL}, Output Low Voltage			0.4	V	
I_{OL}, Output Low Current			500	µA	
POWER SUPPLIES					
AV_{DD}	2.85		3.15	V	
DV_{DD}	2.85		3.15	V	
V_P	2.85		3.15	V	
I_{DD}[3]		27	30	mA	T_A = 25°C
I_P[3]		4.5	5	mA	T_A = 25°C
Power-Down Mode		1		µA	T_A = 25°C

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor[4]		−221		dBc/Hz	PLL loop bandwidth = 500 kHz
Normalized 1/f Noise[5]		−118		dBc/Hz	Normalized to 10 kHz offset at 1 GHz
Phase Noise Performance[6]					At VCO output
5.7 GHz		−89		dBc/Hz	At 1 kHz offset and 2.5 MHz PFD frequency with 20 kHz loop bandwidth
12.5 GHz[7]		−82		dBc/Hz	At 3 kHz offset and 2.5 MHz PFD frequency with 20 kHz loop bandwidth
17.64 GHz		−96		dBc/Hz	At 100 kHz offset and 90 MHz PFD frequency with 700 kHz loop bandwidth
Spurious Signals					
5.7 GHz		−80/−86		dBc	At 2.5 MHz/5 MHz and 2.5 MHz PFD frequency
12.5 GHz[7]		−98/<−110		dBc	At 2.5 MHz/5 MHz and 2.5 MHz PFD frequency
17.64 GHz		−109/−113		dBc	At 90 MHz/180 MHz and 90 MHz PFD frequency

[1] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] T_A = 25°C; AV_{DD} = DV_{DD} = V_P = 3.0 V; P = 16; $f_{REF_{IN}}$ = 100 MHz; f_{PFD} = 100 MHz; RF_{IN} = 12.8 GHz.
[4] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log f_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10 \log f_{PFD} - 20 \log N$.
[5] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by $PN = PN_{1\_f} + 10 \log(10 \text{ kHz}/f) + 20 \log(f_{RF}/1 \text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[6] The phase noise is measured with a Rohde & Schwarz FSUP spectrum analyzer. The reference is provided by a Rohde & Schwarz SMA100A.
[7] The phase noise and spurious noise is measured with the EV-ADF41020EB1Z evaluation board and the Rohde & Schwarz FSUP spectrum analyzer.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = V_P = 3.0 V, GND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 2.

Parameter	Limit	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLK setup time
t_2	10	ns min	DATA to CLK hold time
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time
t_6	20	ns min	LE pulse width

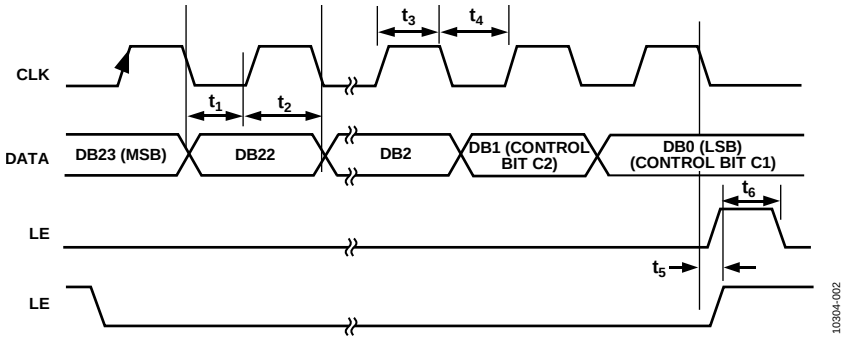

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +3.9 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +3.9 V
V_P to AV_{DD}	−0.3 V to +0.3 V
Digital I/O Voltage, REF_{IN} to GND	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance[1] (Paddle Soldered)	62.82°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6610
Bipolar	358
ESD (Charged Device Model)	1500 V
ESD (Human Body Model)	4000 V

[1] Two signal planes (that is, on the top and bottom surfaces of the board), two buried planes, and four vias.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

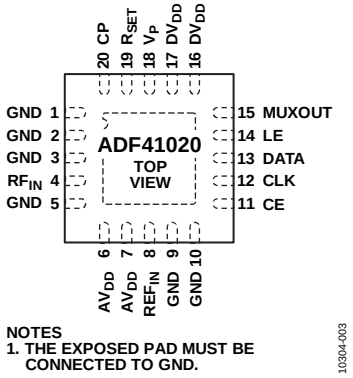

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 5, 9, 10	GND	Ground Pins.
4	RF_{IN}	Input to the RF Prescaler. This input is ac-coupled internally.
6, 7	AV_{DD}	Analog Power Supply. This may range from 2.85 V to 3.15 V. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. Pin 6 is the supply for the fixed divide-by-4 prescaler.
8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $DV_{DD}/2$ and a dc equivalent input resistance of 100 kΩ (see Figure 9). This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, PD1.
12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This is a high impedance CMOS input.
13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This is a high impedance CMOS input.
14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches with the latch being selected using the control bits.
15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
16, 17	DV_{DD}	Digital Power Supply. This may range from 2.85 V to 3.15 V. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
18	V_P	Charge Pump Power Supply.
19	R_{SET}	Connecting a resistor between this pin and GND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $$I_{CP\,MAX} = \frac{25.5}{R_{SET}}$$ So, with R_{SET} = 5.1 kΩ, $I_{CP\,MAX}$ = 5.0 mA.
20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
	EP	Exposed Pad. The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

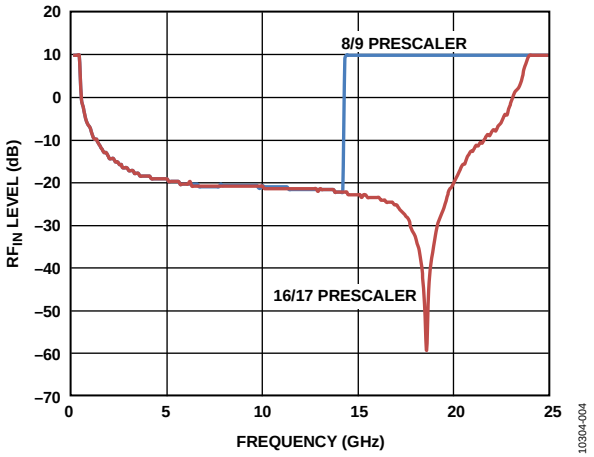

Figure 4. RF Input Sensitivity

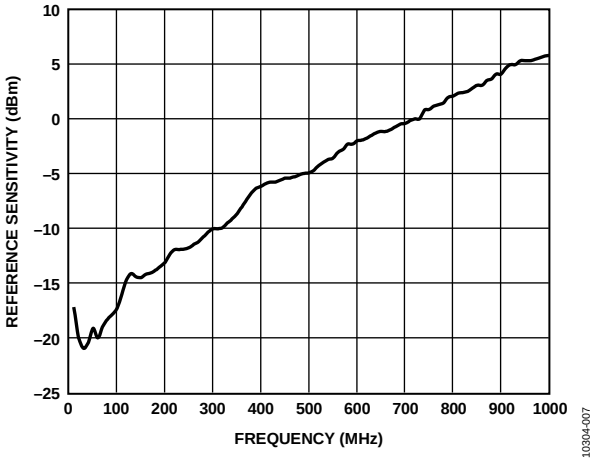

Figure 7. REF$_{IN}$ Sensitivity

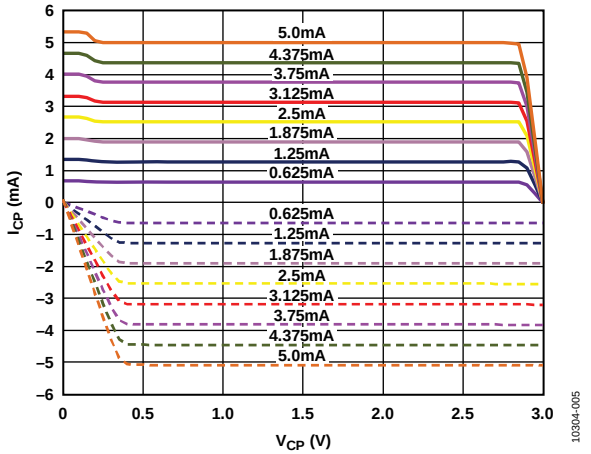

Figure 5. Charge Pump Output Characteristics

FREQ UNIT: GHz KEYWORD: R
PARAM TYPE: S
DATA FORMAT: MA

FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
4.0	0.20099200	−133.9429000	10.2	0.05542031	130.0581000
4.2	0.19669930	−134.7069000	10.4	0.05306026	126.9556000
4.4	0.19140480	−135.0024000	10.6	0.05123230	115.8988000
4.6	0.18317790	−135.1249000	10.8	0.04471957	102.0333000
4.8	0.17232760	−135.0415000	11.0	0.03846892	86.3895600
5.0	0.16071930	−135.1840000	11.4	0.03402513	51.1515300
5.2	0.14943970	−136.0447000	11.8	0.04456061	21.0829700
5.4	0.13791310	−137.7694000	12.2	0.05158395	16.8124600
5.6	0.12839340	−140.5623000	12.6	0.06039219	16.5178200
5.8	0.12090700	−144.7454000	13.0	0.05580344	31.4631600
6.0	0.11516160	−149.8260000	13.4	0.08402054	36.3540700
6.2	0.11252430	−155.1801000	13.8	0.10374910	18.8428500
6.4	0.11213720	−160.0477000	14.2	0.11639920	0.2817307
6.6	0.11236920	−164.5794000	14.6	0.13647950	−15.4473000
6.8	0.11323590	−168.1217000	15.0	0.16700580	−22.3273100
7.0	0.11401910	−170.9163000	15.2	0.18309070	−24.3333900
7.2	0.11361600	−173.2882000	15.4	0.19458010	−25.3870800
7.4	0.11225360	−175.2539000	15.6	0.20377790	−25.0101800
7.6	0.10909150	−176.9327000	15.8	0.21170140	−24.2554800
7.8	0.10484100	−179.0774000	16.0	0.21883690	−23.4312200
8.0	0.09871251	178.5525000	16.2	0.22280700	−23.5596400
8.2	0.09258573	175.9697000	16.4	0.22498210	−24.411100
8.4	0.08667851	172.5878000	16.6	0.22589250	−26.5202700
8.6	0.08075383	168.3692000	16.8	0.22572100	−30.3773300
8.8	0.07542522	163.5676000	17.0	0.22596830	−36.2808700
9.0	0.07048169	159.0954000	17.2	0.23197900	−42.8398200
9.2	0.06751262	154.6976000	17.4	0.24339450	−50.7222200
9.4	0.06561201	149.2087000	17.6	0.26023130	−57.5844600
9.6	0.06308079	142.2284000	17.8	0.28636130	−63.0764200
9.8	0.05995205	137.8226000	18.0	0.31905490	−67.5389600
10.0	0.05666475	134.1730000			

10304-008

Figure 8. S-Parameters

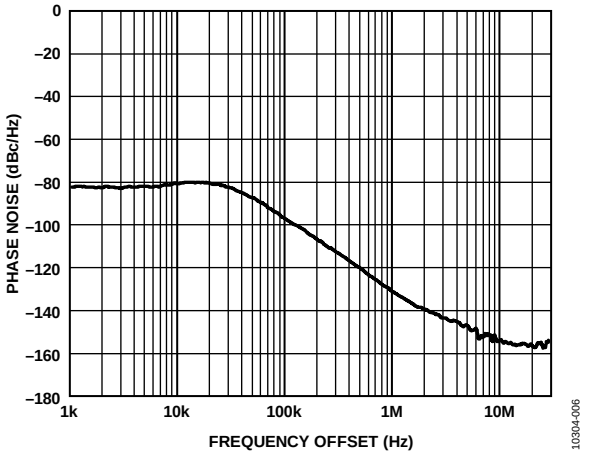

Figure 6. Closed-Loop Phase Noise, RF = 12.5 GHz, PFD = 2.5 MHz, Loop Bandwidth = 20 kHz

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 9. SW1 and SW2 are normally closed switches. SW3 is a normally open switch. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

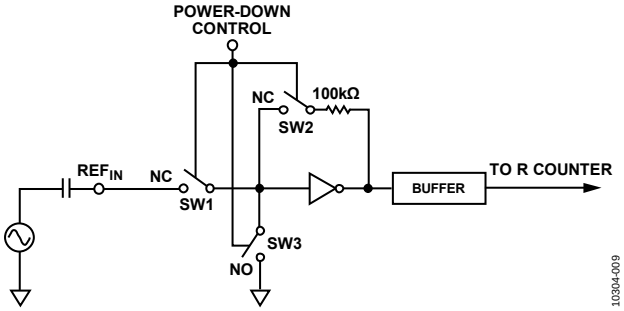

Figure 9. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 10. It is followed by a buffer, which generates the differential CML levels needed for the prescaler.

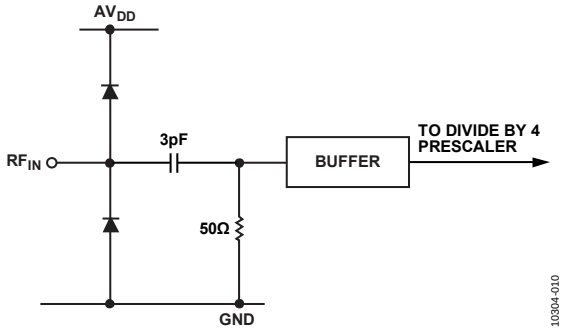

Figure 10. RF Input Stage

PRESCALER

The ADF41020 uses a two prescaler approach to achieve operation up to 18 GHz. The first prescaler is a fixed divide-by-4 block. The second prescaler, which takes its input from the divide-by-4 output, is implemented as a dual-modulus prescaler (P/P + 1), which allows finer frequency resolution vs. a fixed prescaler. Along with the A counter and B counter, this enables the large division ratio, N, to be realized (N = 4(BP + A)). The dual-modulus prescaler, operating at CML levels, takes the clock from the fixed prescaler stage and divides it down to a manageable frequency for the CMOS A counter and B counter. The second prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for contiguous output frequencies. This minimum is given by $4(P^2 - P)$.

A COUNTER AND B COUNTER

The A counter and B counter combine with the two prescalers to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 350 MHz or less.

Pulse Swallow Function

Because of the fixed divide-by-4 block, the generated output frequencies are spaced by four times the reference frequency divided by R. The equation for VCO frequency is

$$f_{VCO} = \left[(P \times B) + A\right] \times \frac{4 \times f_{REF_{IN}}}{R}$$

where:

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (such as, 8/9, 16/17).

B is the preset divide ratio of the binary 13-bit counter (2 to 8191).

A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).

$f_{REF_{IN}}$ is the external reference frequency oscillator.

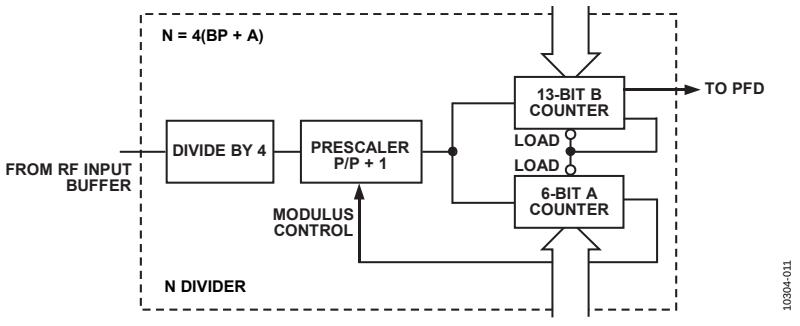

Figure 11. Prescalers, A and B Counters that Make Up the N-Divide Value

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PFD AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 13 is a simplified schematic. The PFD includes a fixed delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. The charge pump converts the PFD output to current pulses, which are integrated by the PLL loop filter.

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF41020 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 17 shows the full truth table. Figure 12 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed with digital lock detect.

Digital lock detect is active high. Digital lock detect is set high when the phase error on five consecutive phase detector cycles is less than 15 ns. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

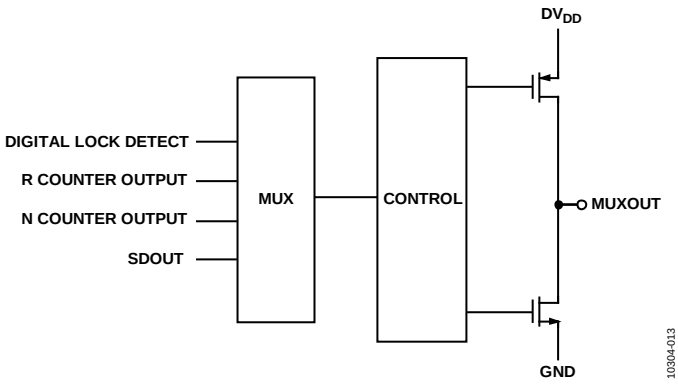

Figure 12. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF41020 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of three latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. C2 and C1 are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5. Table 5 shows a summary of how the latches are programmed. The SPI is both 1.8 V and 3 V compatible.

Table 5. C1, C2 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R counter
0	1	N counter (A and B)
1	0	Function latch (including prescaler)

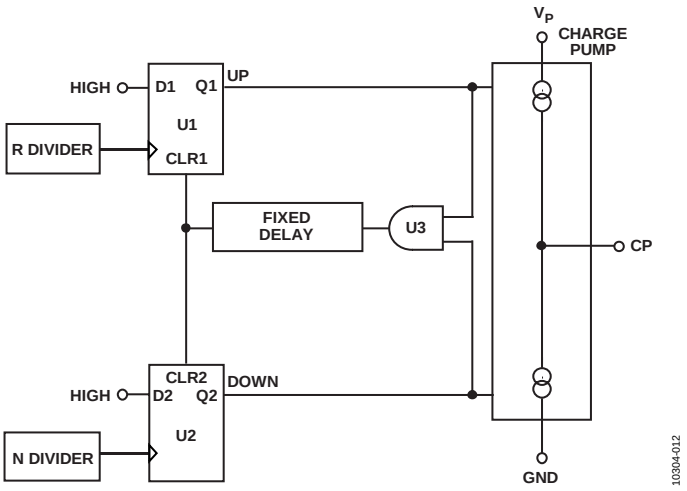

Figure 13. PFD Simplified Schematic

REFERENCE COUNTER LATCH

RESERVED								14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FAST LOCK MODE	FAST LOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

10304-014

Figure 14. Latch Summary

RESERVED								14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

10304-015

Figure 15. Reference Counter Latch Map

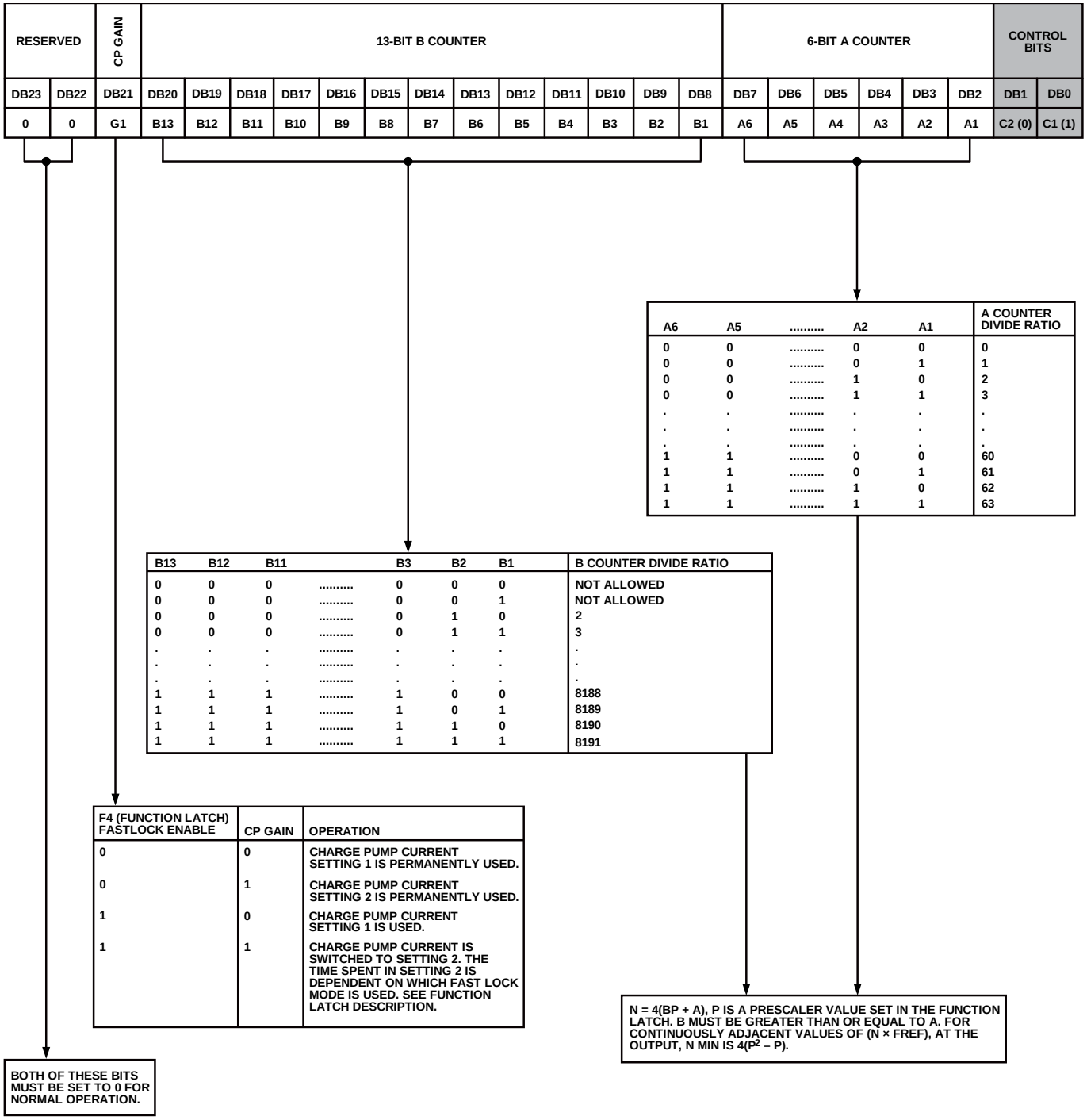

Figure 16. N (A, B) Counter Latch Map

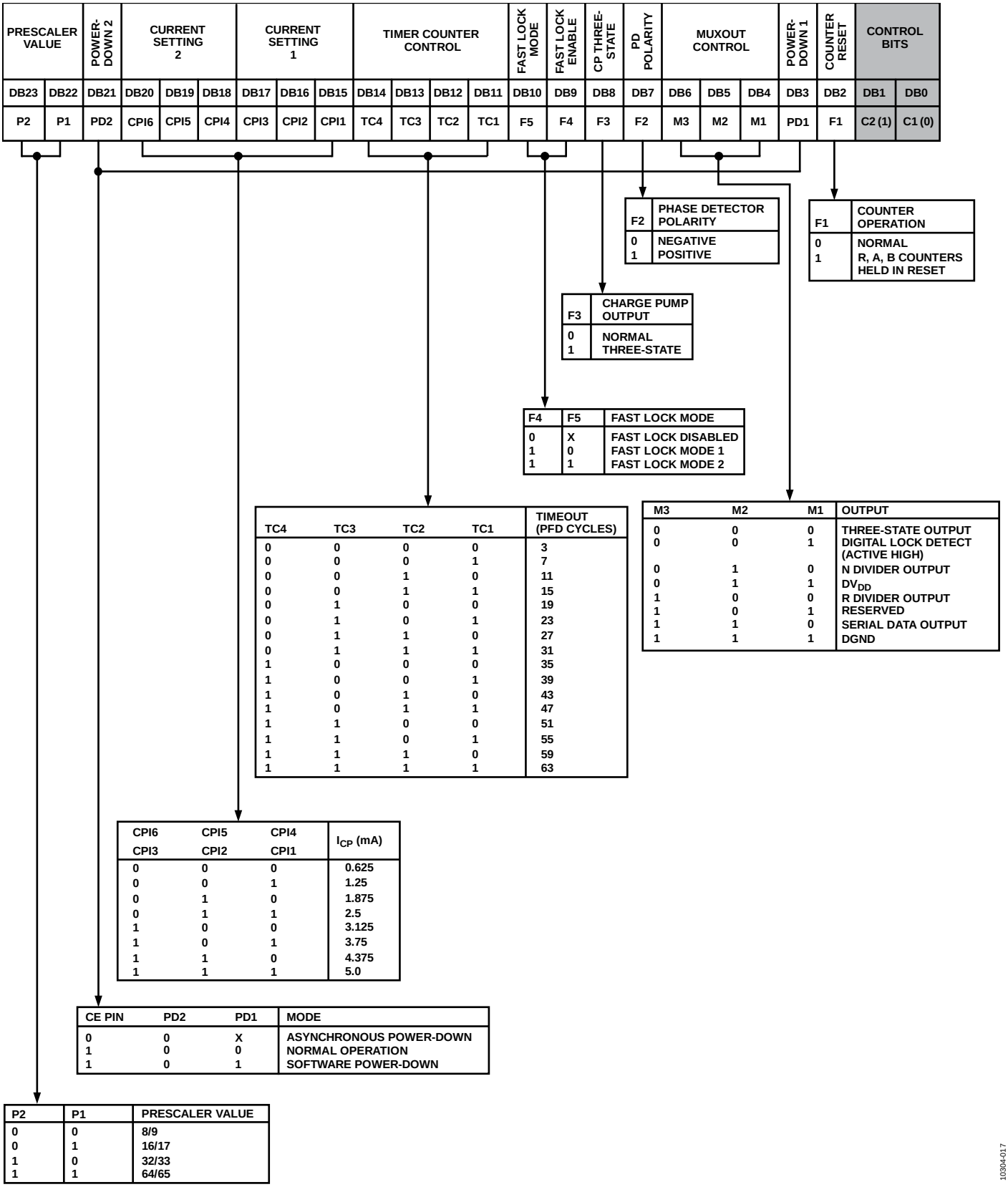

Figure 17. Function Latch Map

THE FUNCTION LATCH

With C2 and C1 set to 1 and 0, respectively, the on-chip function latch is programmed. Figure 17 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this is 1, the R counter and the N (A, B) counter is reset. For normal operation, this bit should be 0. When powering up, disable the F1 bit (set to 0). The N counter then resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle).

Power-Down

Bit DB3 (PD1) provides a software power-down mode to reduce the overall current drawn by the device. It is enabled by the CE pin. When the CE pin is low, the device is immediately disabled regardless of the state of PD1.

In the programmed software power-down, the device powers down immediately after latching 1 into the PD1 bit. PD2 is a reserved bit and should be cleared to 0.

When a power-down is activated, the following events occur:

- All active dc current paths in the main synthesizer section are removed. However, the RF divide-by-4 prescaler remains active.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF41020. Figure 17 shows the truth table.

Fast Lock Enable Bit

Bit DB9 (F4) of the function latch is the fast lock enable bit. When this bit is 1, fast lock is enabled.

Fast Lock Mode Bit

Bit DB10 (F5)of the function latch is the fast lock mode bit. When fast lock is enabled, this bit determines which fast lock mode is used. If the fast lock mode bit is 0, then Fast Lock Mode 1 is selected; and if the fast lock mode bit is 1, then Fast Lock Mode 2 is selected.

Fast Lock Mode 1

The charge pump current is switched to the contents of Current Setting 2. The device enters fast lock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fast lock when 0 is written to the CP gain bit in the N (A, B) counter latch.

Fast Lock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters fast lock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fast lock under the control of the timer counter. After the timeout period, which is determined by the value in TC4 to TC1, the CP gain bit in the N (A, B) counter latch is automatically reset to 0, and the device reverts to normal mode instead of fast lock. See Figure 17 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed). The normal sequence of events follows.

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 0.85 mA as Current Setting 1 and 1.7 mA as Current Setting 2.

Simultaneously, the decision must be made as to how long the secondary current stays active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 to DB11 (TC4 to TC1), in the function latch. The truth table is given in Figure 17.

To program a new output frequency, simply program the N (A, B) counter latch with new values for A and B. Simultaneously, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the N (A, B) counter latch is reset to 0 and is ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fast Lock Mode 2 is chosen by setting the fast lock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Figure 17.

Prescaler Value

P2 and P1 in the function latch set the programmable P prescaler value. The P value should be chosen so that the prescaler output frequency is always less than or equal to 350 MHz.

PD Polarity

Bit DB7 (F2) sets the phase detector polarity bit. See Figure 17.

CP Three-State

Bit DB8 (F3) controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

Device Programming After Initial Power-Up

After initial power up of the device, there are three methods for programming the device: function latch, CE pin, and counter reset.

Function Latch Method

1. Apply V_{DD}.
2. Program the function latch load (10 in two LSBs of the control word), making sure that the F1 bit is programmed to a 0.
3. Do an R load (00 in two LSBs).
4. Do an N (A, B) load (01 in two LSBs).

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asychronous power-down in that it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the N (A, B) counter latch (01).
6. Bring CE high to take the device out of power-down. The R and N (A, B) counters now resume counting in close alignment.

Note that after CE goes high, a 1 µs duration may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it is programmed at least once after V_{DD} is initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Do a function latch load (10 in two LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in two LSBs).
4. Do an N (A, B) counter load (01 in two LSBs).
5. Do a function latch load (10 in two LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides direct control over the internal counter reset.

APPLICATIONS INFORMATION

INTERFACING

The ADF41020 has a simple 1.8 V and 3 V SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz.

ADuC7020 Interface

Figure 18 shows the interface between the ADF41020 and the ADuC7019 to ADuC7023 family of analog microcontrollers. The ADuC70xx family is based on an AMR7 core, although the same interface can be used with any 8051-based microcontroller. The microcontroller is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF41020 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the microcontroller to the device. When the third byte is written, bring the LE input high to complete the transfer.

On first applying power to the ADF41020, it needs three writes (one each to the function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the microcontroller are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SPI transfer rate of the ADuC7023 is 20 Mbps. This means that the maximum rate at which the output frequency can be changed is 833 kHz. If using a faster SPI clock, ensure adherence to the SPI timing requirements listed in Table 1.

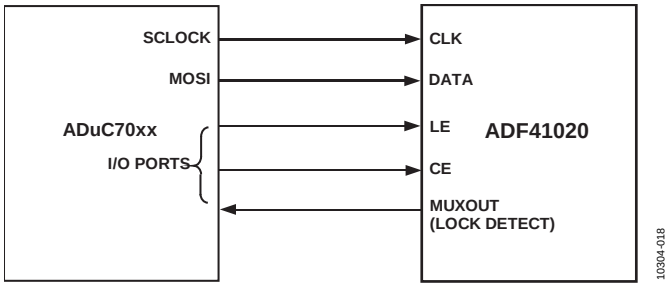

Figure 18. ADuC70xx-to-ADF41020 Interface

Blackfin BF527 Interface

Figure 19 shows the interface between the ADF41020 and the Blackfin® ADSP-BF527 digital signal processor (DSP). The ADF41020 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the Blackfin family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer. As in the microcontroller case, ensure the clock speeds are within the maximum limits outlined in Table 1.

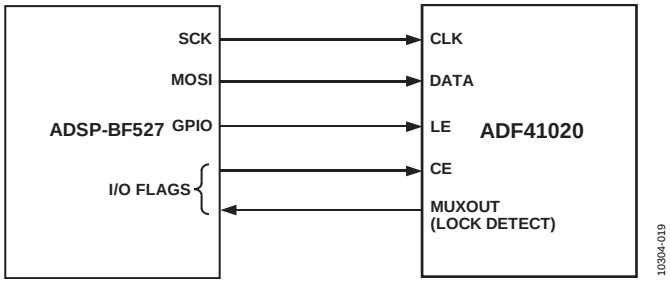

Figure 19. ADSP-BF527-to-ADF41020 Interface

PCB DESIGN GUIDELINES

The lands on the LFCSP (CP-20) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center the land on the pad to ensure that the solder joint size is maximized. The bottom of the LFCSP has a central thermal pad.

The thermal pad on the PCB should be at least as large as the exposed pad. To avoid shorting, on the PCB, provide a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern.

Thermal vias may be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and plate the via barrel with 1 oz copper to plug the via.

Connect the PCB thermal pad to GND.

OUTLINE DIMENSIONS

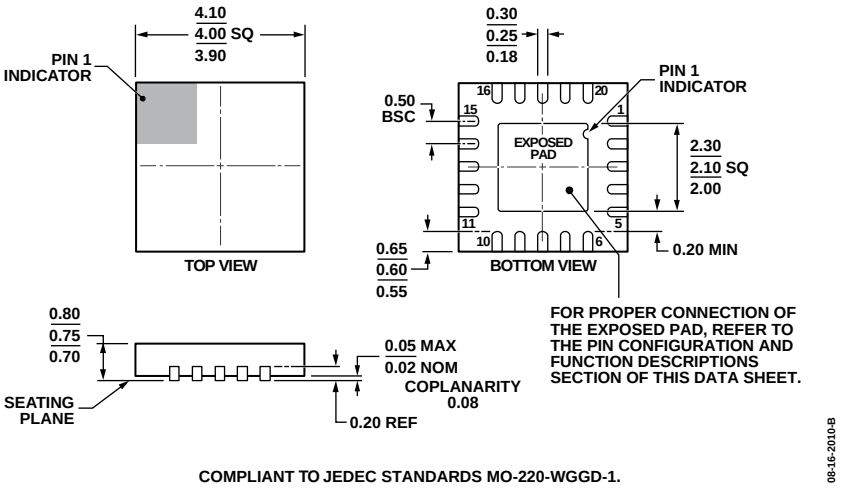

Figure 20. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF41020BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF41020BCPZ-RL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
EV-ADF41020EB1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.