

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



1.8V Wide Range Frequency Clock Driver

Recommended Application:

- DDR2 Memory Modules / Zero Delay Board Fan Out
- Provides complete DDR DIMM logic solution with ICSSTU32864

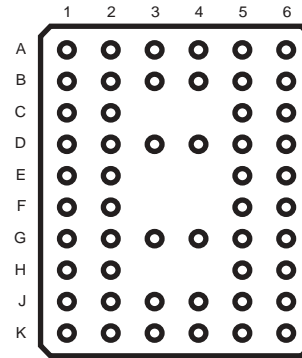
Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL_18)
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- Auto PD when input signal is at a certain logic state

Switching Characteristics:

- Period jitter: 40ps
- Half-period jitter: 60ps
- CYCLE - CYCLE jitter 40ps
- OUTPUT - OUTPUT skew: 40ps

Pin Configuration

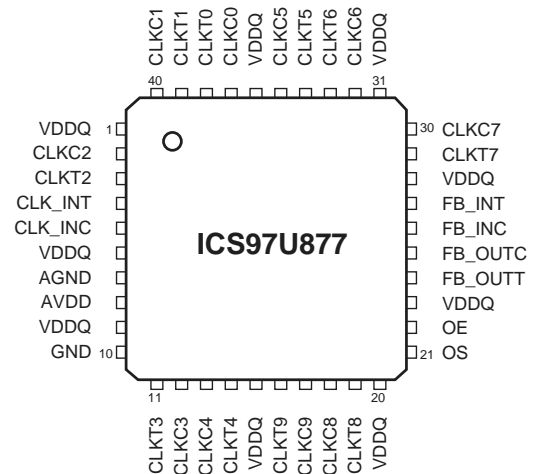
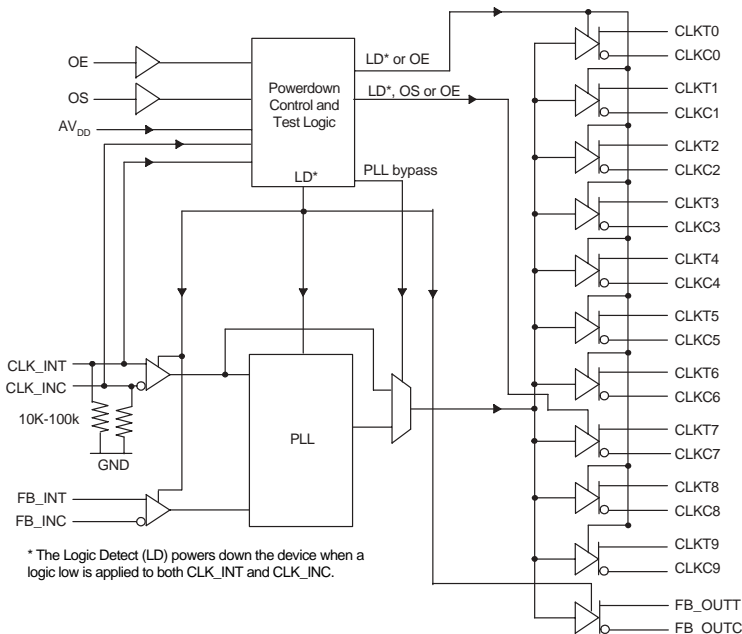


52-Ball BGA

Top View

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---------|-------|-------|-------|-------|---------|
| A | CLKT1 | CLKT0 | CLKC0 | CLKC5 | CLKT5 | CLKT6 |
| B | CLKC1 | GND | GND | GND | GND | CLKC6 |
| C | CLKC2 | GND | NB | NB | GND | CLKC7 |
| D | CLKT2 | VDDQ | VDDQ | VDDQ | OS | CLKT7 |
| E | CLK_INT | VDDQ | NB | NB | VDDQ | FB_INT |
| F | CLK_INC | VDDQ | NB | NB | OE | FB_INC |
| G | AGND | VDDQ | VDDQ | VDDQ | VDDQ | FB_OUTC |
| H | AVDD | GND | NB | NB | GND | FB_OUTT |
| J | CLKT3 | GND | GND | GND | GND | CLKT8 |
| K | CLKC3 | CLKC4 | CLKT4 | CLKT9 | CLKC9 | CLKC8 |

Block Diagram



40-Pin MLF



Pin Descriptions

| Terminal Name | Description | Electrical Characteristics |
|------------------|---|----------------------------|
| AGND | Analog Ground | Ground |
| AV _{DD} | Analog power | 1.8 V nominal |
| CLK_INT | Clock input with a (10K-100K Ohm) pulldown resistor | Differential input |
| CLK_INC | Complementary clock input with a (10K-100K Ohm) pulldown resistor | Differential input |
| FB_INT | Feedback clock input | Differential input |
| FB_INC | Complementary feedback clock input | Differential input |
| FB_OUTT | Feedback clock output | Differential output |
| FB_OUTC | Complementary feedback clock output | Differential output |
| OE | Output Enable (Asynchronous) | LVC MOS input |
| OS | Output Select (tied to GND or V _{DDQ}) | LVC MOS input |
| GND | Ground | Ground |
| V _{DDQ} | Logic and output power | 1.8V nominal |
| CLKT[0:9] | Clock outputs | Differential outputs |
| CLKC[0:9] | Complementary clock outputs | Differential outputs |
| NB | No ball | |

The PLL clock buffer, **ICS97U877**, is designed for a V_{DDQ} of 1.8 V, a AV_{DD} of 1.8 V and differential data input and output levels. Package options include a plastic 52-ball VFPGA and a 40-pin MLF.

ICS97U877 is a zero delay buffer that distributes a differential clock input pair (CLK_INT, CLK_INC) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock outputs (FB_OUTT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INT, CLK_INC), the feedback clocks (FB_INT, FB_INC), the LVC MOS program pins (OE, OS) and the Analog Power input (AVDD). When OE is low, the outputs (except FB_OUTT/FB_OUTC) are disabled while the internal PLL continues to maintain its locked-in frequency. OS (Output Select) is a program pin that must be tied to GND or V_{DDQ}. When OS is high, OE will function as described above. When OS is low, OE has no effect on CLK7/CLKC7 (they are free running in addition to FB_OUTT/FB_OUTC). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock signals (CLK_INT, CLK_INC) are logic low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INT, CLK_INC) within the specified stabilization time t_{STAB}.

The PLL in **ICS97U877** clock driver uses the input clocks (CLK_INT, CLK_INC) and the feedback clocks (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter output differential clocks (CLKT[0:9], CLKC[0:9]). **ICS97U877** is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

ICS97U877 is characterized for operation from 0°C to 70°C.



Function Table

| Inputs | | | | | Outputs | | | | PLL |
|-----------|----|----|---------|---------|---------------------------|---------------------------|---------|---------|--------------|
| AVDD | OE | OS | CLK_INT | CLK_INT | CLKT | CLKC | FB_OUTT | FB_OUTC | |
| GND | H | X | L | H | L | H | L | H | Bypassed/Off |
| GND | H | X | H | L | H | L | H | L | Bypassed/Off |
| GND | L | H | L | H | *L(Z) | *L(Z) | L | H | Bypassed/Off |
| GND | L | L | H | L | *L(Z), CLKT7 active | *L(Z), CLKC7 active | H | L | Bypassed/Off |
| 1.8V(nom) | L | H | L | H | *L(Z) | *L(Z) | L | H | On |
| 1.8V(nom) | L | L | H | L | *L(Z), CLKT7 active | *L(Z), CLKC7 active | H | L | On |
| 1.8V(nom) | H | X | L | H | L | H | L | H | On |
| 1.8V(nom) | H | X | H | L | H | L | H | L | On |
| 1.8V(nom) | X | X | L | L | *L(Z) | *L(Z) | *L(Z) | *L(Z) | Off |
| 1.8V(nom) | X | X | H | H | Reserved | | | | |

*L(Z) means the outputs are disabled to a low stated meeting the I_{ODL} limit.



Absolute Maximum Ratings

| | |
|-------------------------------|---------------------------------------|
| Supply Voltage (VDDQ & AVDD) | -0.5V to 2.5V |
| Logic Inputs | GND - 0.5V to V _{DDQ} + 0.5V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = 0 - 70°C; Supply Voltage AVDDQ, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------|---|------------------------|------|------|-------|
| Input High Current (CLK_INT, CLK_INC) | I _{IH} | V _I = V _{DDQ} or GND | | | ±250 | μA |
| Input Low Current (OE, OS, FB_INT, FB_INC) | I _{IL} | V _I = V _{DDQ} or GND | | | ±10 | μA |
| Output Disabled Low Current | I _{ODL} | OE = L, V _{ODL} = 100mV | 100 | | | μA |
| Operating Supply Current | I _{DD1.8} | C _L = 0pf @ 270MHz | | | 300 | mA |
| | I _{DDLD} | C _L = 0pf | | | 500 | μA |
| Input Clamp Voltage | V _{IK} | V _{DDQ} = 1.7V I _{in} = -18mA | | | -1.2 | V |
| High-level output voltage | V _{OH} | I _{OH} = -100 μA | V _{DDQ} - 0.2 | | | V |
| | | I _{OH} = -9 mA | 1.1 | 1.45 | | V |
| Low-level output voltage | V _{OL} | I _{OL} = 100 μA | | 0.25 | 0.10 | V |
| | | I _{OL} = 9 mA | | | 0.6 | V |
| Input Capacitance ¹ | C _{IN} | V _I = GND or V _{DDQ} | 2 | | 3 | pF |
| Output Capacitance ¹ | C _{OUT} | V _{OUT} = GND or V _{DDQ} | 2 | | 3 | pF |

¹Guaranteed by design, not 100% tested in production.



Recommended Operating Condition (see note1)

T_A = 0 - 70°C; Supply Voltage AVDD, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------------------------|---------------------------------------|----------------------------|--------------------|----------------------------|-------|
| Supply Voltage | V _{DDQ} , A _{VDD} | | 1.7 | 1.8 | 1.9 | V |
| Low level input voltage | V _{IL} | CLK_INT, CLK_INC, FB_INC, FB_INT | | | 0.35 x V _{DDQ} | V |
| | | OE, OS | | | 0.35 x V _{DDQ} | V |
| High level input voltage | V _{IH} | CLK_INT, CLK_INC, FB_INC, FB_INT | 0.65 x V _{DDQ} | | | V |
| | | OE, OS | 0.65 x V _{DDQ} | | | V |
| DC input signal voltage (note 2) | V _{IN} | | -0.3 | | V _{DDQ} + 0.3 | V |
| Differential input signal voltage (note 3) | V _{ID} | DC - CLK_INT, CLK_INC, FB_INC, FB_INT | 0.3 | | V _{DDQ} + 0.4 | V |
| | | AC - CLK_INT, CLK_INC, FB_INC, FB_INT | 0.6 | | V _{DDQ} + 0.4 | V |
| Output differential cross-voltage (note 4) | V _{OX} | | V _{DDQ} /2 - 0.10 | | V _{DDQ} /2 + 0.10 | V |
| Input differential cross-voltage (note 4) | V _{IX} | | V _{DDQ} /2 - 0.15 | V _{DD} /2 | V _{DDQ} /2 + 0.15 | V |
| High level output current | I _{OH} | | | | -9 | mA |
| Low level output current | I _{OL} | | | | 9 | mA |
| Operating free-air temperature | T _A | | 0 | | 70 | °C |

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signal must be crossing.



Timing Requirements

$T_A = 0 - 70^\circ\text{C}$ Supply Voltage AVDD, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS |
|-----------------------------|----------------------------|------------------|-----|-----|-------|
| Max clock frequency | freq_{op} | 1.8V±0.1V @ 25°C | 95 | 370 | MHz |
| Application Frequency Range | freq_{App} | 1.8V±0.1V @ 25°C | 160 | 350 | MHz |
| Input clock duty cycle | d_{tin} | | 40 | 60 | % |
| CLK stabilization | T_{STAB} | | | 15 | μs |

Switching Characteristics¹

$T_A = 0 - 70^\circ\text{C}$ Supply Voltage AVDD, VDDQ = 1.8 V +/- 0.1V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|------------------------|--------------------------|-------|------|-------|-------|
| Output enable time | t_{en} | OE to any output | | 4.73 | 8 | ns |
| Output disable time | t_{dis} | OE to any output | | 5.82 | 8 | ns |
| Period jitter | $t_{\text{jit(per)}}$ | | -30 | | 30 | ps |
| Half-period jitter | $t_{\text{jit(hper)}}$ | | -60 | | 60 | ps |
| Input slew rate | SLr1(i) | Input Clock | 1 | 2.5 | 4 | v/ns |
| | | Output Enable (OE), (OS) | 0.5 | | | v/ns |
| Output clock slew rate | SLr1(o) | | 1.5 | 2.5 | 3 | v/ns |
| Cycle-to-cycle period jitter | $t_{\text{jit(cc+)}}$ | | 0 | | 40 | ps |
| | $t_{\text{jit(cc-)}}$ | | 0 | | -40 | ps |
| Dynamic Phase Offset | $t_{\text{(dyn)}}$ | | -20 | | 20 | ps |
| Static Phase Offset | t_{SPO}^2 | | -50 | 0 | 50 | ps |
| Output to Output Skew | t_{skew} | | | | 40 | ps |
| SSC modulation frequency | | | 30.00 | | 33 | kHz |
| SSC clock input frequency deviation | | | 0.00 | | -0.50 | % |
| PLL Loop bandwidth (-3 dB from unity gain) | | | 2.0 | | | MHz |

Notes:

1. Switching characteristics guaranteed for application frequency range.
2. Static phase offset shifted by design.



Parameter Measurement Information

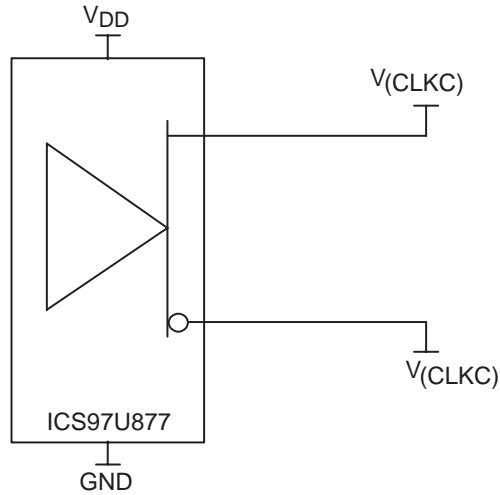


Figure 1. IBIS Model Output Load

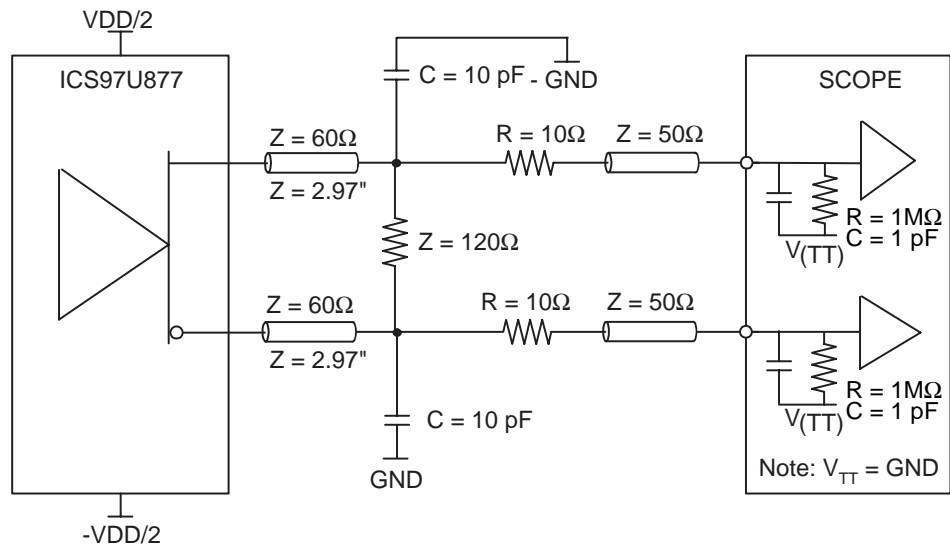


Figure 2. Output Load Test Circuit

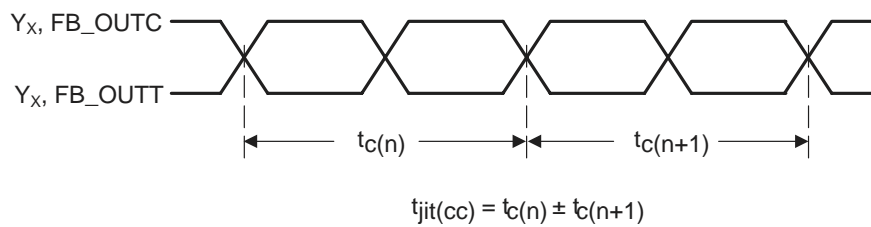
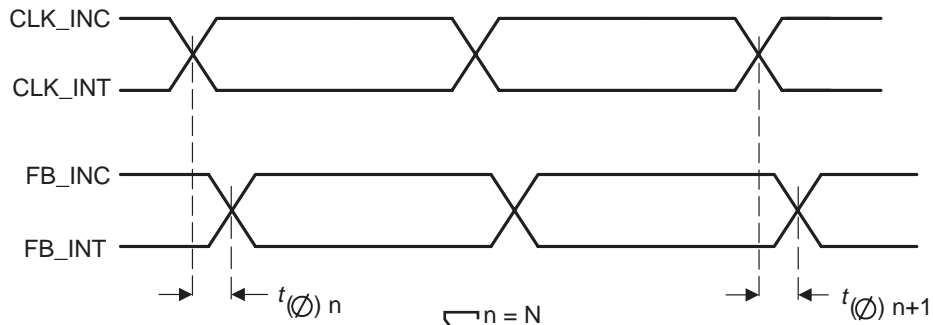


Figure 3. Cycle-to-Cycle Jitter



Parameter Measurement Information



$$t_{(\phi)} = \frac{\sum_{n=1}^N t_{(\phi) n}}{N}$$

(N is a large number of samples)

Figure 4. Static Phase Offset

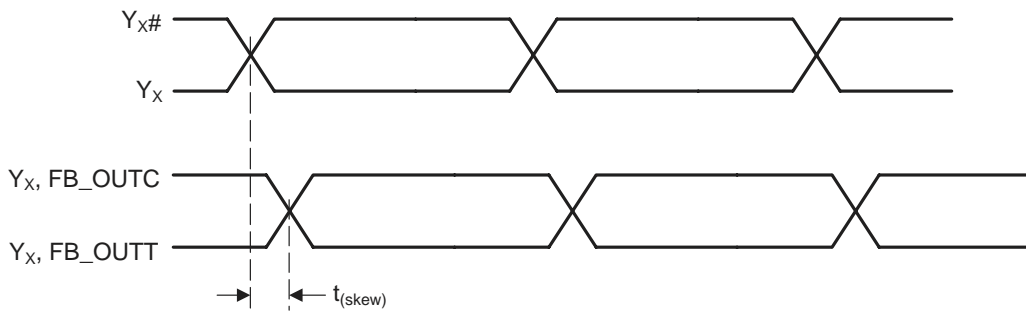
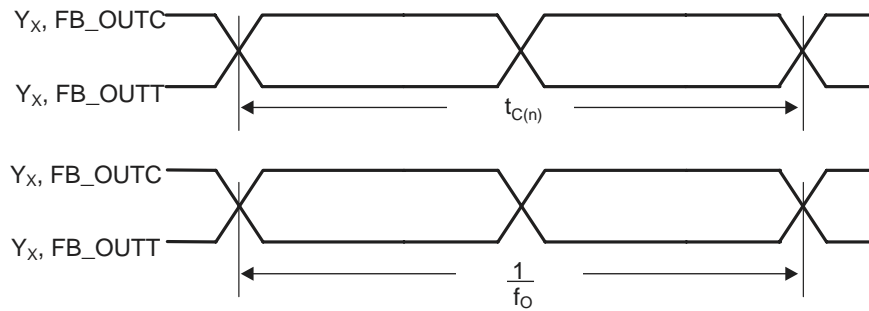


Figure 5. Output Skew



$$t_{(jit_per)} = t_{c(n)} - \frac{1}{f_0}$$

Figure 6. Period Jitter



Parameter Measurement Information

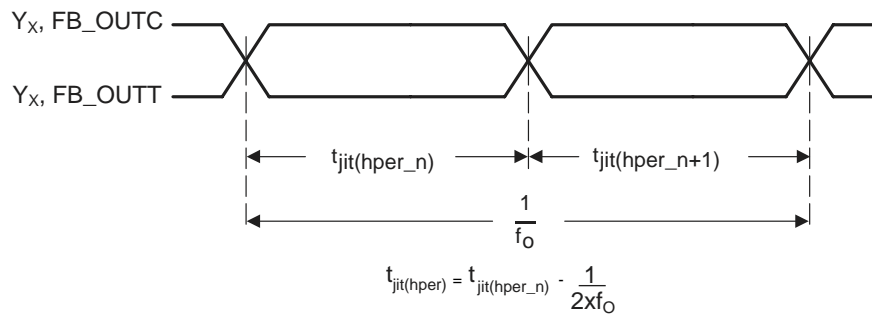


Figure 7. Half-Period Jitter

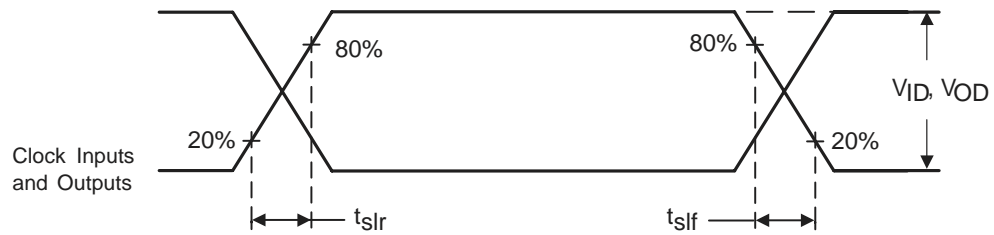


Figure 8. Input and Output Slew Rates

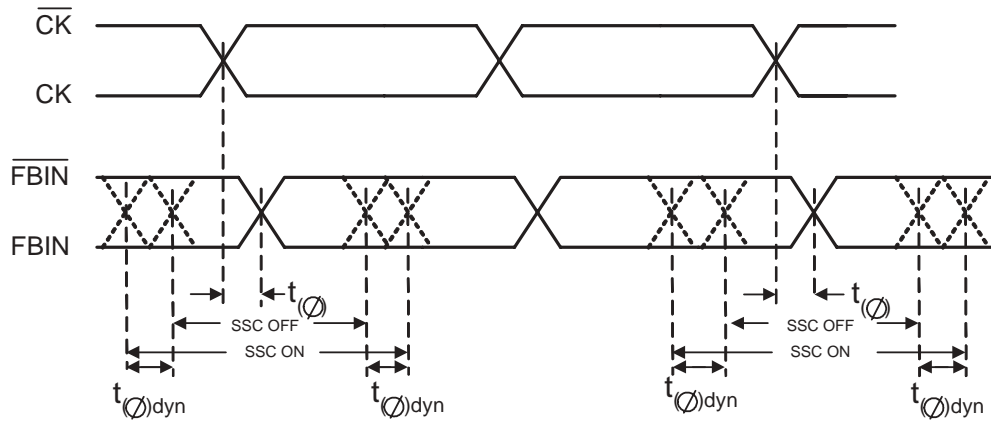


Figure 9. Dynamic Phase Offset

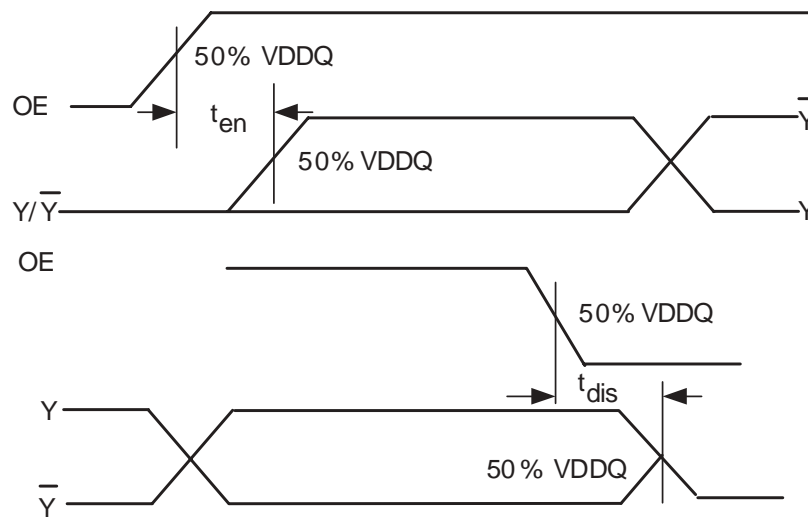


Figure 10. Time delay between OE and Clock Output (Y, \overline{Y})

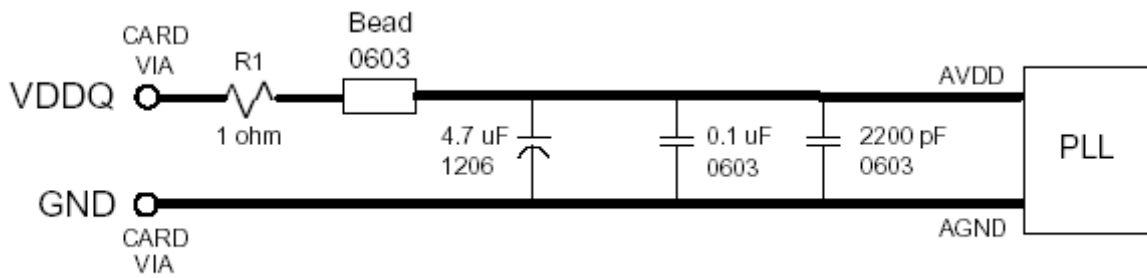
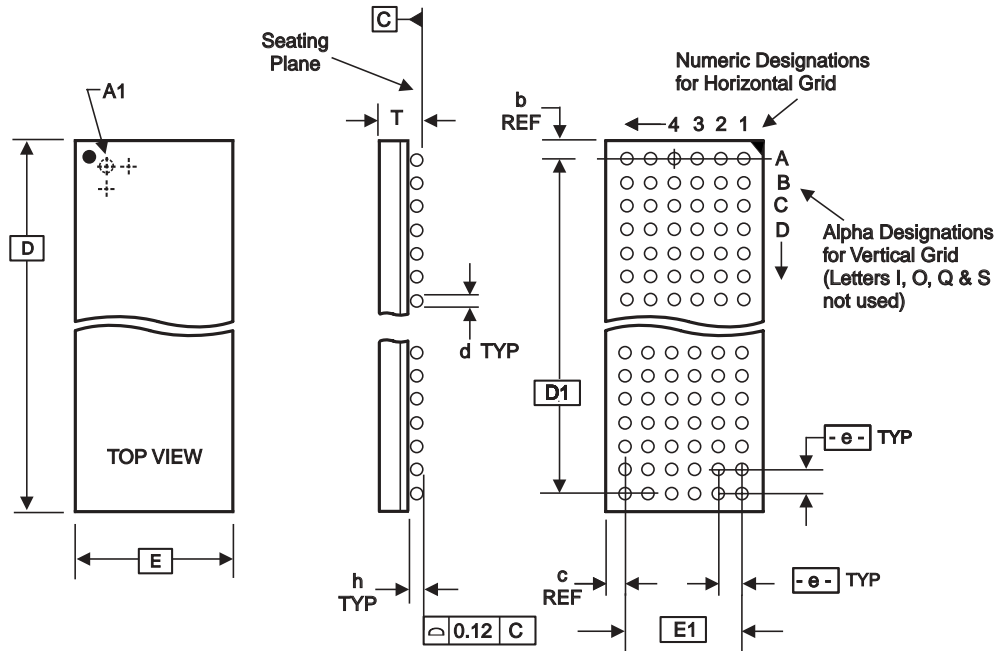


Figure 11. AV_{DD} Filtering

- Place the 2200pF capacitor close to the PLL.
- Use a wide trace for the PLL analog power & ground. Connect PLL & caps to AGND trace & connect trace to one GND via (farthest from PLL).
- Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.8 Ohm DC max, 600 Ohms @ 100 MHz).



ALL DIMENSIONS IN MILLIMETERS

| D | E | T Min/Max | e | BALL GRID | | Max. TOTAL | d Min/Max | h Min/Max | D1 | E1 | REF. DIMENSIONS | |
|----------|----------|--------------|----------|-----------|------|---------------|--------------|--------------|----------|----------|-----------------|-------|
| | | | | HORIZ | VERT | | | | | | b | c |
| 7.00 Bsc | 4.50 Bsc | 0.86/1.00 | 0.65 Bsc | 6 | 10 | 60 | 0.35/0.45 | 0.15/0.21 | 5.85 Bsc | 3.25 Bsc | 0.575 | 0.625 |

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

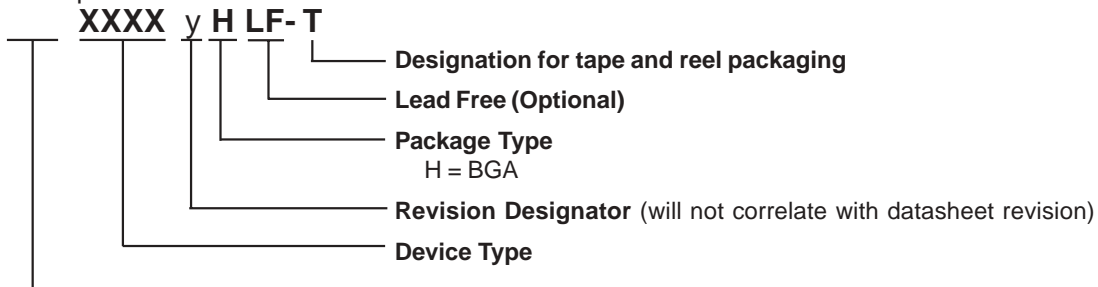
* Source Ref.: JEDEC Publication 95, MO-205*, MO-225**

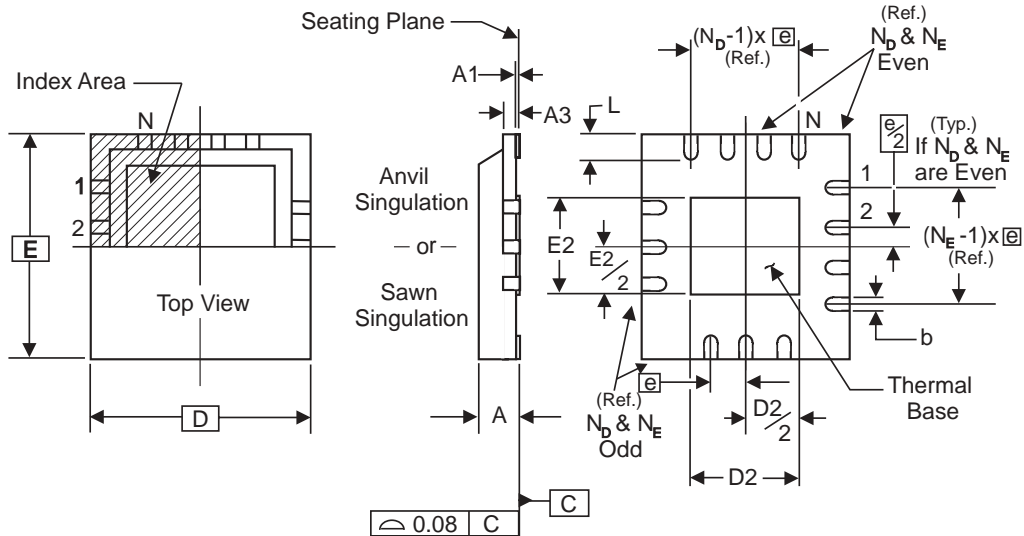
10-0055

Ordering Information

97U877yHLF-T

Example:





**THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE**

ALL DIMENSIONS IN MILLIMETERS

| N | 40 | SYMBOL | MIN. | MAX. |
|----------------|-------------|--------|----------------|------|
| N_D | 10 | A | 0.80 | 1.00 |
| N_E | 10 | A1 | 0 | 0.05 |
| D x E BASIC | 6.00 x 6.00 | A3 | 0.25 Reference | |
| D2 MIN. / MAX. | 2.75 / 3.05 | b | 0.18 | 0.30 |
| E2 MIN. / MAX. | 2.75 / 3.05 | e | 0.50 BASIC | |
| L MIN. / MAX. | 0.30 / 0.50 | | | |

SPECIAL
NON-JEDEC

ALL DIM.
SAME EXCEPT
AS BELOW:

| | |
|----------------|-------------|
| D2 MIN. / MAX. | 4.35 / 4.65 |
| E2 MIN. / MAX. | 5.05 / 5.35 |

Source Reference: MLF2™SEF
10-0053

Ordering Information

97U877yKLF-T

Example:

XXXX y K LF-T

