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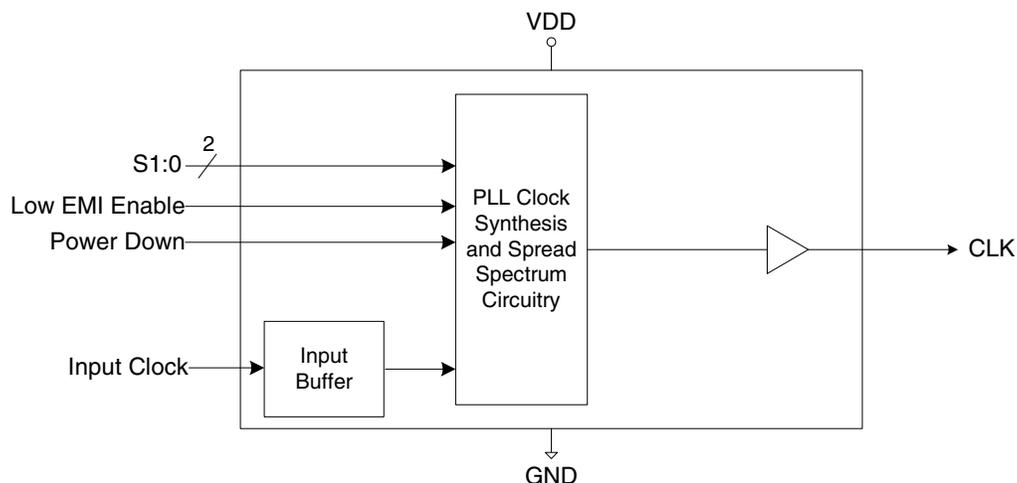
ATI LOW EMI CLOCK GENERATOR
MK1705A
Description

The MK1705A generates a low EMI output clock from a clock or crystal input. The part is designed to dither the LCD interface clock or other clocks for ATI's flat panel graphics controllers. The MK1705A uses IDT's proprietary mixture of analog and digital Phase Locked Loop (PLL) technology to synthesize the frequency. It also uses IDT's patented technique to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

The MK1705A is designed to have the output spread centered around the input frequency. Refer to the MK1704A for spreading down from the input frequency or the MK1714-0x for a crystal input and the widest selection of spread rates and multipliers.

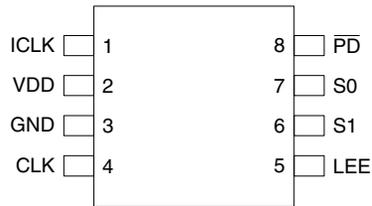
IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

Note: When changing input frequency, the LEE pin must be set low for a minimum of 10 μ S to allow the PLL to lock to the new frequency. Alternatively, the \overline{PD} pin maybe be set low while changing frequencies.

Block Diagram

Features

- 8-pin SOIC package
- Provides a spread spectrum output clock
- Supports ATI's flat panel controllers
- Accepts a clock input, provides same frequency dithered output
- Good for all VGA modes from 40 to 167 MHz
- Peak reduction by 7 dB - 14 dB typical on 3rd - 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 3.3 V or 5 V
- Advanced, low power CMOS process

Pin Assignment



8 pin (150 mil) SOIC

Output Clock Selection Table

| S1 pin 6 | S0 pin 7 | Input/Output Range pin 1/pin 4 | Frequency Spread vs. CLK |
|-------------|-------------|--------------------------------------|-----------------------------|
| 0 | 0 | 40 to 167 MHz | Center $\pm 1.25\%$ |
| 0 | 1 | 60 to 167 MHz | Center $\pm 0.5\%$ |
| 1 | 0 | Test | Test |
| 1 | 1 | 40 to 100 MHz | Center $\pm 1\%$ |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|------------------------|----------|---|
| 1 | ICLK | XI | Connect to a clock input as shown in table above. |
| 2 | VDD | Power | Connect to +3.3 V or +5 V. |
| 3 | GND | Power | Connect to ground. |
| 4 | CLK | Output | Clock output equal to input frequency. |
| 5 | LEE | Input | Low EMI enable. Turns on the spread spectrum when high. Internal pull-up. |
| 6 | S1 | Input | Frequency select 1 input. Selects input/output clock range per table above. Internal pull-up. |
| 7 | S0 | Input | Frequency select 0 input. Selects input/output clock range per table above. Internal pull-up. |
| 8 | $\overline{\text{PD}}$ | Input | Power down. Stops output low when this pin is low. Internal pull-up. |

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω .

Decoupling Capacitor

A decoupling capacitor of $0.01\mu\text{F}$ must be connected

between VDD and GND on pins 2 and 3 as close to the chip as possible.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The $0.01\mu\text{F}$ decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as

possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK1705A. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1705A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +5.5 | V |

DC Electrical Characteristics

Unless stated otherwise, VDD = 5 V, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|------------------|--------------------------|-----------|-------|-----------|-------|
| Operating Voltage | VDD | | 3.0 | | 5.5 | V |
| Supply Current | IDD | No load, 3.3V | | 20 | | mA |
| | | No load, 5V | | 15 | | mA |
| Input High Voltage | V _{IH} | Clock input | (VDD/2)+1 | VDD/2 | | V |
| Input Low Voltage | V _{IL} | Clock input | | VDD/2 | (VDD/2)-1 | V |
| Output High Voltage | V _{OH} | I _{OH} = -4 mA | VDD-0.4 | | | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | | | 0.4 | V |
| Input Capacitance | C _{IN} | S0 pin | | 7 | | pF |
| Nominal Output Impedance | Z _{OUT} | | | 20 | | Ω |
| Internal Pull-up Resistor | R _{PU} | LEE pin only | | 500 | | kΩ |

AC Electrical Characteristics

Unless stated otherwise, VDD = 5 V, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|--------------------------|------|------|------|-------|
| Input Frequency | | | 40 | | 167 | MHz |
| Input Clock Duty Cycle | | Time above VDD/2 | 20 | | 80 | % |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, Note 1 | | | 1.5 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.8 V, Note 1 | | | 1.5 | ns |
| Output Clock Duty Cycle | | Time above 1.5 V | 40 | 50 | 60 | % |
| Output Clock Frequency Variation from Mean | | LEE high | ±0.5 | | 2.5 | % |
| EMI Peak Frequency Reduction | | 3rd - 19th odd harmonics | 7 | | 14 | dB |

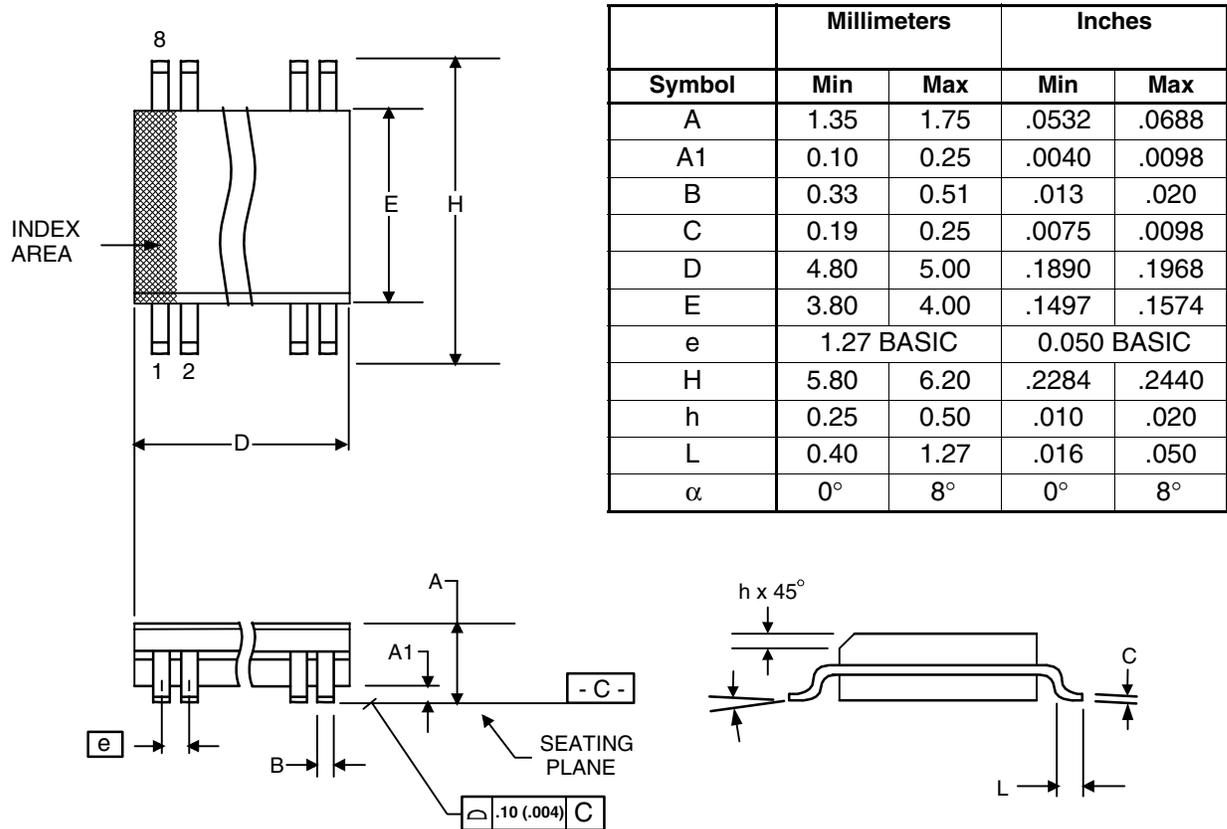
Note 1: Measured with 15 pF load.

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ _{JA} | Still air | | 150 | | °C/W |
| | θ _{JA} | 1 m/s air flow | | 140 | | °C/W |
| | θ _{JA} | 3 m/s air flow | | 120 | | °C/W |
| Thermal Resistance Junction to Case | θ _{JC} | | | 40 | | °C/W |

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|----------|--------------------|------------|-------------|
| MK1705A | MK1705A | Tubes | 8-pin SOIC | 0 to +70° C |
| MK1705ATR | MK1705A | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| MK1705ALF | MK1705AL | Tubes | 8-pin SOIC | 0 to +70° C |
| MK1705ATRLF | MK1705AL | Tape and Reel | 8-pin SOIC | 0 to +70° C |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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