阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

LOW PHASE NOISE CLOCK MULTIPLIER ICS613

Description

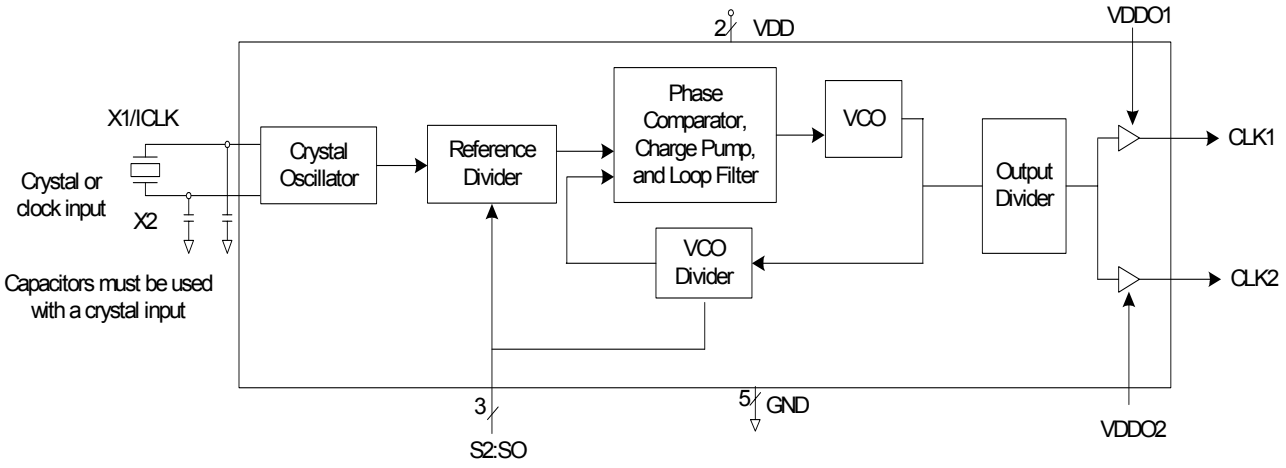
The ICS613 is a low cost, low phase noise, high performance clock synthesizer for any applications that require low phase noise and low jitter. It is IDT's lowest phase noise multiplier. Using IDT's patented analog and digital Phase Locked Loop (PLL) techniques, the chip can accept a 25 MHz crystal or clock input, and produces output clocks up to 157.5 MHz.

The chip has separate power supplies for the clock outputs, allowing each output to be run at different voltages. It also allows the core of the chip to operate at 3.3 V, while the output clocks run at either 2.5 V or 3.3 V.

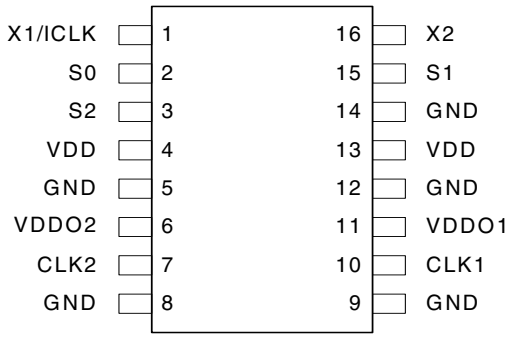
Features

- Packaged in 16 pin SOIC
- Pb (lead) free package
- Uses a fundamental 25 MHz crystal or clock
- Operating voltage of 3.3 V
- Separate output voltage supplies which can run at 2.5 V or 3.3 V
- Output clocks up to 157.5 MHz
- Low phase noise: -110 dBc/Hz at 10 kHz
- Low jitter of 36 ps (one sigma)
- Advanced, low power, sub-micron CMOS process

Block Diagram



Pin Assignment



16 Pin (150 mil) SOIC

Clock Select Table

S2	S1	S0	Input	Output (CLK1 and CLK2)
0	0	0	25	125
0	0	1	25	156.25
0	1	0	25	143.75
0	1	1	25	150
1	0	0	25	146.875
1	0	1	25	157.5
1	1	0	25	140
1	1	1	25	156.25

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI/ICLK	Input	Crystal Connection. Connect to a 25 MHz crystal or clock.
2	S0	Input	Select pin 0. Internal pull-down.
3	S2	Input	Select pin 2. Internal pull-down.
4	VDD	Power	Connect to +3.3V. Must be the same as pin 13.
5	GND	Power	Connect to ground.
6	VDDO2	Power	Output VDD for CLK2. Connect to either +2.5V or +3.3V.
7	CLK2	Output	CLK2 output. Frequency based on table above.
8	GND	Power	Connect to ground.
9	GND	Power	Connect to ground.
10	CLK1	Output	CLK1 output. Frequency based on table above.
11	VDDO1	Power	Output VDD for CLK1. Connect to either +2.5V or +3.3V.
12	GND	Power	Connect to ground.
13	VDD	Power	Connect to +3.3V. Must be the same as pin 4.
14	GND	Power	Conenct to ground.
15	S1	Input	Select pin 1. Internal pull-up.
16	X2	Input	Crystal Connection. Connect to a 25 MHz crystal. Leave unconnected for clock input.

External Component Selection

The ICS613 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between VDD and GND pairs on pins 4 and 5, pins 6 and 8, pins 11 and 9, and pins 13 and 14 as close to the ICS613 as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB traces between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Tuning Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal (C_L -6pF)*2. In this equation, C_L= crystal load capacitance in pF.

Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

Reducing Jitter and Phase Noise

For applications that only require one output, jitter and phase noise can be reduced by tying the unused VDDO to ground. This will stop the output clock low which will result in less switching noise on the active output.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS613. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V

DC Electrical Characteristics

VDD=3.3V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output Voltage	VDDO		2.375		VDD	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Input High Voltage (S2:S0)	V_{IH}		2.5			V
Input Low Voltage (S2:S0)	V_{IL}				0.5	V
Input High Voltage (ICLK)	V_{IH}		1.7			V
Input Low Voltage (ICLK)	V_{IL}				0.7	V
Operating Supply Current	IDD	No load		27		mA
Short Circuit Current	I_{OS}			±50		mA

AC Electrical Characteristics

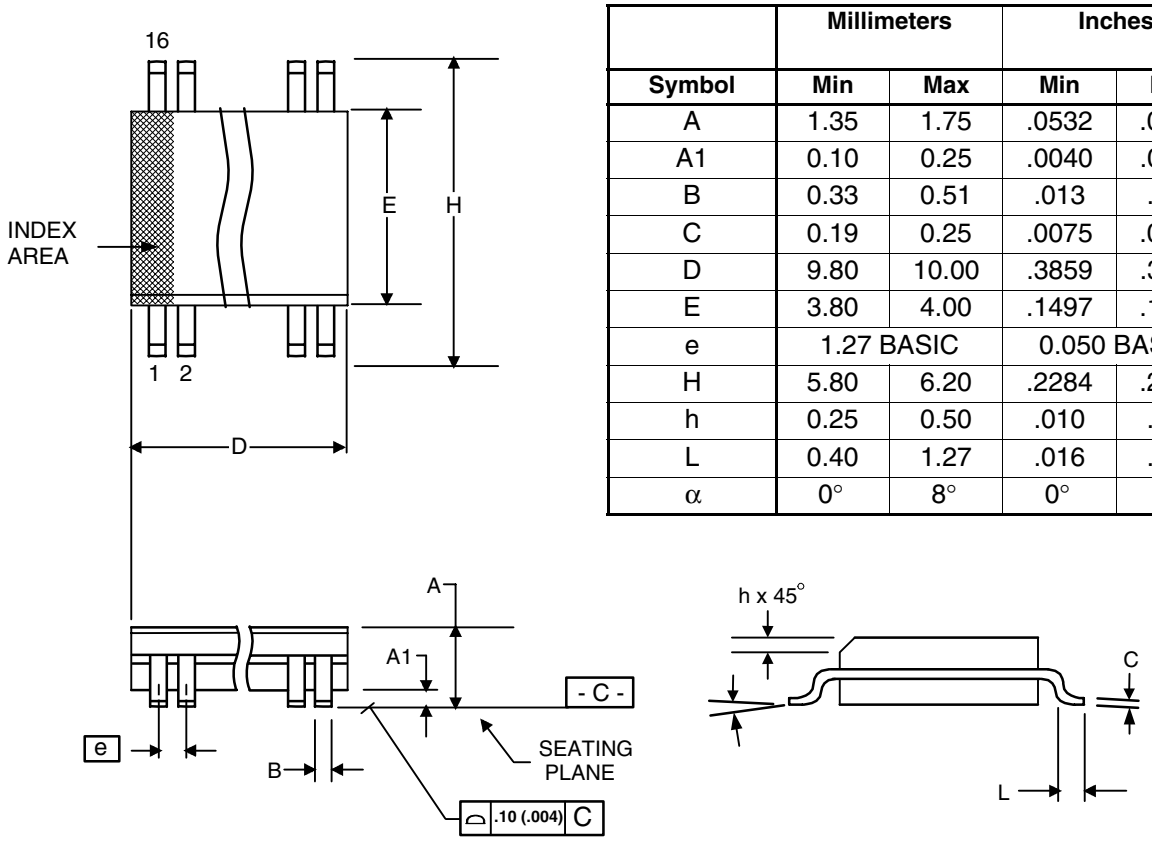
VDD = 3.3V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{in}			25		MHz
Output Frequency	f_{out}		125		157.5	MHz
Output Rise Time	t_{OR}	20% to 80%, C_L=15 pF, VDD=3.3 V		700		ps
Output Fall Time	t_{OF}	80% to 20%, C_L=15 pF, VDD=3.3 V		700		ps
Output Rise Time	t_{OR}	20% to 80%, C_L=15 pF, VDDO's=2.5 V			1.0	ns
Output Fall Time	t_{OF}	80% to 20%, C_L=15 pF, VDDO's=2.5 V			1.0	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Duty Cycle	t_D	At VDDO's/2, C_L=15 pF	45	50	55	%
Maximum Output Jitter, short term	t_J	C_L=15 pF, 125 MHz output		±30	±60	ps
Maximum one sigma jitter	t_{SJ}	C_L=15 pF, 125 MHz output		8	20	ps
Phase Noise, relative to carrier, 125 MHz		100 Hz offset		-90		dBc/Hz
Phase Noise, relative to carrier, 125 MHz		1 kHz offset		-115		dBc/Hz
Phase Noise, relative to carrier, 125 MHz		10 kHz offset		-120		dBc/Hz
Phase Noise, relative to carrier, 125 MHz		100 kHz offset		-115		dBc/Hz
Skew		VDDO1=VDDO2		0	250	ps

Package Outline and Package Dimensions (16 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
613MLF	ICS613MLF	Tubes	16 pin SOIC	0 to +70° C
613MLFT	ICS613MLF	Tape and Reel	16 pin SOIC	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
www.idt.com/go/clockhelp

Corporate Headquarters
Integrated Device Technology, Inc.
www.idt.com

www.IDT.com