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MPEG CLOCK SYNTHESIZER

ICS650-12

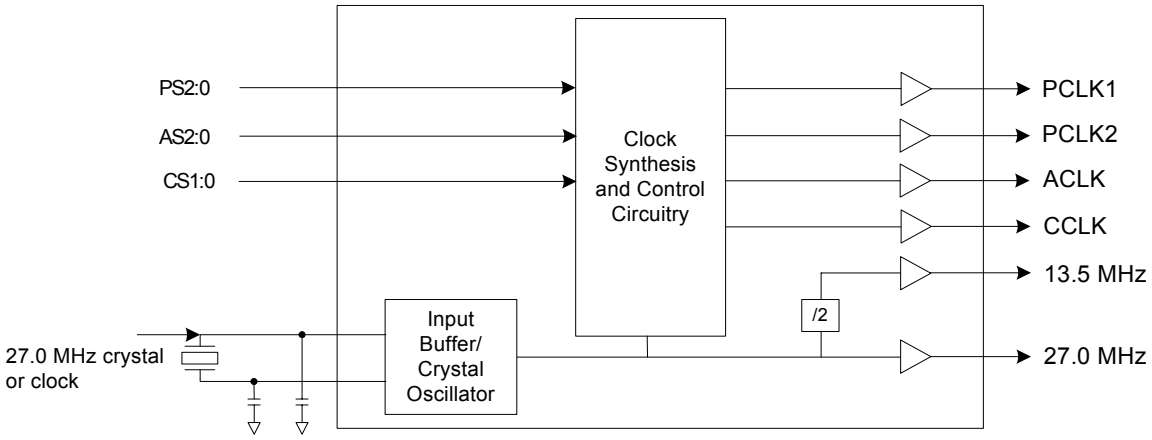
Description

The ICS650-12 is a low cost, low-jitter, high-performance clock synthesizer designed to produce fixed clock outputs of 13.5 MHz and 27.0 MHz, and four selectable clock outputs: two Processor Clocks (PCLK1) and PCLK2), an Audio Clock, and a Communications Clock (CCLK). Using analog Phase-Locked Loop (PLL) techniques, the device uses a 27.0 MHz clock or fundamental crystal to produce clocks ideal for Digital Video/MPEG-based applications.

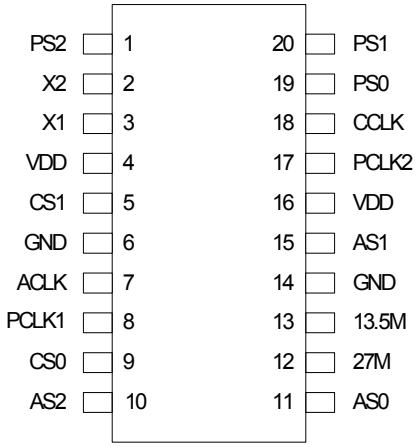
Features

- Packaged in 20-pin tiny SSOP (QSOP)
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant package
- Input frequency of 27.0 MHz
- Zero ppm synthesis error in output clocks
- Provides fixed 13.5 MHz and 27.0 MHz. Also provides two selectable processor clocks, one audio clock, and one communications clock.
- Ideal for digital video MPEG-based applications
- 3.3 V or 5.0 V operating voltage
- Entire chip powers down (when CS1=CS0=0)

Block Diagram



Pin Assignment



20-pin SSOP (QSOP)

PCLK1 and PCLK2 Select Table (in MHz)

PS2	PS1	PS0	PCLK1	PCLK2
0	0	0	108.00	54.00
0	0	1	55.00	27.5
0	1	0	66.67	33.33
0	1	1	80.00	40.00
1	0	0	54.00	27.00
1	0	1	81.00	40.5
1	1	0	50.00	25.00
1	1	1	60.00	30.00

ACLK Select Table (in MHz)

AS2	AS1	AS0	ACLK
0	0	0	12.288
0	0	1	11.2896
0	1	0	8.192
0	1	1	24.576
1	0	0	8.192
1	0	1	16.9344
1	1	0	18.432
1	1	1	11.2896

CCLK Select Table (in MHz)

CS1	CS0	CCLK
0	0	All off*
0	1	20.00
1	0	66.6666
1	1	24.576

*Note: Entire chip powers-down (outputs stop low) when CS1=CS0=0.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	PS2	Input	Processor Clock Select pin 2. See table on page 2.
2	X2	XO	Crystal connection. Connect to a 27.0 MHz crystal or leave unconnected for a clock input.
3	X1	XI	Crystal connection. Connect to a 27.0 MHz fundamental mode crystal or clock input.
4, 16	VDD	Power	Connect to +3.3 V or +5 V.
5	CS1	Input	Communications Clock Select Pin 1. See table on page 2.
6, 14	GND	Power	Connect to ground.
7	ACLK	Output	Audio Clock Output. See table on page 2.
8	PCLK1	Output	Processor Clock Output 1. See table on page 2.
9	CS0	Input	Communications Clock Select 0. See table on page 2.
10	AS2	Input	Audio Clock Select Pin 2. See table on page 2.
11	AS0	Input	Audio Clock Select Pin 0. See table on page 2.
12	27M	Output	27 MHz buffered clock output.
13	13.5M	Output	13.5 MHz clock output.
15	AS1	Input	Audio Clock Select Pin 1. See table on page 2.
17	PCLK2	Output	Processor Clock Output 2. See table on page 2.
18	CCLK	Output	Communications Clock Output. See table on page 2.
19	PS0	Input	Processor Clock Select Pin 0. See table on page 2.
20	PS1	Input	Processor Clock Select Pin 1. See table on page 2.

Key: **Input** = input with internal pull-up; **XI** and **XO** = crystal connections; **Power** = power supply connection; **Output** = output

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-12. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Conditions	Rating
Supply Voltage, VDD	Referenced to GND	7 V
All Inputs and Outputs	Referenced to GND	-0.5 V to VDD+0.5 V
Ambient Operating Temperature		0 to +70° C
Storage Temperature		-65 to +150° C
Soldering Temperature	Max. of 10 seconds	260° C

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V or 5 V**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V_{IH}		2	VDD/2		V
Input Low Voltage	V_{IL}			VDD/2	0.8	V
Output High Voltage	V_{OH}	VDD = 3.3 V, I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	VDD = 3.3 V, I_{OL} = 8 mA			0.8	V
Output High Voltage	V_{OH}, VDD = 3.3 or 5 V	I_{OH} = -8 mA	VDD-0.4			V
Operating Supply Current	I_{DD}@5 V	No Load		39		mA
Operating Supply Current	I_{DD}@5 V	No Load		22		mA
Short Circuit Current	I_{OS}, VDD = 3.3 V	Each output		±50		mA
Input Capacitance		Except X1		7		pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V or 5 V**, Ambient Temperature 0 to +70° C

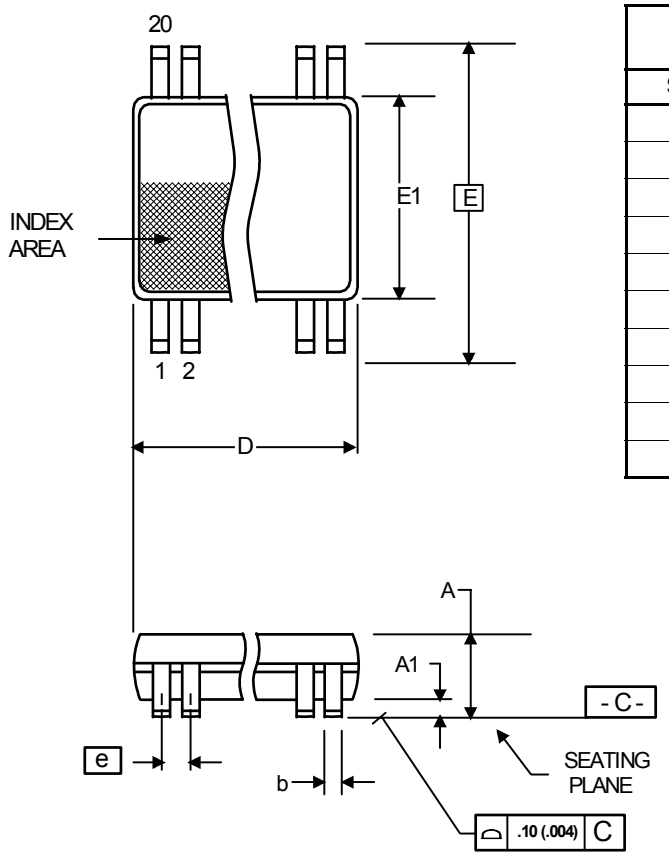
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Crystal or Clock Frequency				27		MHz
Output Clocks Accuracy (synthesis error)		All clocks		0	1	ppm
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V			1.5	ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle		At VDD/2	40	50	60	%
One Sigma Jitter, ACLK		VDD = 3.3 V		100		ps
		VDD = 5.0 V		40		ps
Absolute Clock Period Jitter		VDD = 3.3 V, except CCLK = 20 MHz		±300		ps
		VDD = 5.0 V, except CCLK = 20 MHz		±200		ps

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD and GND on pins 4 and 6, 16 and 14, and a 33Ω terminating resistor may be used on each clock output if the trace is longer than 1 inch.

Package Outline and Package Dimensions (20-pin SSOP)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	0.016	0.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650R-12LF	650R-12LF	Tubes	20-pin SSOP	0 to +70° C
650R-12LFT	650R-12LF	Tape and Reel	20-pin SSOP	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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