

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



## 3.3V ZERO DELAY CLOCK MULTIPLIER

**IDT2308A**

### FEATURES:

- Phase-Lock Loop Clock Distribution for Applications ranging from 10MHz to 133MHz operating frequency
- Distributes one clock input to two banks of four outputs
- Separate output enable for each output bank
- External feedback (FBK) pin is used to synchronize the outputs to the clock input
- Output Skew <200 ps
- Low jitter <200 ps cycle-to-cycle
- 1x, 2x, 4x output options (see table):
  - IDT2308A-1 1x
  - IDT2308A-2 1x, 2x
  - IDT2308A-3 2x, 4x
  - IDT2308A-4 2x
  - IDT2308A-1H and -2H for High Drive
- No external RC network required
- Operates at 3.3V VDD
- Available in SOIC and TSSOP packages

### DESCRIPTION:

The IDT2308A is a high-speed phase-lock loop (PLL) clock multiplier. It is designed to address high-speed clock distribution and multiplication applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

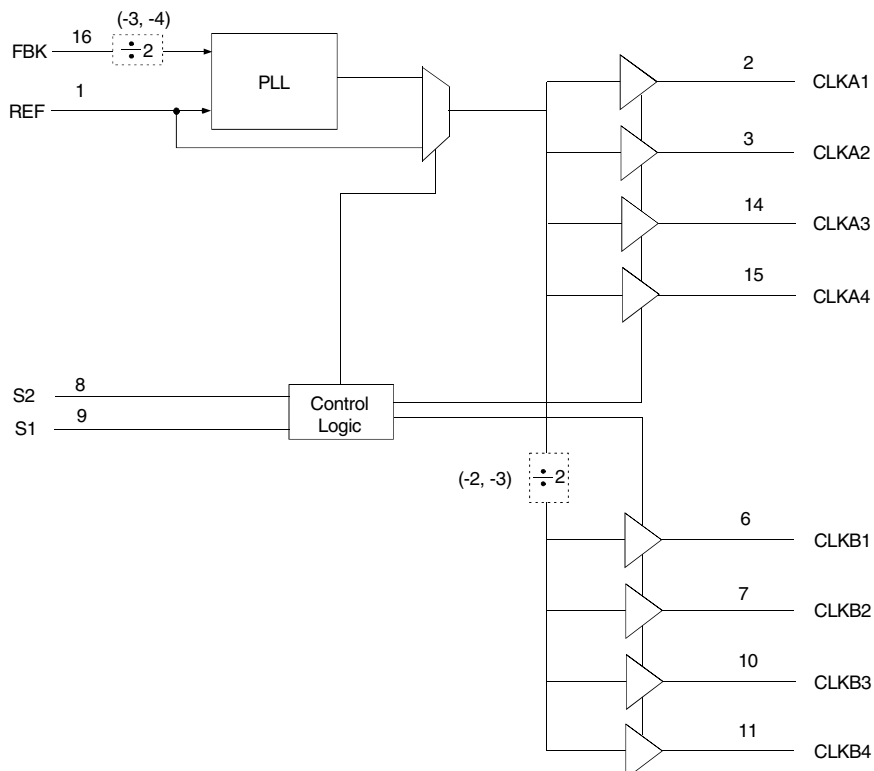
The IDT2308A has two banks of four outputs each that are controlled via two select addresses. By proper selection of input addresses, both banks can be put in tri-state mode. In test mode, the PLL is turned off, and the input clock directly drives the outputs for system testing purposes. In the absence of an input clock, the IDT2308A enters power down. In this mode, the device will draw less than 12µA for Commercial Temperature range and less than 25µA for Industrial temperature range, and the outputs are tri-stated.

The IDT2308A is available in six unique configurations for both pre-scaling and multiplication of the Input REF Clock. (See available options table.)

The PLL is closed externally to provide more flexibility by allowing the user to control the delay between the input clock and the outputs.

The IDT2308A is characterized for both Industrial and Commercial operation.

### FUNCTIONAL BLOCK DIAGRAM

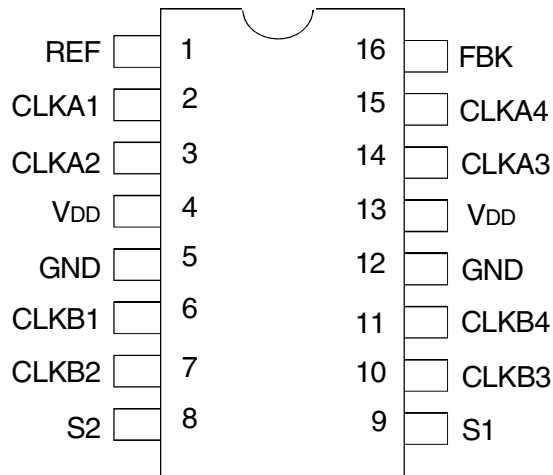


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

**COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES**

**AUGUST 2012**

## PIN CONFIGURATION



SOIC/ TSSOP  
TOP VIEW

## PIN DESCRIPTION

	Pin Number	Functional Description
REF	1	Input Reference Clock, 5 Volt Tolerant Input
CLKA1 <sup>(1)</sup>	2	Clock Output for Bank A
CLKA2 <sup>(1)</sup>	3	Clock Output for Bank A
VDD	4	3.3V Supply
GND	5	Ground
CLKB1 <sup>(1)</sup>	6	Clock Output for Bank B
CLKB2 <sup>(1)</sup>	7	Clock Output for Bank B
S2 <sup>(2)</sup>	8	Select Input, Bit 2
S1 <sup>(2)</sup>	9	Select Input, Bit 1
CLKB3 <sup>(1)</sup>	10	Clock Output for Bank B
CLKB4 <sup>(1)</sup>	11	Clock Output for Bank B
GND	12	Ground
VDD	13	3.3V Supply
CLKA3 <sup>(1)</sup>	14	Clock Output for Bank A
CLKA4 <sup>(1)</sup>	15	Clock Output for Bank A
FBK	16	PLL Feedback Input

### NOTES:

1. Weak pull down on all outputs.
2. Weak pull ups on these inputs.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Max.	Unit
VDD	Supply Voltage Range	-0.5 to +4.6	V
V <sub>I</sub> <sup>(2)</sup>	Input Voltage Range (REF)	-0.5 to +5.5	V
V <sub>I</sub>	Input Voltage Range (except REF)	-0.5 to VDD+0.5	V
I <sub>IK</sub> (V <sub>I</sub> < 0)	Input Clamp Current	-50	mA
I <sub>O</sub> (V <sub>O</sub> = 0 to VDD)	Continuous Output Current	±50	mA
VDD or GND	Continuous Current	±100	mA
T <sub>A</sub> = 55°C (in still air) <sup>(3)</sup>	Maximum Power Dissipation	0.7	W
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
Operating Temperature	Commercial Temperature Range	0 to +70	°C
Operating Temperature	Industrial Temperature Range	-40 to +85	°C

### NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## APPLICATIONS:

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay Designs

**FUNCTION TABLE<sup>(1)</sup> SELECT INPUT DECODING**

S2	S1	CLK A	CLK B	Output Source	PLL Shut Down
L	L	Tri-State	Tri-State	PLL	Y
L	H	Driven	Tri-State	PLL	N
H	L	Driven	Driven	REF	Y
H	H	Driven	Driven	PLL	N

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level

**AVAILABLE OPTIONS FOR IDT2308A**

Device	Feedback From	Bank A Frequency	Bank B Frequency
IDT2308A-1	Bank A or Bank B	Reference	Reference
IDT2308A-1H	Bank A or Bank B	Reference	Reference
IDT2308A-2	Bank A	Reference	Reference/2
IDT2308A-2	Bank B	2 x Reference	Reference
IDT2308A-2H	Bank A	Reference	Reference/2
IDT2308A-2H	Bank B	2 x Reference	Reference
IDT2308A-3	Bank A	2 x Reference	Reference or $\overline{\text{Reference}}$ <sup>(1)</sup>
IDT2308A-3	Bank B	4 x Reference	2 x Reference
IDT2308A-4	Bank A or Bank B	2 x Reference	2 x Reference

**NOTE:**

- Output phase is indeterminant (0° or 180° from input clock).

**ZERO DELAY AND SKEW CONTROL**

To close the feedback loop of the IDT2308A, the FBK pin can be driven from any of the eight available output pins. The output driving the FBK pin will be driving a total load of 7pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. Ensure the outputs are loaded equally, for zero output-output skew.

### OPERATING CONDITIONS-COMMERCIAL

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		3	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)		0	70	°C
C <sub>L</sub>	Load Capacitance below 100MHz		—	30	pF
	Load Capacitance from 100MHz to 133MHz		—	15	pF
C <sub>IN</sub>	Input Capacitance <sup>(1)</sup>		—	7	pF

**NOTE:**

1. Applies to both REF and FBK.

### DC ELECTRICAL CHARACTERISTICS-COMMERCIAL

Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit	
V <sub>IL</sub>	Input LOW Voltage Level		—	—	0.8	V	
V <sub>IH</sub>	Input HIGH Voltage Level		2	—	—	V	
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0V	—	—	50	μA	
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = V <sub>DD</sub>	—	—	100	μA	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 8mA (-1, -2, -3, -4) I <sub>OL</sub> = 12mA (-1H, -2H)	—	—	0.4	V	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -8mA (-1, -2, -3, -4) I <sub>OH</sub> = -12mA (-1H, -2H)	2.4	—	—	V	
I <sub>DD_PD</sub>	Power Down Current	REF = 0MHz (S2 = S1 = H)	—	—	12	μA	
I <sub>DD</sub>	Supply Current	Unloaded Outputs Select Inputs at V <sub>DD</sub> or GND	100MHz CLKA (-1, -2, -3, -4)	—	—	45	mA
			100MHz CLKA (-1H, -2H)	—	—	70	
			66MHz CLKA (-1, -2, -3, -4)	—	—	32	
			66MHz CLKA (-1H, -2H)	—	—	50	
			33MHz CLKA (-1, -2, -3, -4)	—	—	18	
			33MHz CLKA (-1H, -2H)	—	—	30	

## SWITCHING CHARACTERISTICS - COMMERCIAL

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t <sub>1</sub>	Output Frequency	30pF Load, all devices	10	—	100	MHz
t <sub>1</sub>	Output Frequency	20pF Load, -1H, -2H Devices	10	—	133.3	MHz
t <sub>1</sub>	Output Frequency	15pF Load, -1, -2, -3, -4 devices	10	—	133.3	MHz
	Duty Cycle = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -2H)	Measured at 1.4V, F <sub>OUT</sub> = 66.66MHz 30pF Load	40	50	60	%
	Duty Cycle = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -2H)	Measured at 1.4V, F <sub>OUT</sub> = 50MHz 15pF Load	45	50	55	%
t <sub>3</sub>	Rise Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 30pF Load	—	—	2.2	ns
t <sub>3</sub>	Rise Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 15pF Load	—	—	1.5	ns
t <sub>3</sub>	Rise Time (-1H, -2H)	Measured between 0.8V and 2V, 30pF Load	—	—	1.5	ns
t <sub>4</sub>	Fall Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 30pF Load	—	—	2.2	ns
t <sub>4</sub>	Fall Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 15pF Load	—	—	1.5	ns
t <sub>4</sub>	Fall Time (-1H)	Measured between 0.8V and 2V, 30pF Load	—	—	1.25	ns
t <sub>5</sub>	Output to Output Skew on same Bank (-1, -2, -3, -4)	All outputs equally loaded	—	—	200	ps
	Output to Output Skew (-1H, -2H)	All outputs equally loaded	—	—	200	ps
	Output Bank A to Output Bank B (-1, -4, -2H)	All outputs equally loaded	—	—	200	ps
	Output Bank A to Output Bank B Skew (-2, -3)	All outputs equally loaded	—	—	400	ps
t <sub>6</sub>	Delay, REF Rising Edge to FBK Rising Edge	Measured at V <sub>DD</sub> /2	—	0	±250	ps
t <sub>7</sub>	Device to Device Skew	Measured at V <sub>DD</sub> /2 on the FBK pins of devices	—	0	700	ps
t <sub>8</sub>	Output Slew Rate	Measured between 0.8V and 2V on -1H, -2H device using Test Circuit 2	1	—	—	V/ns
t <sub>J</sub>	Cycle to Cycle Jitter (-1, -1H, -4)	Measured at 66.67 MHz, loaded outputs, 15pF Load	—	—	200	ps
		Measured at 66.67 MHz, loaded outputs, 30pF Load	—	—	200	
		Measured at 133.3 MHz, loaded outputs, 15pF Load	—	—	100	
t <sub>J</sub>	Cycle to Cycle Jitter (-2, -2H, -3)	Measured at 66.67 MHz, loaded outputs, 30pF Load	—	—	400	ps
		Measured at 66.67 MHz, loaded outputs, 15pF Load	—	—	400	
t <sub>LOCK</sub>	PLL Lock Time	Stable Power Supply, valid clocks presented on REF and FBK pins	—	—	1	ms

### OPERATING CONDITIONS-INDUSTRIAL

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		3	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)		-40	+85	°C
C <sub>L</sub>	Load Capacitance below 100MHz		—	30	pF
	Load Capacitance from 100MHz to 133MHz		—	15	pF
C <sub>IN</sub>	Input Capacitance <sup>(1)</sup>		—	7	pF

**NOTE:**

1. Applies to both REF and FBK.

### DC ELECTRICAL CHARACTERISTICS-INDUSTRIAL

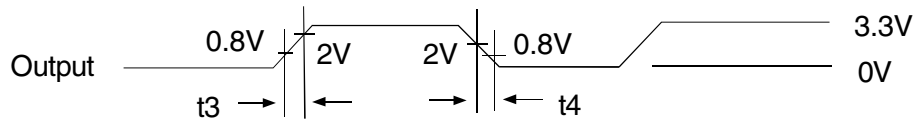
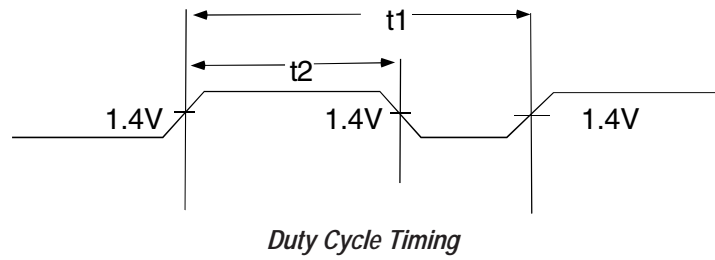
Symbol	Parameter	Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit	
V <sub>IL</sub>	Input LOW Voltage Level		—	—	0.8	V	
V <sub>IH</sub>	Input HIGH Voltage Level		2	—	—	V	
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0V	—	—	50	μA	
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = V <sub>DD</sub>	—	—	100	μA	
V <sub>OL</sub>	Output LOW Voltage	I <sub>oL</sub> = 8mA (-1, -2, -3, -4) I <sub>oL</sub> = 12mA (-1H, -2H)	—	—	0.4	V	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>oH</sub> = -8mA (-1, -2, -3, -4) I <sub>oH</sub> = -12mA (-1H, -2H)	2.4	—	—	V	
I <sub>DD_PD</sub>	Power Down Current	REF = 0MHz (S2 = S1 = H)	—	—	25	μA	
I <sub>DD</sub>	Supply Current	Unloaded Outputs Select Inputs at V <sub>DD</sub> or GND	100MHz CLKA (-1, -2, -3, -4)	—	—	45	mA
			100MHz CLKA (-1H, -2H)	—	—	70	
			66MHz CLKA (-1, -2, -3, -4)	—	—	32	
			66MHz CLKA (-1H, -2H)	—	—	50	
			33MHz CLKA (-1, -2, -3, -4)	—	—	18	
			33MHz CLKA (-1H, -2H)	—	—	30	

**SWITCHING CHARACTERISTICS - INDUSTRIAL**

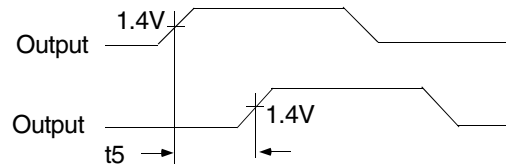
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t <sub>i</sub>	Output Frequency	30pF Load, all devices	10	—	100	MHz
t <sub>i</sub>	Output Frequency	20pF Load, -1H, -2H Devices	10	—	133.3	MHz
t <sub>i</sub>	Output Frequency	15pF Load, -1, -2, -3, -4 devices	10	—	133.3	MHz
	Duty Cycle = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -2H)	Measured at 1.4V, F <sub>OUT</sub> = 66.66MHz 30pF Load	40	50	60	%
	Duty Cycle = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -2H)	Measured at 1.4V, F <sub>OUT</sub> = 50MHz 15pF Load	45	50	55	%
t <sub>r</sub>	Rise Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 30pF Load	—	—	2.2	ns
t <sub>r</sub>	Rise Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 15pF Load	—	—	1.5	ns
t <sub>r</sub>	Rise Time (-1H, -2H)	Measured between 0.8V and 2V, 30pF Load	—	—	1.5	ns
t <sub>f</sub>	Fall Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 30pF Load	—	—	2.2	ns
t <sub>f</sub>	Fall Time (-1, -2, -3, -4)	Measured between 0.8V and 2V, 15pF Load	—	—	1.5	ns
t <sub>f</sub>	Fall Time (-1H)	Measured between 0.8V and 2V, 30pF Load	—	—	1.25	ns
t <sub>s</sub>	Output to Output Skew on same Bank (-1, -2, -3, -4)	All outputs equally loaded	—	—	200	ps
	Output to Output Skew (-1H, -2H)	All outputs equally loaded	—	—	200	ps
	Output Bank A to Output Bank B (-1, -4, -2H)	All outputs equally loaded	—	—	200	ps
	Output Bank A to Output Bank B Skew (-2, -3)	All outputs equally loaded	—	—	400	ps
t <sub>d</sub>	Delay, REF Rising Edge to FBK Rising Edge	Measured at V <sub>DD</sub> /2	—	0	±250	ps
t <sub>r</sub>	Device to Device Skew	Measured at V <sub>DD</sub> /2 on the FBK pins of devices	—	0	700	ps
t <sub>s</sub>	Output Slew Rate	Measured between 0.8V and 2V on -1H, -2H device using Test Circuit 2	1	—	—	V/ns
∫	Cycle to Cycle Jitter (-1, -1H, -4)	Measured at 66.67 MHz, loaded outputs, 15pF Load	—	—	200	ps
		Measured at 66.67 MHz, loaded outputs, 30pF Load	—	—	200	
		Measured at 133.3 MHz, loaded outputs, 15pF Load	—	—	100	
∫	Cycle to Cycle Jitter (-2, -2H, -3)	Measured at 66.67 MHz, loaded outputs, 30pF Load	—	—	400	ps
		Measured at 66.67 MHz, loaded outputs, 15pF Load	—	—	400	
t <sub>LOCK</sub>	PLL Lock Time	Stable Power Supply, valid clocks presented on REF and FBK pins	—	—	1	ms



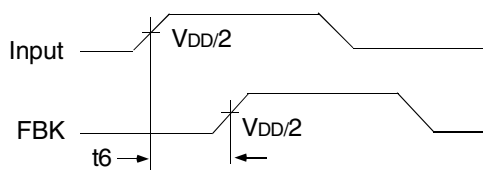
## SWITCHING WAVEFORMS



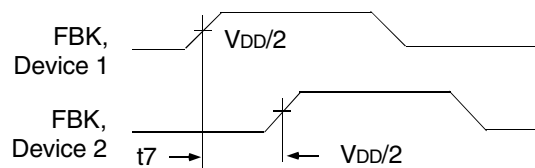
*All Outputs Rise/Fall Time*



*Output to Output Skew*



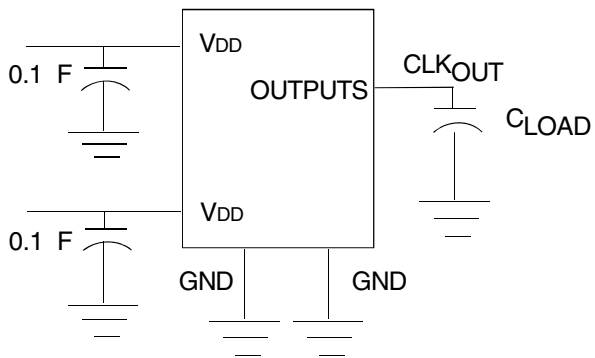
*Input to Output Propagation Delay*



*Device to Device Skew*

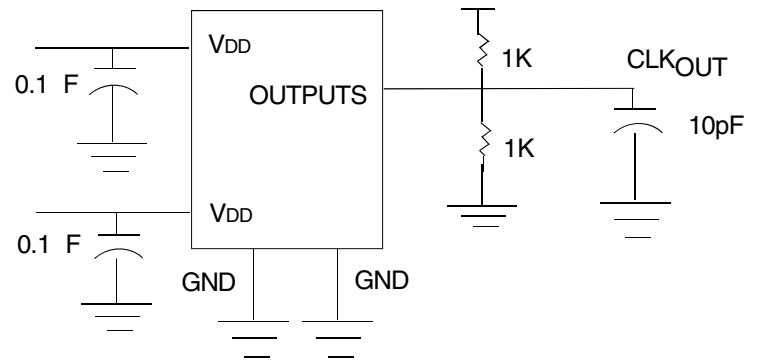
## TEST CIRCUITS

TEST CIRCUIT 1



Test Circuit for all Parameters Except  $t_8$

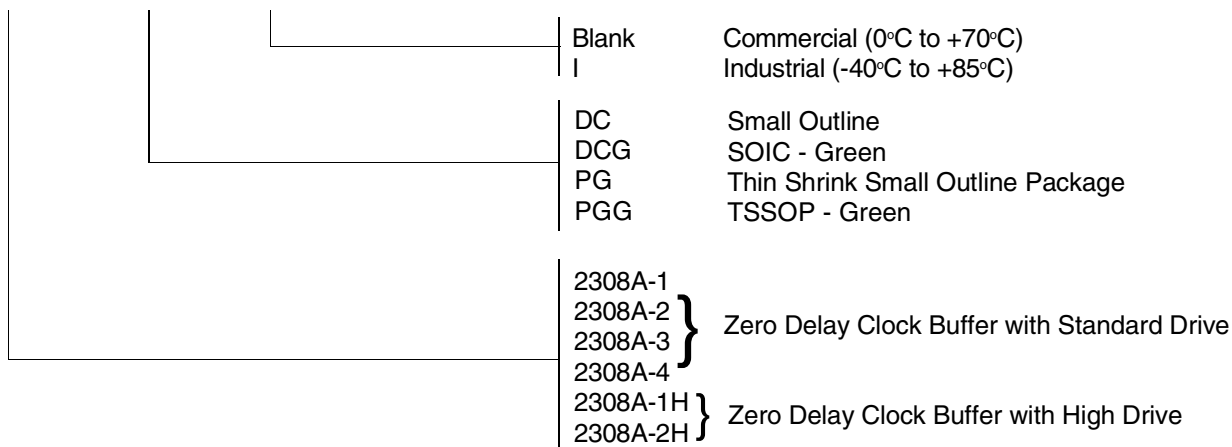
TEST CIRCUIT 2



Test Circuit for  $t_8$ , Output Slew Rate On -1H and -2H Devices

**ORDERING INFORMATION**

IDT XXXXX XX X  
 Device Type Package Process



Ordering Code	Package Type	Operating Range
IDT2308A-1DCG	16-Pin SOIC	Commercial
IDT2308A-1DCGI	16-Pin SOIC	Industrial
IDT2308A-1HDCG	16-Pin SOIC	Commercial
IDT2308A-1HDCGI	16-Pin SOIC	Industrial
IDT2308A-1HPG	16-Pin TSSOP	Commercial
IDT2308A-1HPGG	16-Pin TSSOP	Commercial
IDT2308A-1HPGGI	16-Pin TSSOP	Industrial
IDT2308A-1HPGI	16-Pin TSSOP	Industrial
IDT2308A-2DCG	16-Pin SOIC	Commercial
IDT2308A-2DCGI	16-Pin SOIC	Industrial
IDT2308A-2HDCG	16-Pin SOIC	Commercial
IDT2308A-2HDCGI	16-Pin SOIC	Industrial
IDT2308A-3DCG	16-Pin SOIC	Commercial
IDT2308A-3DCGI	16-Pin SOIC	Industrial
IDT2308A-4DCG	16-Pin SOIC	Commercial
IDT2308A-4DCGI	16-Pin SOIC	Industrial



**CORPORATE HEADQUARTERS**  
 6024 Silver Creek Valley Road  
 San Jose, CA 95138

**for SALES:**  
 800-345-7015 or 408-284-8200  
 fax: 408-284-2775  
 www.idt.com

**for Tech Support:**  
 clockhelp@idt.com