

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



3.3V PHASE-LOCK LOOP CLOCK DRIVER ZERO DELAY BUFFER

IDTCSP2510D

FEATURES:

- Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications
- Distributes one clock input to one bank of ten outputs
- Output enable bank control
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal
- No external RC network required for PLL loop stability
- Operates at 3.3V V_{DD}
- t_{pd} Phase Error at 166MHz: < ±150ps
- Jitter (peak-to-peak) at 166MHz: < ±75ps @ 166MHz
- Spread Spectrum Compatible
- Operating frequency 50MHz to 175MHz
- Available in 24-Pin TSSOP package

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

DESCRIPTION:

The CSP2510D is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CSP2510D operates at 3.3V.

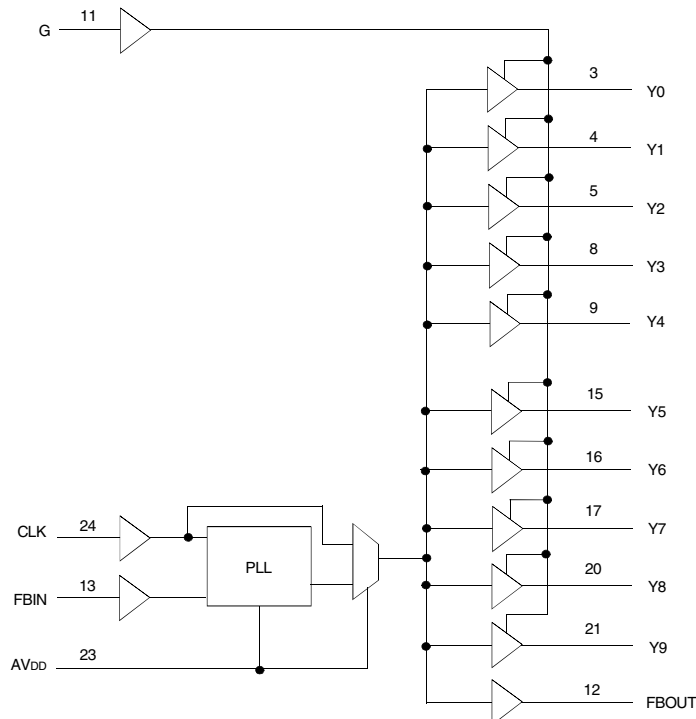
One bank of ten outputs provide low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the control G input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CSP2510D does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CSP2510D requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for the test purposes by strapping AV_{DD} to ground.

The CSP2510D is specified for operation from 0°C to +85°C. This device is also available (on special order) in Industrial temperature range (-40°C to +85°C). See ordering information for details.

FUNCTIONAL BLOCK DIAGRAM

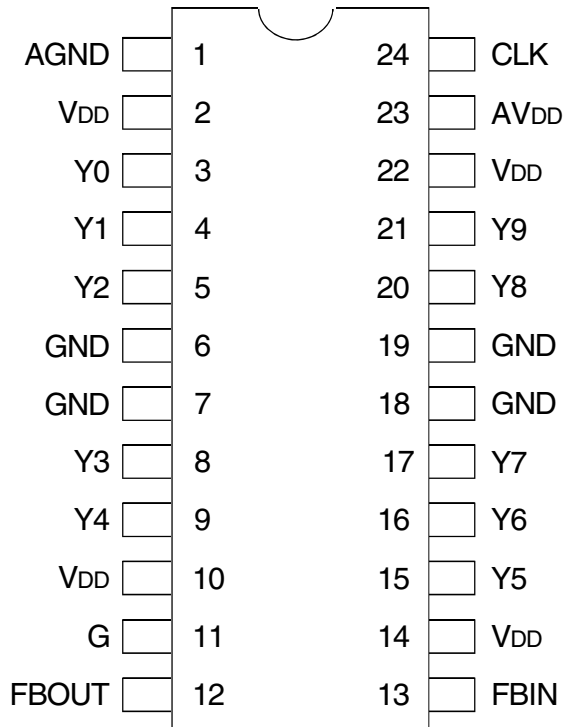


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

0°C TO 85°C TEMPERATURE RANGE

OCTOBER 2001

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Max	Unit
V _{DD}	Supply Voltage Range	-0.5 to +4.6	V
V _I ⁽¹⁾	Input Voltage Range	-0.5 to +6.5	V
V _O ^(1,2)	Voltage range applied to any output in the high or low state	-0.5 to V _{DD} + 0.5	V
I _{IK} (V _I < 0)	Input clamp current	-50	mA
I _{OK} (V _O < 0 or V _O > V _{DD})	Terminal Voltage with Respect to GND (inputs V _{IH} 2.5, V _{IL} 2.5)	±50	mA
I _O (V _O = 0 to V _{DD})	Continuous Output Current	±50	mA
V _{DD} or GND	Continuous Current	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _J	Junction Temperature	+150	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE

Parameter	Description	Min.	Typ.	Max.	Unit
C _{IN}	Input Capacitance V _I = V _{DD} or GND	—	5	—	pF
C _O	Output Capacitance V _O = V _{DD} or GND	—	6	—	pF
C _L	Load Capacitance	—	30	—	pF

NOTE:

- Unused inputs must be held HIGH or LOW to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min.	Max.	Unit
V _{DD} , AV _{DD}	Power Supply Voltage	3	3.6	V
T _A	Operating Free-Air Temperature	0	+85	°C

PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CSP2510D clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs Y(0:9). When G is low, outputs Y(0:9) are disabled to a logic-low state. When G is high, all outputs Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
Y (0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by de-asserting the G control input.
AVDD	23	Power	Analog power supply. AVDD provides the power reference for the analog circuitry. In addition, AVDD can be used to bypass the PLL for test purposes. When AVDD is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
VDD	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

STATIC FUNCTION TABLE (AVDD = 0V)

Inputs		Outputs	
G	CLK	Y (0:9)	FBOUT
L	L	L	L
L	H	L	H
H	H	H	H
H	L	L	L
H	running	running	running

DYNAMIC FUNCTION TABLE (AVDD = 3.3V)

Inputs		Outputs	
G	CLK	Y (0:9)	FBOUT
X	L	L	L
L	running	L	running in phase with CLK
L	H	L	H
H	running	running in phase with CLK	running in phase with CLK
H	H	H	H

DC ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE⁽¹⁾

Symbol	Description	Test Conditions	V _{DD}	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IK}	Input Clamp Voltage	I _I = -18mA	3V	—	—	-1.2	V
V _{IH}	Input HIGH Level		—	2	—	—	V
V _{IL}	Input LOW Level		—	—	—	0.8	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100μA	Min. to Max.	V _{DD} - 0.2	—	—	V
		I _{OH} = -12mA	3V	2.1	—	—	
		I _{OH} = -6mA	3V	2.4	—	—	
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA	Min. to Max.	—	—	0.2	V
		I _{OL} = 12mA	3V	—	—	0.8	
		I _{OL} = 6mA	3V	—	—	0.55	
I _I	Input Current	V _I = V _{DD} or GND	3.6V	—	—	±5	μA
I _{DD}	Supply Current	V _I = V _{DD} or GND, AV _{DD} = GND, I _o = 0, Outputs: LOW or HIGH	3.6V	—	—	10	μA
ΔI _{DD}	Change in Supply Current	One input at V _{DD} - 0.6V, other inputs at V _{DD} or GND	3.3V to 3.6V	—	—	500	μA
CPD	Power Dissipation Capacitance		3.6V	—	10	14	pF
I _{DDA} ⁽³⁾	AV _{DD} Power Supply Current		AV _{DD} = 3.3V	—	10	—	mA

NOTES:

- For Industrial devices, operating free-air temperature = -40°C to +85°C.
- For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
- For I_{DD} of AV_{DD}, see TYPICAL CHARACTERISTICS.

TIMING REQUIREMENTS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE⁽¹⁾

		Min.	Max.	Unit
f _{CLK}	Clock frequency	50	175	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time ⁽²⁾	—	1	ms

NOTES:

- For Industrial devices, operating free-air temperature = -40°C to +85°C.
- Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

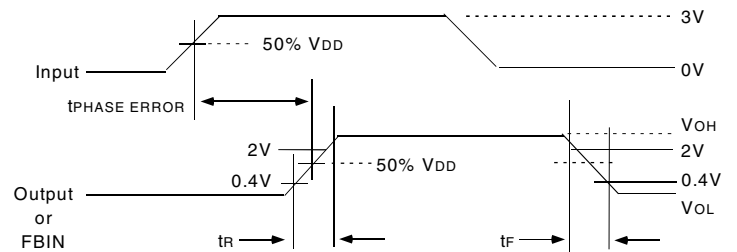
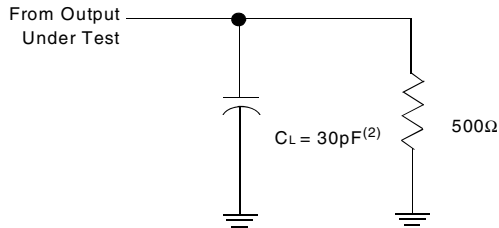
SWITCHING CHARACTERISTICS OVER OPERATING RANGE OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, $C_L = 30\text{pF}^{(1)}$

Parameter ⁽²⁾	From (Input)	To (Output)	$V_{DD} = 3.3V \pm 0.3V$			Unit
			Min.	Typ.	Max.	
t _{PHASE error}	100MHz < CLK↑ < 166MHz	FBIN↑	-150	—	150	ps
t _{PHASE error-jitter} ⁽³⁾	CLK↑ = 166MHz	FBIN↑	-50	—	50	ps
t _{SK(o)} ⁽⁴⁾	Any Y (166MHz)	Any Y	—	—	150	ps
Jitter (cycle-cycle) (peak-to-peak)	CLK = 166MHz	Any Y or FBOUT	-75	—	75	ps
Duty cycle reference ⁽⁵⁾	CLK = 166MHz	Any Y or FBOUT	45	—	55	%
t _R		Any Y or FBOUT	0.8	—	2.1	ns
t _F		Any Y or FBOUT	0.8	—	2.5	ns

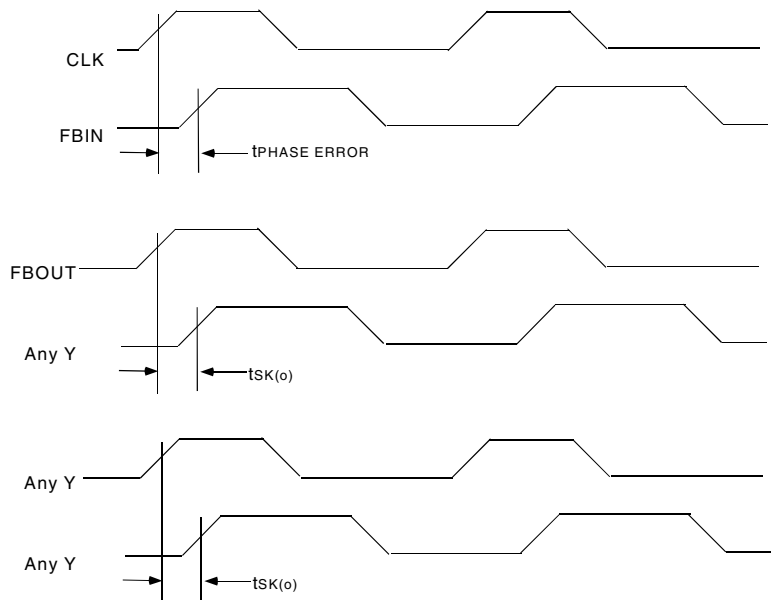
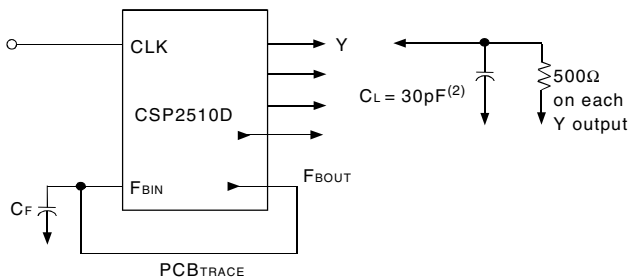
NOTES:

1. For Industrial devices, operating free-air temperature = -40°C to +85°C. See PARAMETER MEASUREMENT INFORMATION.
2. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
3. Phase error does not include jitter.
4. The t_{SK(o)} specification is only valid for equal loading of all outputs.
5. See TYPICAL CHARACTERISTICS.

PARAMETER MEASUREMENT INFORMATION⁽¹⁾



Load Circuit and Voltage Waveforms



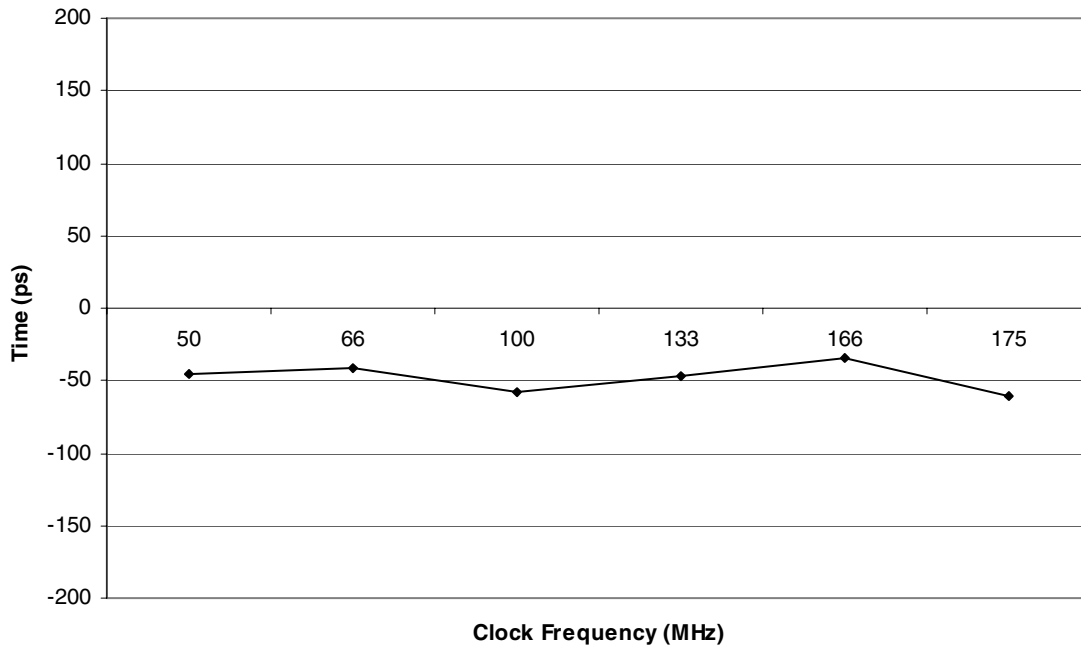
Phase ERROR and Skew Calculations^(3,4)

NOTES:

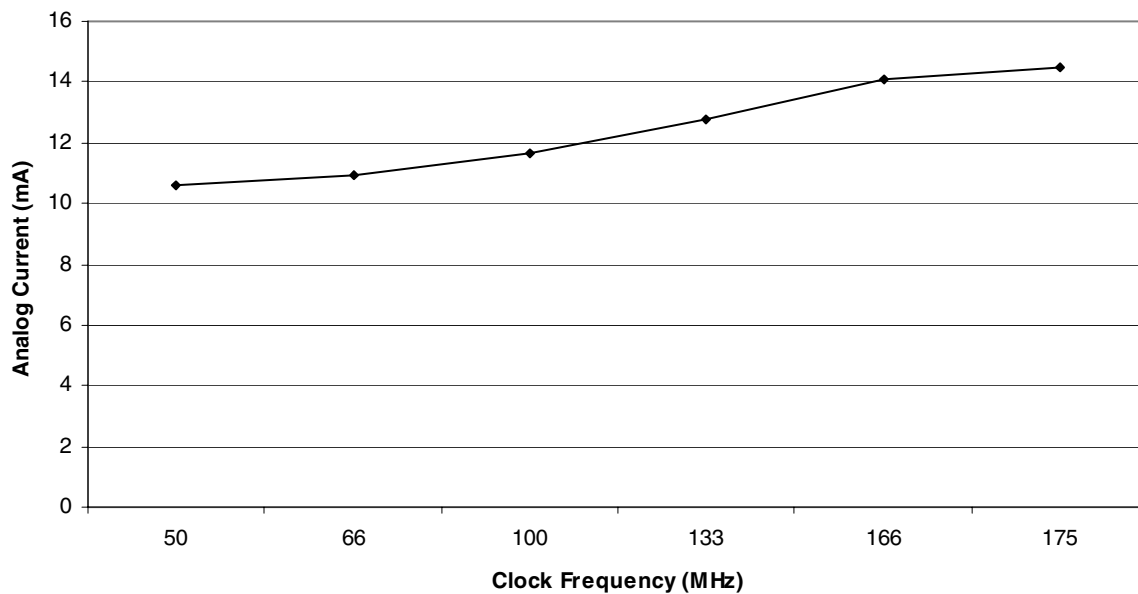
1. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 100MHz Z_O = 50Ω, t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
2. C_L includes probe and jig capacitance.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y and FBOUT. $C_F = C_L - C_{FBIN} - C_{PCBTRACE}$; C_{FBIN} ≅ 6pF.

TYPICAL CHARACTERISTICS

Phase Error vs Clock Frequency
AVDD and VDD = 3.3V
Ta = 25C

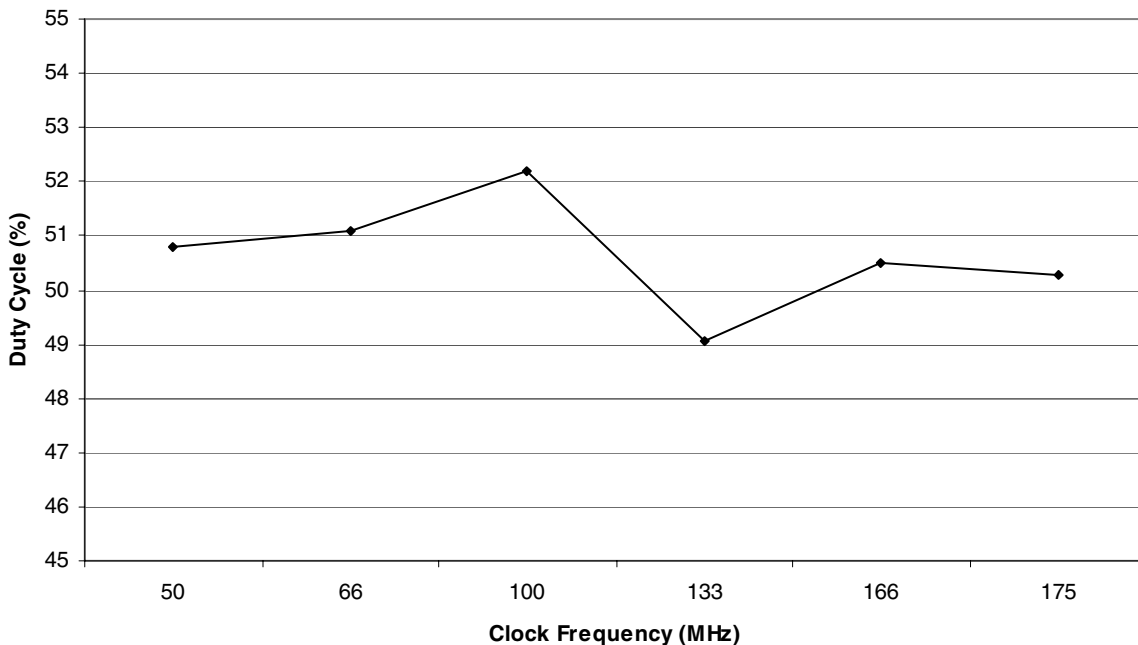


Analog Supply Current vs Clock Frequency
AVDD and VDD = 3.3V
Ta = 25C

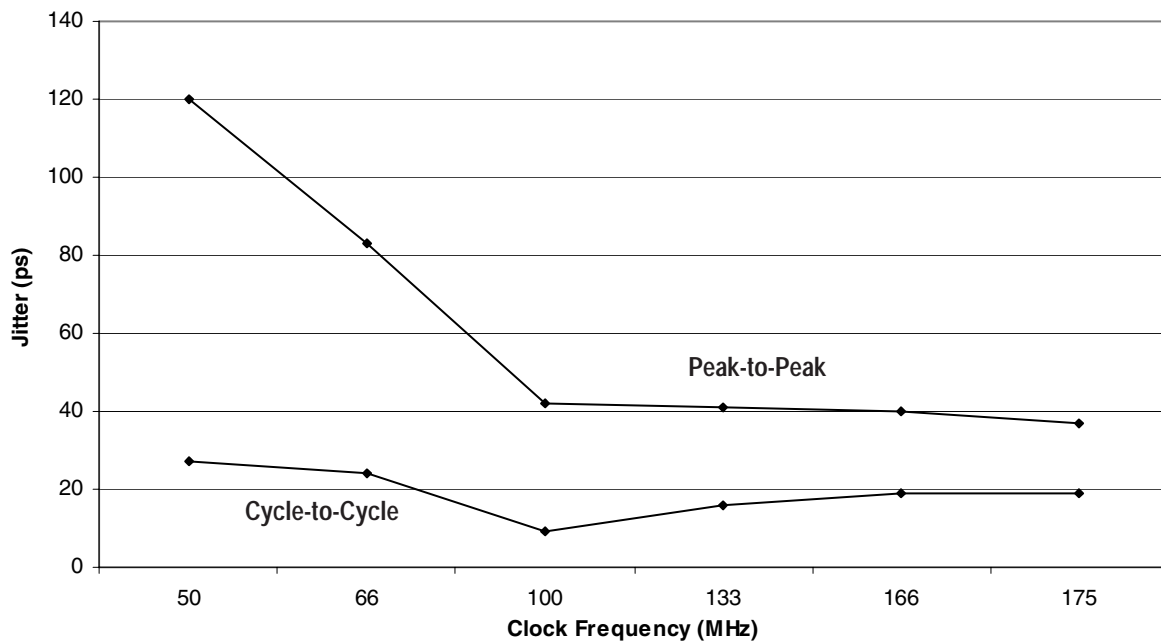


TYPICAL CHARACTERISTICS (CONT.)

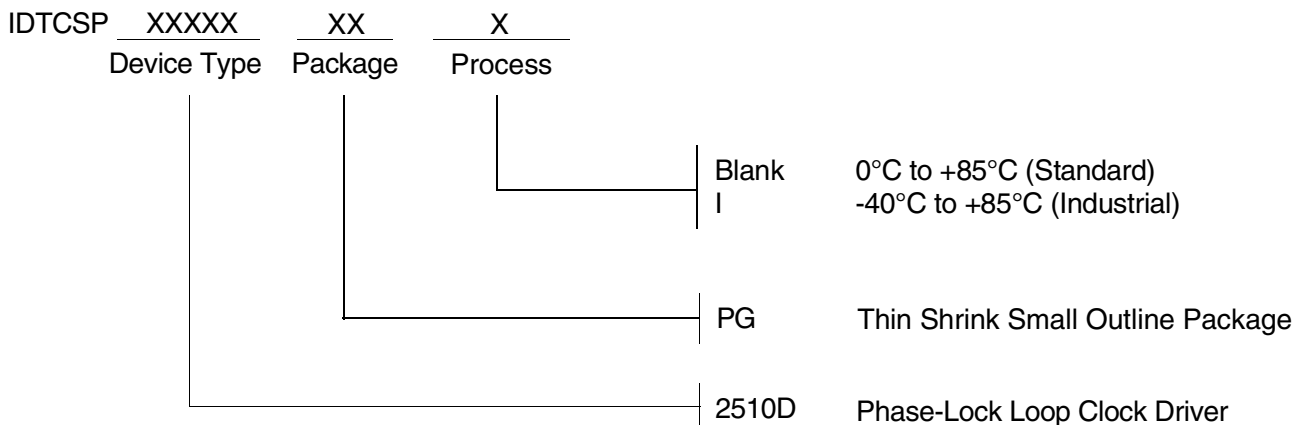
Output Duty Cycle vs Clock Frequency
AVDD and VDD = 3.3V
Ta = 25C



Jitter vs Clock Frequency
AVDD and VDD = 3.3V
Ta = 25C



ORDERING INFORMATION



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com