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LOW PHASE NOISE T1/E1 CLOCK GENERATOR MK1581-01

Description

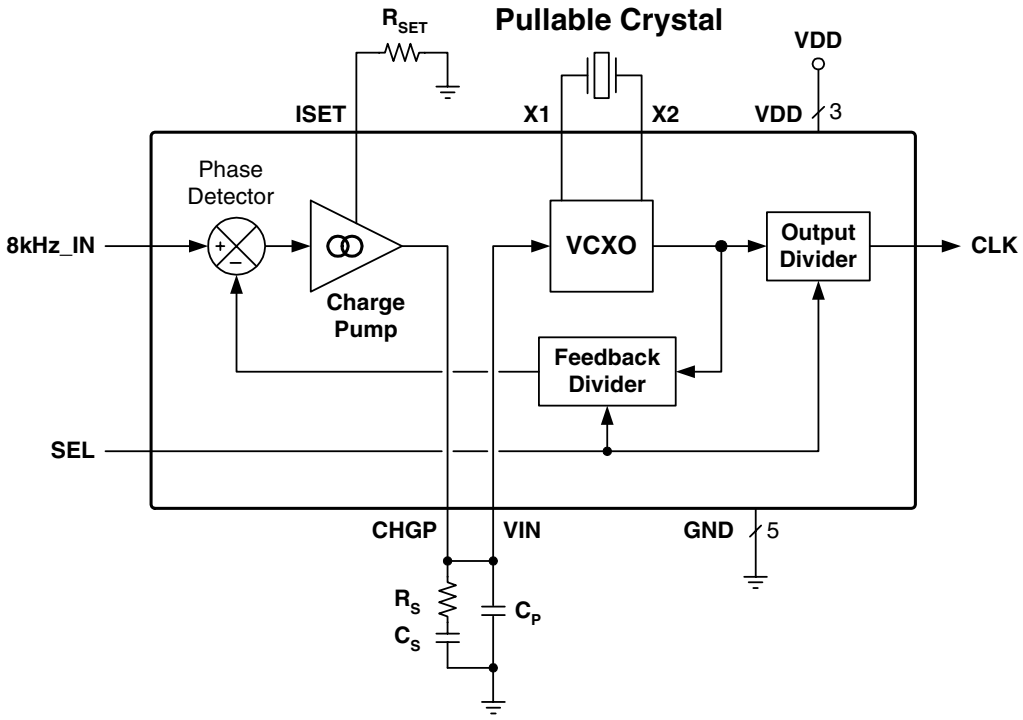
The MK1581-01 provides synchronization and timing control for T1 and E1 based network access or multitrunk telecommunication systems. The device accepts an 8 kHz frame clock input and uses an on-chip VCXO to produce a synchronized low phase noise clock output.

This monolithic IC, combined with an external inexpensive quartz crystal, can be used to replace a more costly hybrid VCXO retiming module. Through selection of external loop filter components values, the device can be tailored to meet the system's clock jitter attenuation requirements. Low-pass jitter attenuation characteristics in the Hz range are possible.

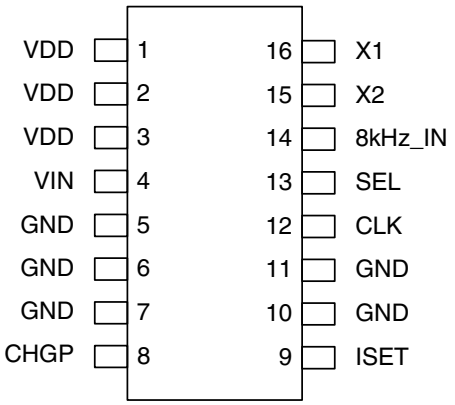
Features

- Generates a T1 (1.544 MHz) or E1 (2.048 MHz) output clock from an 8kHz frame clock input
- Configurable jitter attenuation characteristics, excellent for use as a Stratum source de-jitter circuit
- VCXO-based clock generation ensures very low jitter and phase noise generation
- Output clock is phase and frequency locked to the input reference clock
- ±115ppm minimum crystal frequency pullability range, using recommended crystal
- Industrial temperature range
- Low power CMOS technology
- 16 pin TSSOP package
- Single 3.3 V power supply

Block Diagram



Pin Assignment



16 pin 4.40 mil body, 0.65 mm pitch TSSOP

Output Clock Selection Table

Input Clock	SEL	Output Clock (MHz)	Crystal Used (MHz)
8 kHz	0	1.544	24.704
8 kHz	1	2.048	24.576

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Power Supply. Connect to +3.3 V.
2	VDD	Power	Power Supply. Connect to +3.3 V.
3	VDD	Power	Power Supply. Connect to +3.3 V.
4	VIN	Input	VCXO Control Voltage Input. Connect this pin to CHGP pin and the external loop filter as shown in this data sheet.
5	GND	Power	Connect to ground.
6	GND	Power	Connect to ground.
7	GND	Power	Connect to ground.
8	CHGP	Output	Charge Pump Output. Connect this pin to the external loop filter and to pin VIN.
9	ISET	–	Charge pump current setting node, connection for setting resistor.
10	GND	Power	Connect to ground.
11	GND	Power	Connect to ground.
12	CLK	Output	Clock Output.
13	SEL	Input	Output Frequency Selection. Determines output frequency as per table above. Internal pull-up.
14	8kHz_IN	Input	8 kHz reference clock input.
15	X2	–	Crystal Output. Connect this pin to the specified crystal.
16	X1	–	Crystal Input. Connect this pin to the specified crystal.

Functional Description

The MK1581-01 is a clock generator IC that generates a T1 or E1 reference clock directly from an internal VCXO circuit that works in conjunction with an external quartz crystal. The VCXO output frequency and phase is controlled by an internal PLL (Phase Locked Loop) circuit, enabling the device to perform clock regeneration from an 8 kHz input reference clock.

Most typical PLL clock devices use an internal VCO (Voltage Controlled Oscillator) for output clock generation. By using a VCXO with an external crystal, the MK1581-01 is able to generate a low jitter, low phase-noise output clock. The low bandwidth capability of the PLL circuit serves to provide input clock jitter attenuation and enables stable operation with the low frequency input reference clock.

The internal VCXO circuit requires an external pullable crystal for operation. External loop filter components enable a PLL configuration with low loop bandwidth.

Application Information

Output Frequency Configuration

The MK1581-01 is configured to generate either a 1.544 MHz T1 clock or a 2.048 MHz E1 clock from an 8 kHz input clock. Please refer to the Output Clock Selection Table on Page 2. Input bit SEL is set according to this table, as is the external crystal frequency. Please refer to the Quartz Crystal section on this page regarding external crystal requirements.

Quartz Crystal

It is important that the correct type of quartz crystal is used with the MK1581-01. Failure to do so may result in reduced frequency pullability range, inability of the loop to lock, or excessive output phase jitter.

The MK1581-01 operates by phase-locking the VCXO circuit to the input signal of the selected ICLK input. The VCXO consists of the external crystal and the integrated VCXO oscillator circuit. To achieve the best performance and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the PCB Layout Recommendations section must be followed.

The frequency of oscillation of a quartz crystal is determined by its cut and by the external load capacitance. The MK1581-01 incorporates variable load capacitors on-chip which “pull”, or change, the frequency of the crystal. The crystals specified for use with the MK1581-01 are designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF. To achieve this, the layout should use short traces between the MK1581-01 and the crystal.

A complete description of the recommended crystal parameters is in application note MAN05.

A list of approved crystals is located on the IDT web site **(www.idt.com)**.

PLL Loop Filter Components

A phased-locked loop (PLL) is a control system that keeps the VCO frequency and phase locked with the input reference clock. Like all control systems, analog PLL circuits use a loop filter to establish operating stability. The MK1581-01 uses external loop filter components for the following reasons:

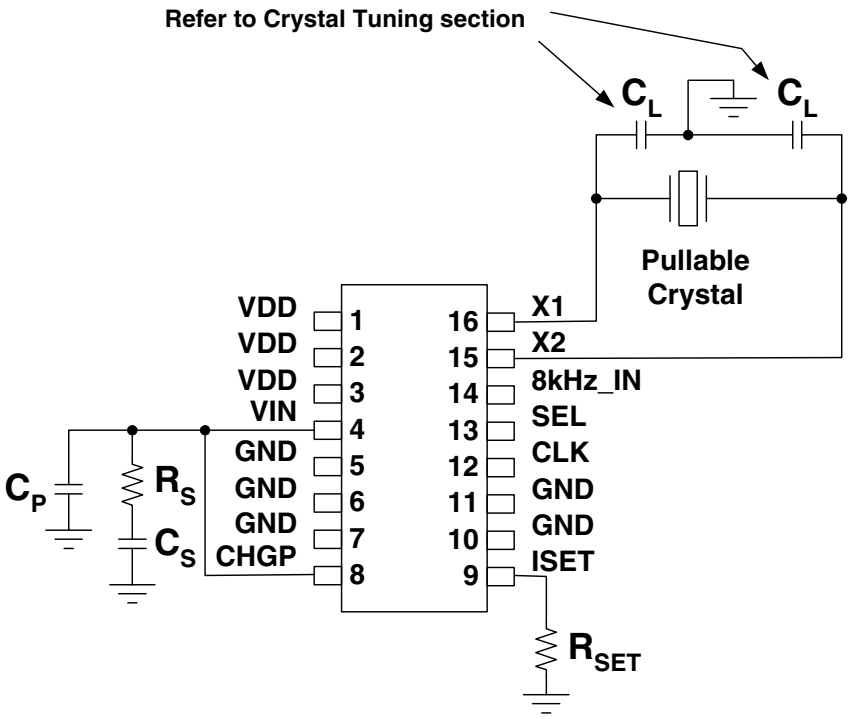
1) Larger loop filter capacitor values can be used, allowing a lower loop bandwidth. This enables the use of lower input clock reference frequencies and also input clock jitter attenuation capabilities. Larger loop filter capacitors also allow higher loop damping factors when less passband peaking is desired.

2) The loop filter values can be user selected to optimize loop response characteristics for a given application.

Referencing the External Component Schematic on this page, the external loop filter is made up of components R_S, C_S and C_P. R_{SET} establishes PLL charge pump current and therefore influences loop filter characteristics.

Design aid tools for configuring the loop filter can be found at www.idt.com, including on-line and PC-based calculators.

External Component Schematic



Recommended Loop Filter Values Vs. Output Frequency Selection

SEL	Output Freq	Crystal Multiplier (N)	R_{SET}	R_S	C_S	C_P	Loop Bandwidth (-3dB point)	Damping Factor
0	1.544 MHz	3088	120 kΩ	1.0 MΩ	0.1 µF	4.7 nF	18 Hz	1.4
1	2.048 MHz	3072	120 kΩ	1.0 MΩ	0.1 µF	4.7 nF	19 Hz	1.4

A “normalized” PLL loop bandwidth may be calculated as follows:

$$NBW = \frac{R_S \times I_{CP} \times 575}{N}$$

The “normalized” bandwidth (NBW) equation above does not take into account the effects of damping factor or the second pole. NBW is approximately equal to the actual -3dB bandwidth of the loop when the damping factor is about 5 and C_2 is very small. In most applications, NBW is about 75% of the actual -3dB bandwidth. However, NBW does provide a useful approximation of filter performance.

The loop damping factor is calculated as follows:

$$\text{Damping Factor} = R_S \times \sqrt{\frac{625 \times I_{CP} \times C_S}{N}}$$

Where:

R_S = Value of resistor in loop filter (Ohms)
I_{CP} = Charge pump current (amps)
(refer to Charge Pump Current Table, below)
N = Crystal multiplier shown in the above table
C_S = Value of capacitor C_S in loop filter (Farads)

As a general rule, the following relationship should be maintained between components C_S and C_P in the loop filter:

$$C_P = \frac{C_S}{20}$$

Charge Pump Current Table

R_{SET}	Charge Pump Current (I_{CP})
1.4 MΩ	10 µA
680 kΩ	20 µA
540 kΩ	25 µA
120 kΩ	100 µA

Special considerations must be made in choosing loop components C_S and C_P.

Series Termination Resistor

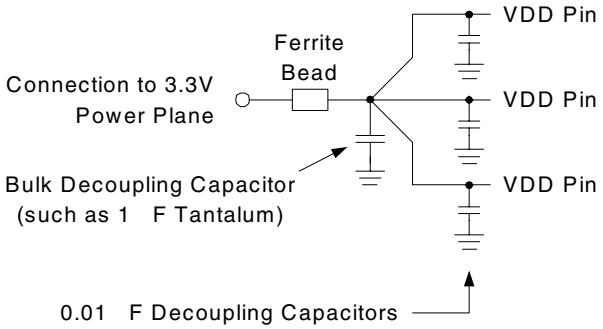
Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω (The optional series termination resistor is not shown in the External Component Schematic.)

Decoupling Capacitors

As with any high performance mixed-signal IC, the MK1581-01 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane. To further guard against interfering system supply noise, the MK1581-01 should use one common connection to the PCB power plane as shown in the diagram on the next page. The ferrite bead and bulk capacitor help reduce lower frequency noise in the supply that can lead to output clock phase modulation.

Recommended Power Supply Connection for Optimal Device Performance



Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground, shown as C_L in the External Component Schematic. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) been the crystal and device.

In most cases the load capacitors will not be required. They should not be stuffed on the prototype evaluation board as the indiscriminate use of these trim capacitors will typically cause more crystal centering error than their absence. If the need for the load capacitors is later determined, the values will fall within the 1-4 pF range. The need for, and value of, these trim capacitors can only be determined at prototype evaluation. Refer to MAN05 for the centering capacitor selection procedure.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please also refer to the Recommended PCB Layout drawing on Page 7.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No via's should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The loop filter components must also be placed close to the CHGP and VIN pins. C_P should be closest to the device. Coupling of noise from other system signal traces should be minimized by keeping traces short and away from active signal traces. Use of vias should be avoided.

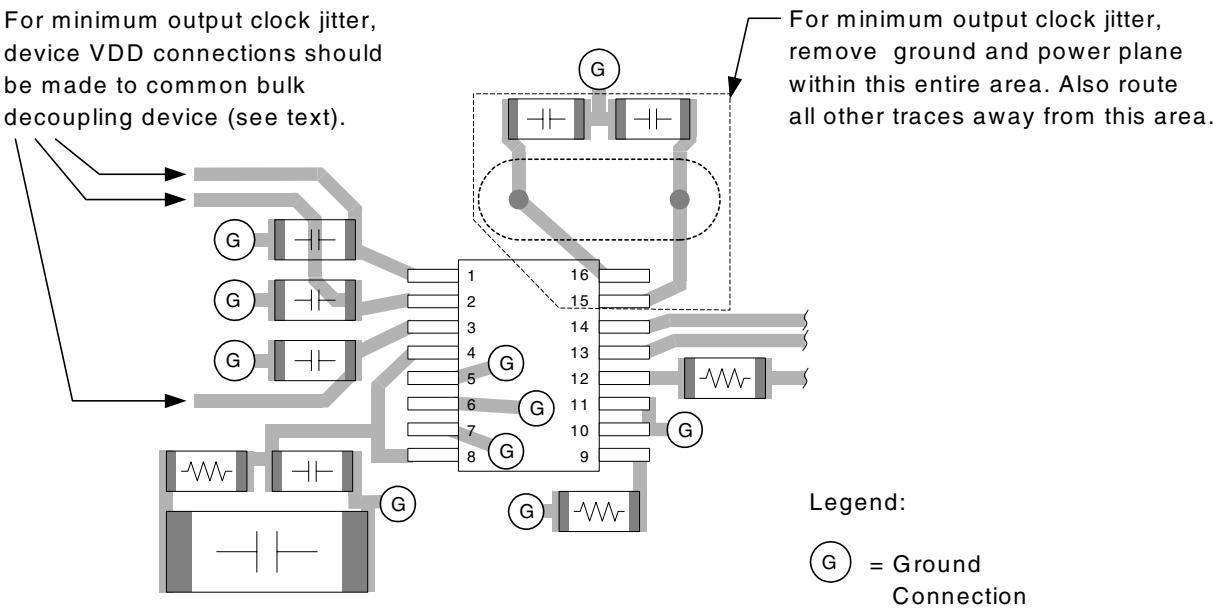
3) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

4) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

5) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK1581-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

The IDT Applications Note MAN05 may also be referenced for additional suggestions on layout of the crystal section.

Recommended PCB Layout



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1581-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Supply Current	IDD	Clock outputs unloaded, VDD = 3.3 V		10	15	mA
Input High Voltage, SEL	V_{IH}		2			V
Input Low Voltage, SEL	V_{IL}				0.8	V
Input High Voltage, 8kHz_IN	V_{IH}		VDD/2+1			V
Input Low Voltage, 8kHz_IN	V_{IL}				VDD/2-1	V
Input High Current	I_{IH}	V_{IH} = VDD	-10		+10	µA
Input Low Current	I_{IL}	V_{IL} = 0	-10		+10	µA
Input Capacitance, except X1	C_{IN}			7		pF
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Short Circuit Current	I_{OS}			±50		mA
VIN, VCXO Control Voltage	V_{XC}		0		VDD	V
Nominal Output Impedance	Z_{OUT}			20		Ω

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VCXO Crystal Pull Range	f_{XP}	Using Recommended Crystal	-115		+115	ppm
VCXO Crystal Nominal Frequency	f_X		24.704		24.576	MHz
Input Jitter Tolerance	t_{ji}	In reference to input clock period			0.4	UI
Input pulse width (1)	t_{pi}		10			ns
Output Frequency Error	F_{OUT}	ICLK = 0 ppm error	0	0	0	ppm
Output Duty Cycle (% high time)	t_{OD}	Measured at VDD/2, C_L=15 pF	40		60	%
Output Rise Time	t_{OR}	0.8 to 2.0V, C_L=15 pF			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8V, C_L=15 pF			1.5	ns
Skew, Input to Output Clock	t_{IO}	Note 2				
Cycle Jitter (short term jitter)	t_{ja}	Peak to Peak		150		ps p-p

Note 1: Minimum high or low time of input clock.

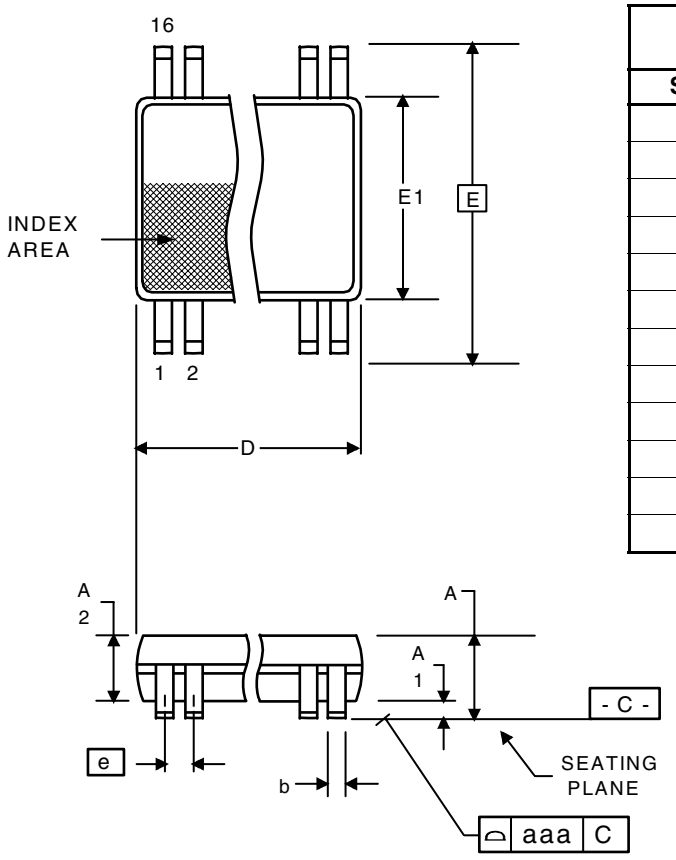
Note 2: The input to output clock skew is not controlled nor predictable and will change between power up cycles. Because it is dependent on the phase relationship between the output and feedback divider states following power up, the input to output clock skew will remain stable during a given power up cycle. If controlled input to output skew is desired for this output clock frequency please refer to the MK2049 or MK2069 products.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1581-01GILF	15810GIL	Tubes	16-pin TSSOP	-40 to +85° C
MK1581-01GILFTR	15810GIL	Tape and Reel	16-pin TSSOP	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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