

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

LOW EMI CLOCK GENERATOR

MK1704A

Description

The MK1704A is an upgraded version of the MK1704 and is recommended for all new designs. It offers more reduction in the frequency amplitude peaks and will support frequencies up to 140 MHz.

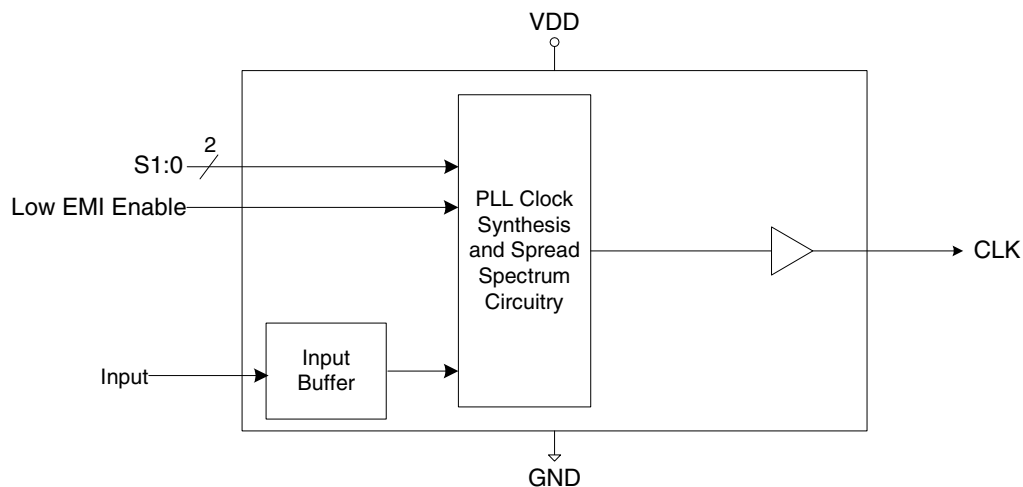
The MK1704A generates a low EMI output clock from a clock input. The part is designed to dither the LCD interface clock or other clocks for flat panel graphics controllers. The MK1704A uses IDT's proprietary mixture of analog and digital Phase Locked Loop (PLL) technology to synthesize the frequency. It also uses IDT's patented technique to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

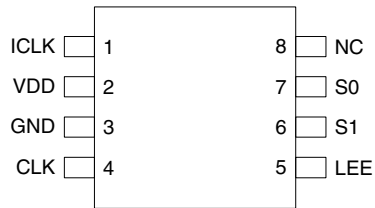
Features

- 8 pin SOIC package
- Pb (lead) free package
- Provides a spread spectrum output clock
- Supports leading flat panel controllers
- Accepts a clock input, provides same frequency dithered output
- Optimized for higher resolutions that require up to 140 MHz, as well as 40 MHz (SVGA) and 65 MHz (XVGA) clocks
- Peak reduction by 7 dB - 14 dB typical on 3rd - 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 3.3V or 5V
- Advanced, low power CMOS process
- See the MK1714-01 for a multiplier with low EMI which can operate from a crystal

Block Diagram



Pin Assignment



8 pin (150 mil) SOIC

Output Clock Selection Table

S1	S0	Input Min.	Input Nom.	Input Max.	Mult.	Freq. spread vs. CLK
0	0	60	135	140	x1	+0.5, -1.5%
0	1	60	80	120	x1	+0.5, -1.5%
1	0	30	40	60	x1	Down 2.5%
1	1	40	65	100	x1	+0.5, -1.5%

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	XI	Connect to a clock input as shown in table above.
2	VDD	Power	Connect to +3.3V or +5V.
3	GND	Power	Connect to ground.
4	CLK	Output	Clock output equal to input frequency.
5	LEE	Input	Low EMI enable. Turns on the spread spectrum when high. Internal pull-up.
6	S1	Input	Frequency select 1 input. Selects input/output clock range per table above. Internal pull-up.
7	S0	Input	Frequency select 0 input. Selects input/output clock range per table above. Internal pull-up.
8	NC	-	No connect. Do not connect anything to this pin.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitor

A decoupling capacitor of 0.01μF must be connected between VDD and GND on pins 2 and 3.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01μF decoupling capacitor should be mounted on

the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal

layers. Other signal traces should be routed away from the MK1704A. This includes signal traces just underneath the

device, or on layers adjacent to the ground plane layer used by the device.

Powerup Considerations

To insure proper operation of the spread spectrum generation circuit, some precautions must be taken in the implementation of the MK1704A.

- 1) An input signal should not be applied to ICLK until VDD is stable. This requirement can easily be met by operating the MK1704A and the ICLK source from the same power supply.
- 2) LEE should not be enabled (taken high) until after the power supplies and input clock are stable. This requirement can be met by direct control of LEE by system logic; for

example, a “power good” signal. Another solution is to leave LEE unconnected to anything but a 0.01 μ F capacitor to ground. The pullup resistor on LEE will charge the capacitor and provide approximately a one millisecond delay until spread spectrum is enabled.

- 3) If the input frequency is changed during operation, disable spread spectrum until the input clock stabilizes at the new frequency. LEE should be disabled for 10 μ s minimum.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1704A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	175° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

Unless stated otherwise, VDD = 5V, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Supply Current	IDD	No load, 3.3V		10		mA
		No load, 5V		15		mA
Input High Voltage	V _{IH}	Clock input	(VDD/2)+1	VDD/2		V
Input Low Voltage	V _{IL}	Clock input		VDD/2	(VDD/2)-1	V
Output High Voltage	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.4	V
Input Capacitance	C _{IN}	S0 pin		7		pF
Nominal Output Impedance	Z _{OUT}			20		Ω
Internal Pull-up Resistor	R _{PU}	LEE pin only		500		kΩ

AC Electrical Characteristics

Unless stated otherwise, VDD = 5V, Ambient Temperature 0 to +70° C

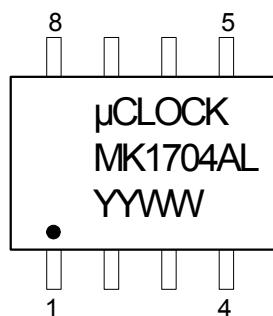
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency		S1=0, S0=0	60	135	140	MHz
		S1=0, S0=1	60	80	120	MHz
		S1=1, S0=0	30	40	60	MHz
		S1=1, S0=1	40	65	100	MHz
Input Clock Duty Cycle		Time above VDD/2	20		80	%
Output Rise Time	t _{OR}	0.8 to 2.0V, Note 1			1.5	ns
Output Fall Time	t _{OF}	2.0 to 0.8V, Note 1			1.5	ns
Output Clock Duty Cycle		Time above 1.5V	40	50	60	%
Output Clock Frequency Variation from Mean				1-2.5		%
EMI Peak Frequency Reduction		3rd - 19th odd harmonics		10-16		dB

Note 1: Measured with 15pF load

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram (Pb free)

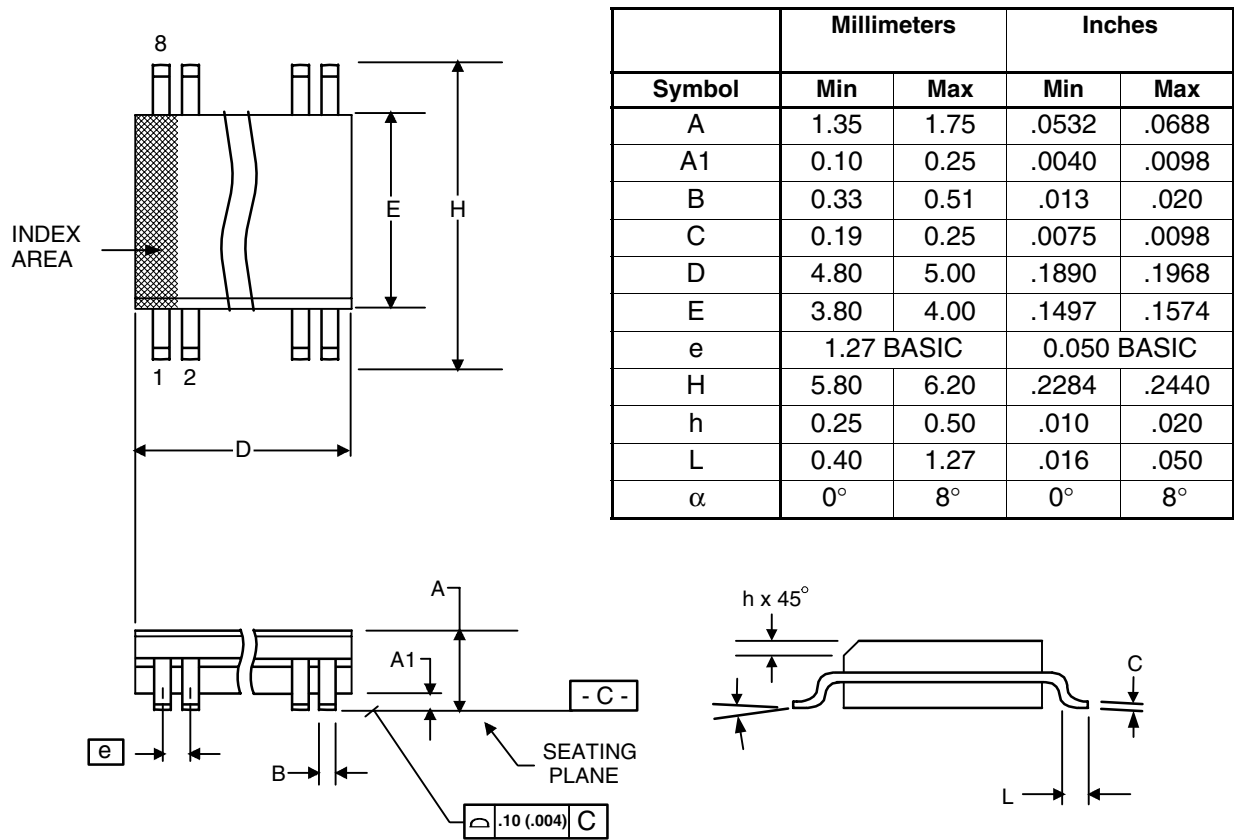


Notes:

- YYWW is the last two digits of the year and week the part was assembled.
- "L" denotes Pb (lead) free package
- Bottom Markings:
 ##### = lot number
 (origin) = country of origin if not USA

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1704ALF	see page 5	Tubes	8 pin SOIC	0 to +70° C
MK1704ALFTR		Tape and Reel	8 pin SOIC	0 to +70° C

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com



www.IDT.com