

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

LOW EMI CLOCK GENERATOR

MK1707

Description

The MK1707 generates a low EMI output clock from a clock input. The part is designed to dither the LCD interface clock for flat panel graphics controllers. The device uses IDT's proprietary mix of analog and digital Phase Locked Loop (PLL) technology to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

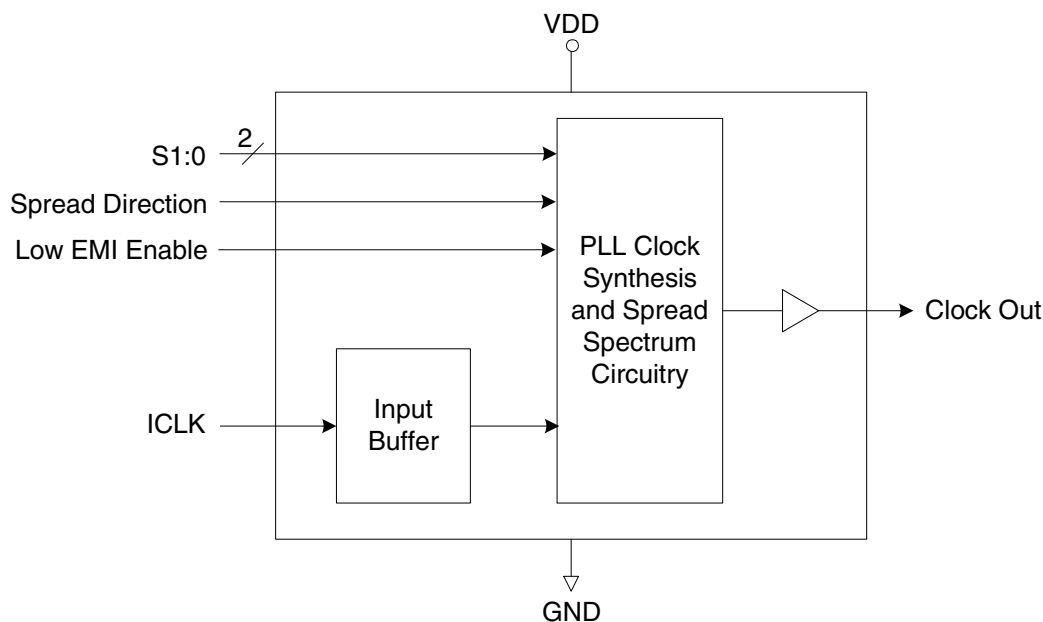
The MK1707 offers both centered and down spread from a high speed clock input. Refer to the MK1714-01/02 for a crystal input and the widest selection of input frequencies and multipliers.

IDT offers many other clocks for computers and computer peripherals. Consult us when you need to remove crystals and oscillators from your board.

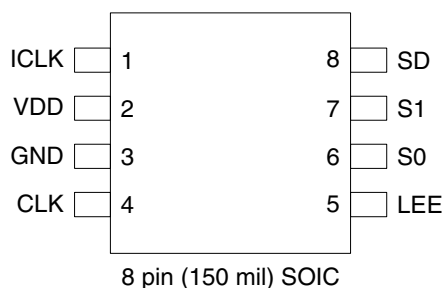
Features

- Packaged in 8-pin SOIC
- Pb-free package
- Industrial temperature range available
- Provides a spread spectrum output clock
- Supports ATI's flat panel controllers
- Guaranteed to +85° C operation
- Accepts a clock input, provides same frequency dithered output
- Good for all VGA modes from 80 to 167 MHz
- Peak reduction by 7dB - 14dB typical on 3rd - 19th odd harmonics
- Low EMI feature can be disabled
- Includes Power-down
- Operating voltage of 3.3 V or 5 V
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



Spread Direction and Percentage Select Table

SD Pin 8	S1 Pin 7	S0 Pin 6	Spread Direction	Spread Percentage (%)
0	0	0	Down	0.6
0	0	M	Down	0.8
0	0	1	Down	1.25
0	M	0	Down Center	+0.5, -1.5
0	M	M	Down	2
0	M	1	Down Center	+0.5, -2.5
0	1	0	Down Center	+0.5, -3
0	1	M	Down	5
0	1	1	Power Down	-
1	0	0	Center	±0.35
1	0	M	Center	±0.5
1	0	1	Center	±0.7
1	M	0	Center	±0.8
1	M	M	Center	±1.1
1	M	1	Center	±1.4
1	1	0	Test	Test
1	1	M	Center	±2.5
1	1	1	Power Down	-

0 = connect to GND

M = unconnected (floating)

1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Connect to graphics input clock.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	CLK	Output	Spread spectrum clock output per table above.
5	LEE	Input	Low EMI enable. Turns on spread spectrum when high. Internal pull-up resistor.
6	S0	Input	Function select 0 input. Selects spread amount and direction per table above. Internal mid-level.
7	S1	Input	Function select 1 input. Selects spread amount and direction per table above. Internal mid-level.
8	SD	Input	Spread direction select input. Selects the direction of spread per table above. Internal pull-up resistor.

External Components

The MK1707 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01 μ F must be connected between VDD and GND on pins 2 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω .

Tri-level Select Pin Operation

The S1, S0 select pins are tri-level, meaning they have three separate states to make the selections shown in the table on page 2. To select the M (mid) level, the connection to these pins must be eliminated by either floating them originally, or tri-stating the GPIO pins which drive the select pins.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01 μ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33 Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK1707. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Powerup Considerations

To insure proper operation of the spread spectrum generation circuit, some precautions must be taken while utilizing the MK1707.

1. An input signal should not be applied to ICLK until VDD is stable (within 10% of its final value). This requirement can easily be met by operating the MK1707 and then ICLK source from the same power supply.
2. LEE should not be enabled (taken high) until after the power supplies and input clock are stable. This requirement can be met by direct control of LEE by system logic - for example, a "power good" signal. Another solution is to leave LEE unconnected to anything but a 0.01 μ F capacitor to ground. The internal pullup resistor on LEE will charge the capacitor and provide approximately a 700 μ s delay until spread spectrum is enabled.
3. If the input frequency is changed during operation, disable spread spectrum until the input clock stabilizes at the new frequency.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1707. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Commercial	0 to +85° C
Ambient Operating Temperature, Industrial	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135		+5.5	V

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V, Ambient Temperature 0 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		5.5	V
Supply Current	IDD	No load, at 3.3 V		20		mA
		No load, at 5 V		31		mA
	IDDPD	S0=S1=SD=1		60		μA
Input High Voltage	V _{IH}	ICLK	(VDD/2) + 1	VDD/2		V
Input Low Voltage	V _{IL}	ICLK		VDD/2	(VDD/2) - 1	V
Input High Voltage	V _{IH}	S1, S0	VDD-0.5			V
Input High Voltage	V _{IH}	other inputs	2.5			V
Input Low Voltage	V _{IL}	S0, S1, SD, LEE pins			0.5	V
Output High Voltage	V _{OH}	CMOS, I _{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V _{OH}	I _{OH} = -12 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = -12 mA			0.4	V
Input Capacitance	C _{IN}	S0, S1, SD, LEE pins		5		pF

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V}$, Ambient Temperature 0 to $+85^{\circ}\text{ C}$

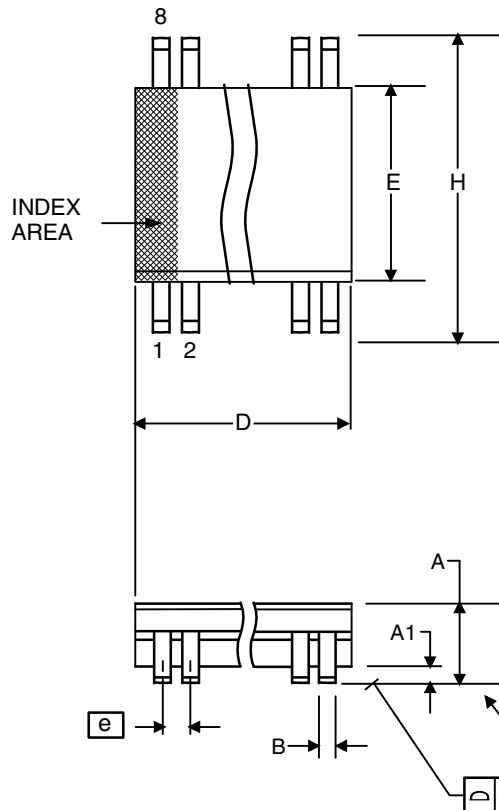
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input/Output Clock Frequency			80		167	MHz
Input Clock Duty Cycle		Time above $V_{DD}/2$	20		80	%
Output Clock Duty Cycle		Time above 1.5 V	40	50	60	%
Output Rise Time	t_{OR}	0.8 to 2.0 V		1.5		ns
Output Fall Time	t_{OF}	2.0 to 0.8 V		1.5		ns
Modulation Frequency			19		41	kHz
EMI Peak Frequency Reduction		3rd - 19th odd harmonics		7 to 14		dB

Thermal Characteristics

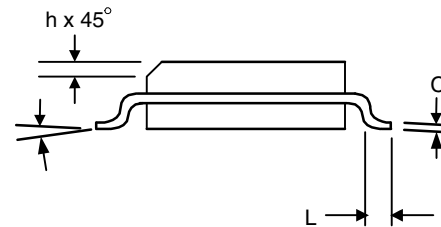
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		$^{\circ}\text{C/W}$
	θ_{JA}	1 m/s air flow		140		$^{\circ}\text{C/W}$
	θ_{JA}	3 m/s air flow		120		$^{\circ}\text{C/W}$
Thermal Resistance Junction to Case	θ_{JC}			40		$^{\circ}\text{C/W}$

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1707SLF	MK1707SL	Tubes	8-pin SOIC	0 to +85° C
MK1707SLFTR	MK1707SL	Tape and Reel	8-pin SOIC	0 to +85° C
MK1707SILF	MK1707IL	Tubes	8-pin SOIC	-40 to +85° C
MK1707SILFTR	MK1707IL	Tape and Reel	8-pin SOIC	-40 to +85° C

Note: "LF" denotes Pb (lead) free package.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

www.idt.com/go/clockhelp

Corporate Headquarters

Integrated Device Technology, Inc.
www.idt.com

