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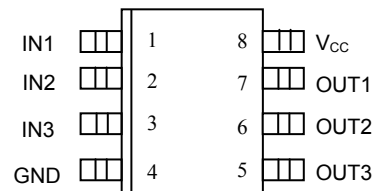
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### FEATURES

- All-Silicon Timing Circuit
- Three Independent Buffered Delays
- Stable and Precise Over Temperature and Voltage
- Leading and Trailing Edge Precision Preserves the Input Symmetry
- Vapor Phase and IR Reflow Solderable
- Available in Tape and Reel
- Delays Specified Over Both Commercial and Industrial Temperature Ranges
- 3V Operation
- Recommended Replacement for DS1033

### PIN ASSIGNMENT



DS1135LZ 8-Pin SO (150 mils)

### PIN DESCRIPTION

IN1-IN3	- Input Signals
OUT1-OUT3	- Output Signals
V <sub>CC</sub>	- +3V Supply
GND	- Ground

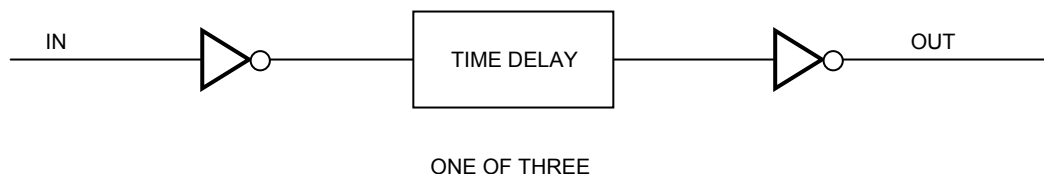
### DESCRIPTION

The DS1135L series is a low-power, 3V high-speed version of the popular DS1013, DS1033, and DS1035 series.

The DS1135L series of delay lines have three independent logic buffered delays in a single package. The device is our fastest 3-in-1 delay line. It is available in a 150-mil 8-pin SO.

The device features precise leading and trailing edge accuracy. It has the inherent reliability of an all-silicon delay line solution.

Standard delay values are indicated in Table 1.

**LOGIC DIAGRAM** Figure 1**PART NUMBER DELAY TABLE ( $t_{PLH}$ ,  $t_{PHL}$ )** Table 1

PART NUMBER	DELAY PER OUTPUT (ns)	INITIAL TOLERANCE (Note 1)	TOLERANCE OVER TEMP AND VOLTAGE (Note 2)	
			0°C to +70°C	-40°C to +85°C
DS1135LZ-10+	10/10/10	±1.0ns	±2.0ns	±3.0ns
DS1135LZ-12+	12/12/12	±1.0ns	±2.0ns	±3.0ns
DS1135LZ-15+	15/15/15	±1.0ns	±2.5ns	±4.0ns
DS1135LZ-20+	20/20/20	±1.0ns	±2.5ns	±4.0ns
DS1135LZ-25+	25/25/25	±1.5ns	±3.0ns	±5.0ns
DS1135LZ-30+	30/30/30	±1.5ns	±3.0ns	±5.0ns

+Denotes a lead(Pb)-free/RoHS-compliant package.

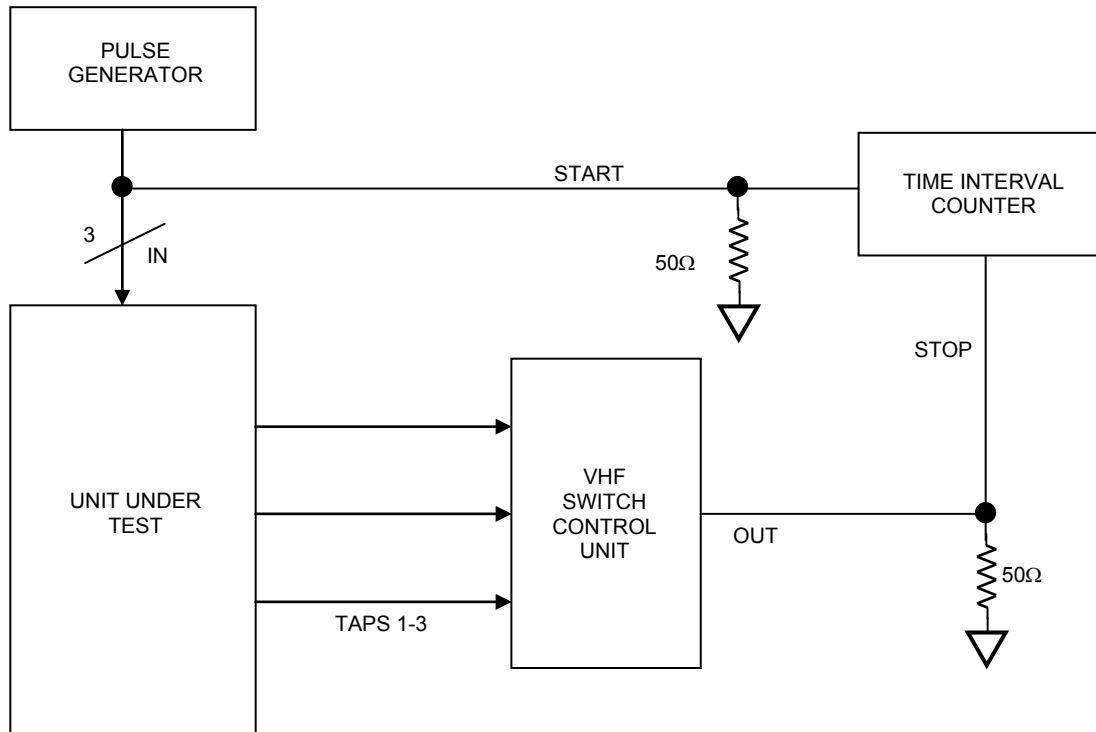
**NOTES:**

1. Nominal conditions are +25°C and  $V_{CC} = +3.3V$ .
2. Voltage range of 2.7V to 3.6V.
3. Delay accuracies are for both leading and trailing edges.

**TEST SETUP DESCRIPTION**

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1135L. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1135L output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

## DS1135L TEST CIRCUIT Figure 2



**ABSOLUTE MAXIMUM RATINGS**

Voltage Range on Any Pin Relative to Ground	-1.0V to +6.0 V
Short-Circuit Output Current	50mA for 1 second
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Soldering Temperature (reflow)	+260°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

**DC ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 2.7V$  to  $3.6V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC}$		2.7	3.3	3.6	V
Active Current	$I_{CC}$	$V_{CC} = 3.6V$ , period = $1\mu s$			10	mA
High Level Input Voltage	$V_{IH}$		2.0		$V_{CC} + 0.5$	V
Low Level Input Voltage	$V_{IL}$		-0.5		0.8	V
Input Leakage	$I_L$	$0V \leq V_I \leq V_{CC}$	-1.0		+1.0	$\mu A$
High Level Output Current	$I_{CC}$	$V_{CC} = 2.7V$ , $V_{OH} = 2V$			-1.0	mA
Low Level Output Current	$I_{CC}$	$V_{CC} = 2.7V$ , $V_{OL} = 0.4V$	8			mA

**AC ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 2.7V$  to  $3.6V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	$t_{PERIOD}$	2 ( $t_{WI}$ )			ns	
Input Pulse Width	$t_{WI}$	100% of Delay Value			ns	
Input-to-Output Delay	$t_{PLH}, t_{PHL}$	See Table 1			ns	
Output Rise or Fall Time	$t_{OF}, t_{OR}$		2.0	2.5	ns	
Power-up Time	$t_{PU}$			1	ms	2

**CAPACITANCE**

( $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$			10	pF	

## TEST CONDITIONS

Ambient Temperature:  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$

Supply Voltage ( $V_{\text{CC}}$ ):  $3.3\text{V} \pm 0.1\text{V}$

Input Pulse:

High:  $3.0\text{V} \pm 0.1\text{V}$

Low:  $0.0\text{V} \pm 0.1\text{V}$

Source Impedance:  $50\Omega$  Max.

Rise and Fall Time:  $3.0\text{ns}$  Max. — Measured between  $0.6\text{V}$  and  $2.4\text{V}$ .

Pulse Width:  $500\text{ns}$

Pulse Period:  $1\mu\text{s}$

Output Load Capacitance:  $15\text{pF}$

Output: Each output is loaded with the equivalent of one 74F04 input gate.

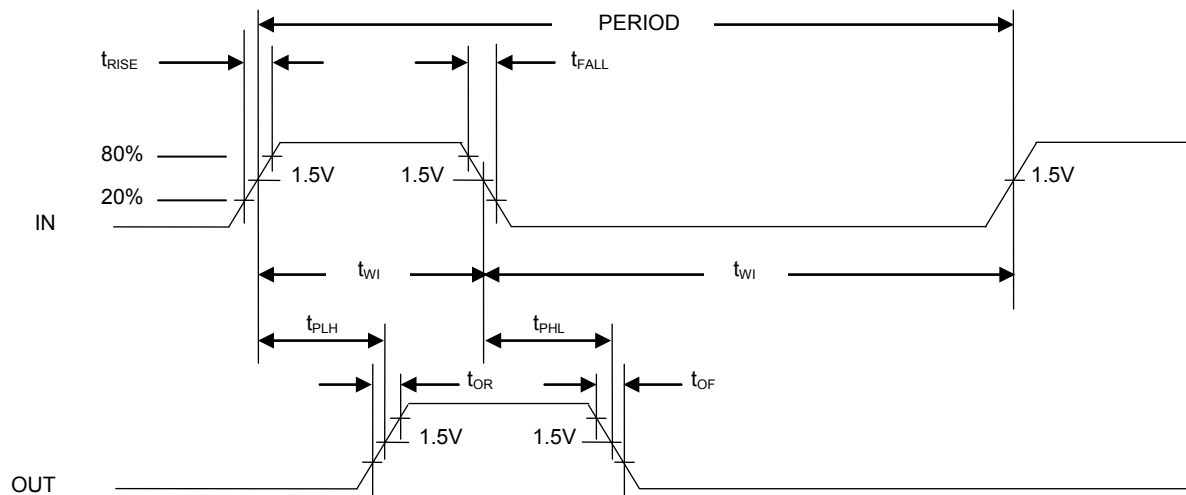
Data is measured at the  $1.5\text{V}$  level on the rising and falling edges.

**Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.**

## NOTES:

1. All voltages are referenced to ground.
2. Power-up time is the time from the application of power to the time stable delays are being produced at the output.

## TIMING DIAGRAM



## TERMINOLOGY

**Period:** The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

**$t_{WI}$  (Pulse Width):** The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

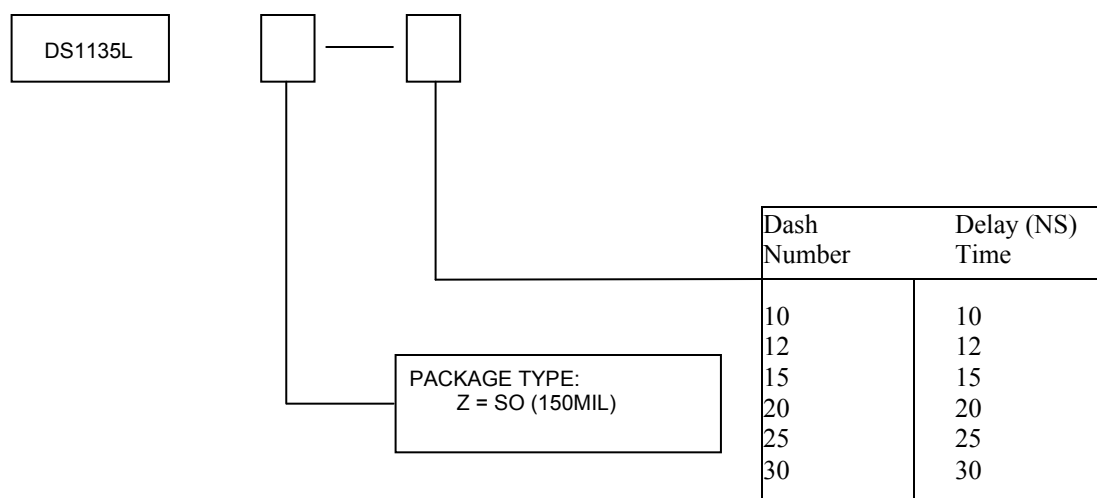
**$t_{RISE}$  (Input Rise Time):** The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

**$t_{FALL}$  (Input Fall Time):** The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

**$t_{PLH}$  (Time Delay, Rising):** The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

**$t_{PHL}$  (Time Delay, Falling):** The elapsed time between the 1.5V point on the falling edge of the input pulse and the 1.5V point on the falling edge of the output pulse.

## ORDERING INFORMATION



## PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+2	<a href="#">21-0041</a>	<a href="#">90-0096</a>

**REVISION HISTORY**

<b>REVISION DATE</b>	<b>DESCRIPTION</b>	<b>PAGES CHANGED</b>
8/12	Removed the $\mu$ SOP package; updated the <i>Absolute Maximum Ratings</i> section; added the <i>Package Information</i> section	1, 2, 4, 6

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