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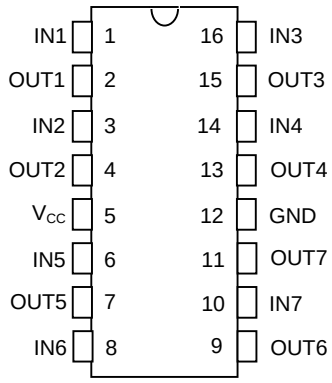
DS1007
7-1 Silicon Delay Line

www.dalsemi.com

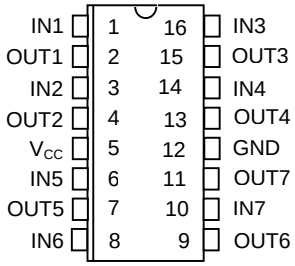
FEATURES

- All-silicon time delay
- 7 independent buffered delays
- Delay tolerance ±2 ns
- Four delays can be custom set between 3 ns and 10 ns
- Three delays can be custom set between 9 ns and 40 ns
- Delays are stable and precise
- Economical
- Auto-insertable, low profile
- Surface mount 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom specifications available
- Quick turn prototypes

PIN ASSIGNMENT



DS1007 16-Pin DIP (300-mil)
See Mech. Drawings Section



DS1007S 16-Pin SOIC
(300-mil)
See Mech. Drawings Section

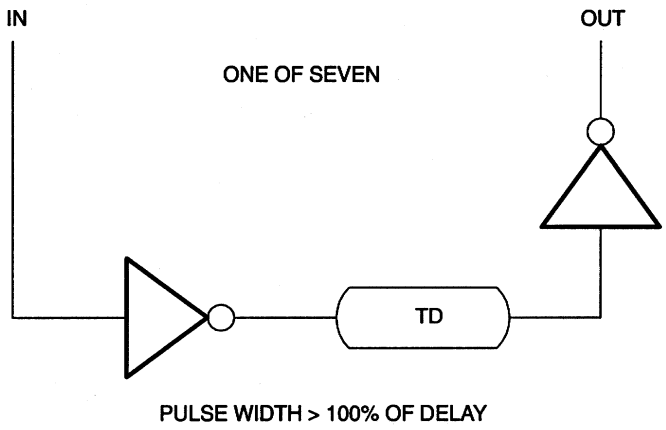
PIN DESCRIPTION

IN1 - IN7	- Inputs
Out1 – Out7	- Outputs
GND	- Ground
V_{CC}	- +5 Volts

DESCRIPTION

The DS1007 7-in-1 Silicon Delay Line provides seven independent delay times which are set by Dallas Semiconductor to the customer's specification. The delay times can be set from 3 ns to 40 ns with an accuracy of ±2 ns at room temperature. The device is offered in both a 16-pin DIP and a 16-pin SOIC. Since the DS1007 is an all-silicon solution, better economy and reliability are achieved when compared to older methods using hybrid technology. The DS1007 reproduces the input logic state at the output after the fixed delay. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (972) 371–4348.

LOGIC DIAGRAM Figure 1

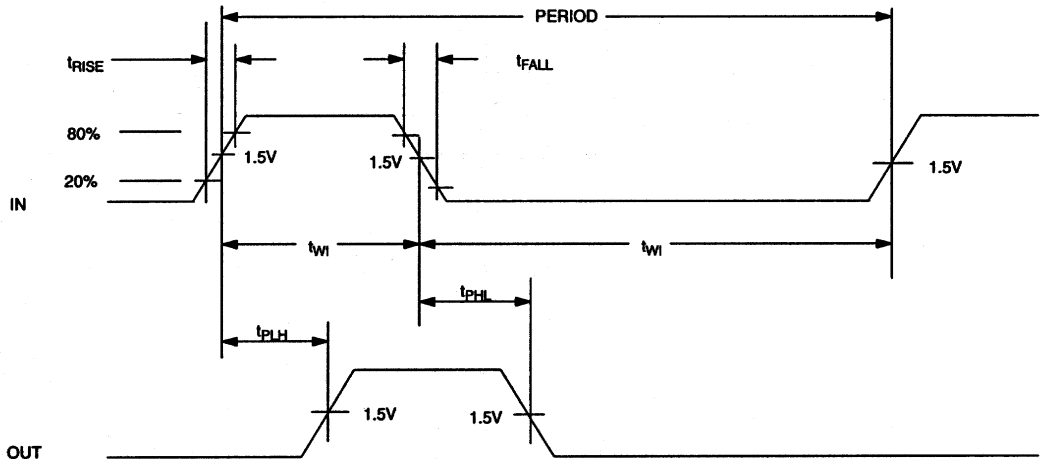


PART NUMBER DELAY TABLE (t_{PLH}) Table 1

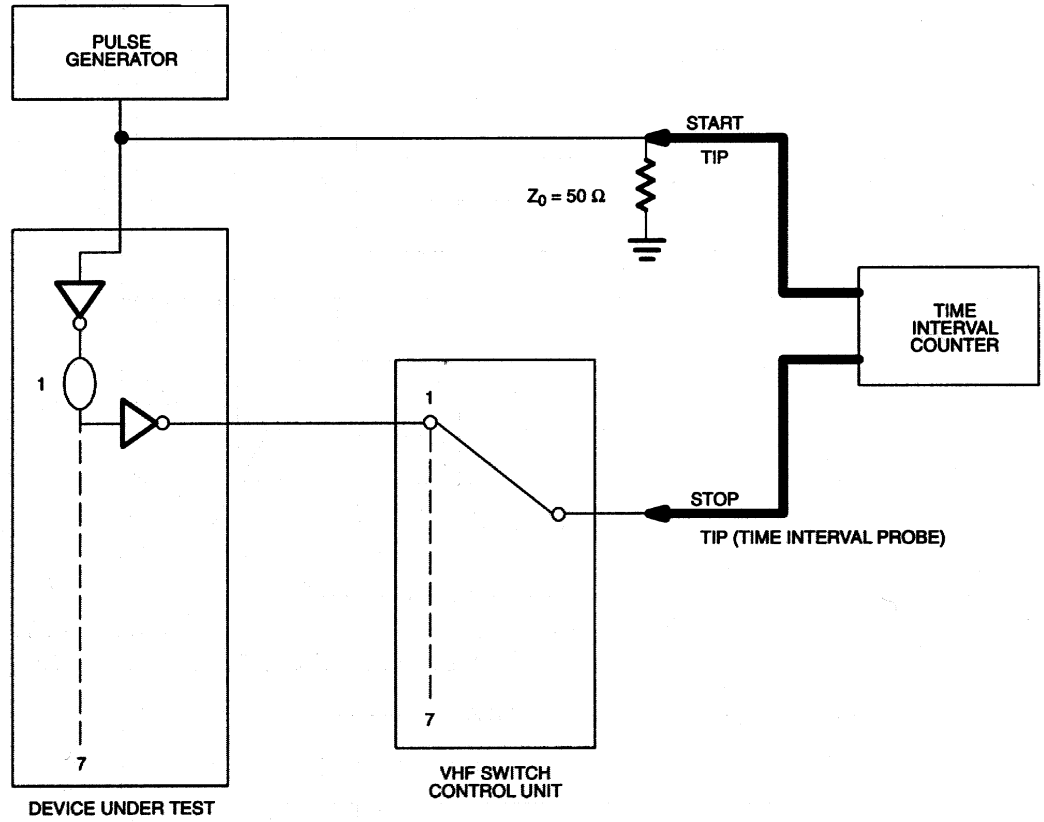
PART #	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7
DS1007-1	3ns	4ns	5ns	6ns	9ns	13ns	18ns
DS1007-2	4	6	8	10	12	14	16
DS1007-3	3	3	3	3	10	10	10
DS1007-4	4	4	4	4	12	12	12
DS1007-5	5	5	5	5	15	15	15
DS1007-6	6	6	6	6	20	20	20
DS1007-7	7	7	7	7	25	25	25
DS1007-8	8	8	8	8	30	30	30
DS1007-9	9	9	9	9	35	35	35
DS1007-10	10	10	10	10	40	40	40
DS1007-11	3	4	6	8	10	12	14
DS1007-12	3	4	6	8	10	15	20
DS1007-13	3	4	6	8	12	15	20
DS1007-14	7	7	7	7	9	9	9

Custom delays available. Out 1 through Out 4 can be custom set from 3 to 10 ns (leading edge only accuracy). Out 5 through Out 7 can be set from 9 to 40 ns (both leading and trailing edge accuracy).

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	uA	
Active Current	I_{CC}	V_{CC}=Max; Period=Min.		40.0	70.0	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5
Power-up Time	t_{PU}			100	ms	7
	Period	3 (t_{WI})			ns	6

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.

2. Measured with outputs open.

3. V_{CC} = 5V @25°C. Delays accurate on rising edges within ±2 ns.

4. See Test Conditions below.

5. All output delays in the same speed output tend to vary unidirectionally with temperature or voltage range (i.e., if Out 2 slows down, all other outputs also slow down).

6. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

7. t_{PU} = 0 ms for Out 1 through Out 4.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the corresponding output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1007. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max.
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.