

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

## DS1100L

# 3.3V 5-Tap Economy Timing Element (Delay Line)

### GENERAL DESCRIPTION

The DS1100L is a 3.3V version of the DS1100. It is characterized for operation over the range 3.0V to 3.6V. The DS1100L series delay lines have five equally spaced taps providing delays from 4ns to 500ns. These devices are offered in surface-mount packages to save PCB area. Low cost and superior reliability over hybrid technology is achieved by the combination of a 100% silicon delay line and industry-standard  $\mu$ MAX<sup>®</sup> and SO packaging. The DS1100L 5-tap silicon delay line reproduces the input-logic state at the output after a fixed delay as specified by the extension of the part number after the dash. The DS1100L is designed to reproduce both leading and trailing edges with equal precision. Each tap is capable of driving up to 10 74LS loads.

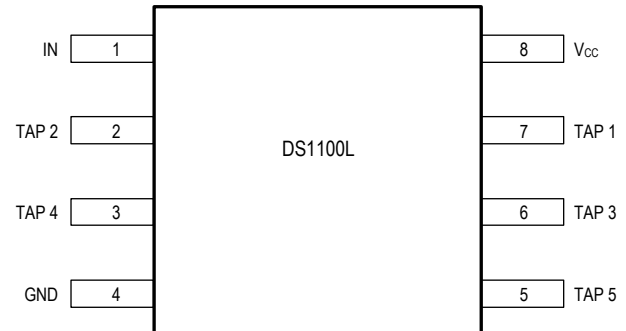
Maxim Integrated can customize standard products to meet special needs.

*$\mu$ MAX is a registered trademark of Maxim Integrated Products, Inc.*

### FEATURES

- All-Silicon Timing Circuit
- Five Taps Equally Spaced
- Delays are Stable and Precise
- Both Leading- and Trailing-Edge Accuracy
- 3.3V Version of the DS1100
- Low-Power CMOS
- TTL-/CMOS-Compatible
- Vapor-Phase and IR Solderable
- Custom Delays Available
- Fast-Turn Prototypes
- Delays Specified Over Both Commercial and Industrial Temperature Ranges

### PIN ASSIGNMENT



DS1100LZ SO (150mils)  
DS1100LU  $\mu$ MAX

### PIN DESCRIPTION

TAP 1 to TAP 5	- TAP Output Number
V <sub>CC</sub>	- +3.3V
GND	- Ground
IN	- Input

**ABSOLUTE MAXIMUM RATINGS**

Voltage Range on Any Pin Relative to Ground .....	-0.5V to +6.0V
Short-Circuit Output Current.....	50mA for 1s
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
SO (derate 5.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	470.6mW
$\mu\text{MAX}$ (derate 4.5mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ ) .....	362mW
Operating Temperature Range .....	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Storage Temperature Range .....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s).....	$+300^\circ\text{C}$
Soldering Temperature (reflow)	
Lead(Pb)-free .....	$+260^\circ\text{C}$
Containing lead(Pb).....	$+240^\circ\text{C}$

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

**DC ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 3.0\text{V}$  to  $3.6\text{V}$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	$V_{CC}$		3.0	3.3	3.6	V	5
High-Level Input Voltage	$V_{IH}$		2.0		$V_{CC} + 0.3$	V	5
Low-Level Input Voltage	$V_{IL}$		-0.3		0.8	V	5
Input-Leakage Current	$I_I$	$0.0\text{V} \leq V_I \leq V_{CC}$	-1.0		+1.0	$\mu\text{A}$	
Active Current	$I_{CC}$	$V_{CC} = \text{Max}$ ; Freq. = 1MHz		10		mA	6, 8
High-Level Output Current	$I_{OH}$	$V_{CC} = \text{Min}$ . $V_{OH} = 2.3$			-1	mA	
Low-Level Output Current	$I_{OL}$	$V_{CC} = \text{Min}$ . $V_{OL} = 0.5$	8			mA	

**AC ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 3.0\text{V}$  to  $3.6\text{V}$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	$t_{WI}$		20% of Tap 5 $t_{PLH}$			ns	9
Input-to-Tap Delay Tolerance (Delays $\leq 40\text{ns}$ )	$t_{PLH}$ , $t_{PHL}$	$+25^\circ\text{C}$ 3.3V	-2	Table 1	+2	ns	1, 3, 4, 7, 10
		$0^\circ\text{C}$ to $+70^\circ\text{C}$	-3	Table 1	+3	ns	1, 2, 3, 4, 7, 10
		$-40^\circ\text{C}$ to $+85^\circ\text{C}$	-4	Table 1	+4	ns	1, 2, 3, 4, 7, 10
Input-to-Tap Delay Tolerance (Delays $> 40\text{ns}$ )	$t_{PLH}$ , $t_{PHL}$	$+25^\circ\text{C}$ 3.3V	-5	Table 1	+5	%	1, 3, 4, 7, 10
		$0^\circ\text{C}$ to $+70^\circ\text{C}$	-8	Table 1	+8	%	1, 2, 3, 4, 7, 10
		$-40^\circ\text{C}$ to $+85^\circ\text{C}$	-13	Table 1	+13	%	1, 2, 3, 4, 7, 10
Output Rise or Fall Time	$t_{OF}$ , $t_{OR}$			2.0	2.5	ns	
Power-Up Time	$t_{PU}$				200	$\mu\text{s}$	
Input Period	Period		$2(t_{WI})$			ns	9

## CAPACITANCE

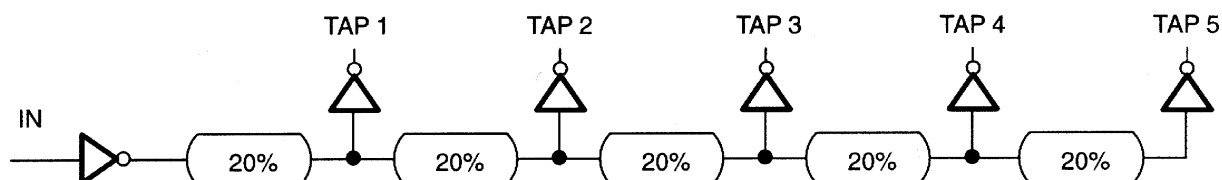
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$			5	10	pF	

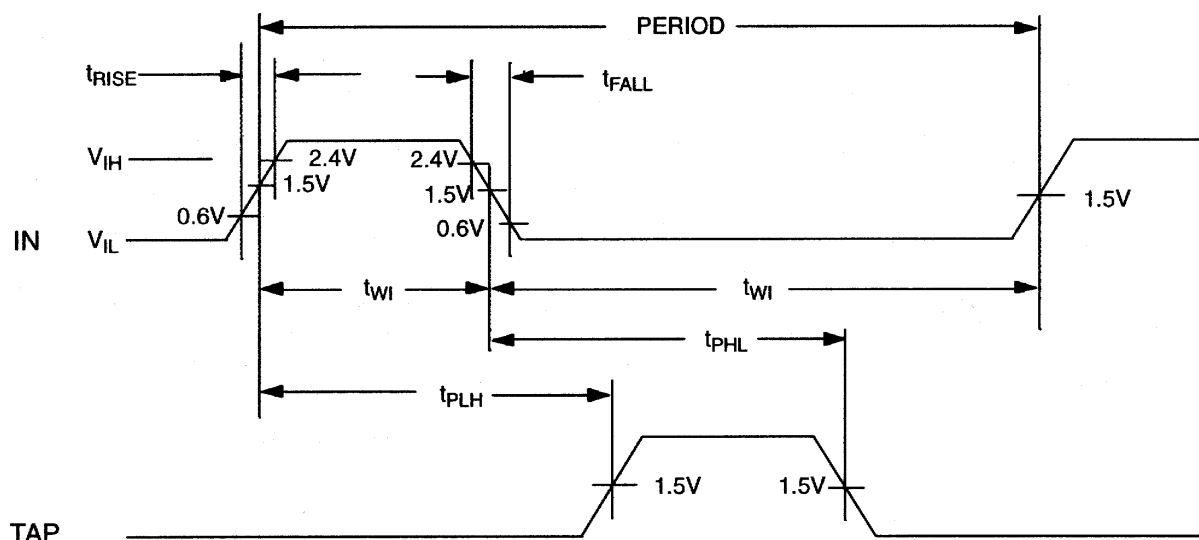
### NOTES:

- 1) Initial tolerances are  $\pm$  with respect to the nominal value at  $+25^\circ\text{C}$  and  $V_{CC} = 3.3\text{V}$  for both leading and trailing edge.
- 2) Temperature and voltage tolerance is with respect to the nominal delay value over the stated temperature range, and a supply-voltage range of  $3.0\text{V}$  to  $3.6\text{V}$ .
- 3) All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps also slow down; TAP 3 can never be faster than TAP 2.
- 4) Intermediate delay values are available on a custom basis. For further information, contact the factory at [custom.oscillators@maximintegrated.com](mailto:custom.oscillators@maximintegrated.com).
- 5) All voltages are referenced to ground.
- 6) Measured with outputs open.
- 7) See *Test Conditions* section at the end of this data sheet.
- 8) Frequencies higher than  $1\text{MHz}$  result in higher  $I_{CC}$  values.
- 9) At or near maximum frequency the delay accuracy can vary and will be application sensitive (i.e., decoupling, layout).
- 10) The “-75” version is specified and tested with an additional  $2\text{ns}$  of tolerance on the specified minimum input-to-tap delay tolerance parameters for TAP 1 to TAP 3. Delay values for TAP 4 to TAP 5 meet data sheet specifications.

**Figure 1. LOGIC DIAGRAM**



**Figure 2. TIMING DIAGRAM: SILICON DELAY LINE**



## TERMINOLOGY

**Period:** The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

**$t_{WI}$  (Pulse Width):** The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

**$t_{RISE}$  (Input Rise Time):** The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

**$t_{FALL}$  (Input Fall Time):** The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

**$t_{PLH}$  (Time Delay, Rising):** The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

**$t_{PHL}$  (Time Delay, Falling):** The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

## TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1100L. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

## TEST CONDITIONS INPUT:

Ambient Temperature:	25°C ±3°C
Supply Voltage ( $V_{CC}$ ):	3.3V ±0.1V
Input Pulse:	High = 3.0V ±0.1V Low = 0.0V ±0.1V
Source Impedance:	50Ω max
Rise and Fall Time:	3.0ns max (measured between 10% and 90%)
Pulse Width:	500ns (1μs for -500 version)
Period:	1μs (2μs for -500 version)

## OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

**Note: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.**

Figure 3. TEST CIRCUIT

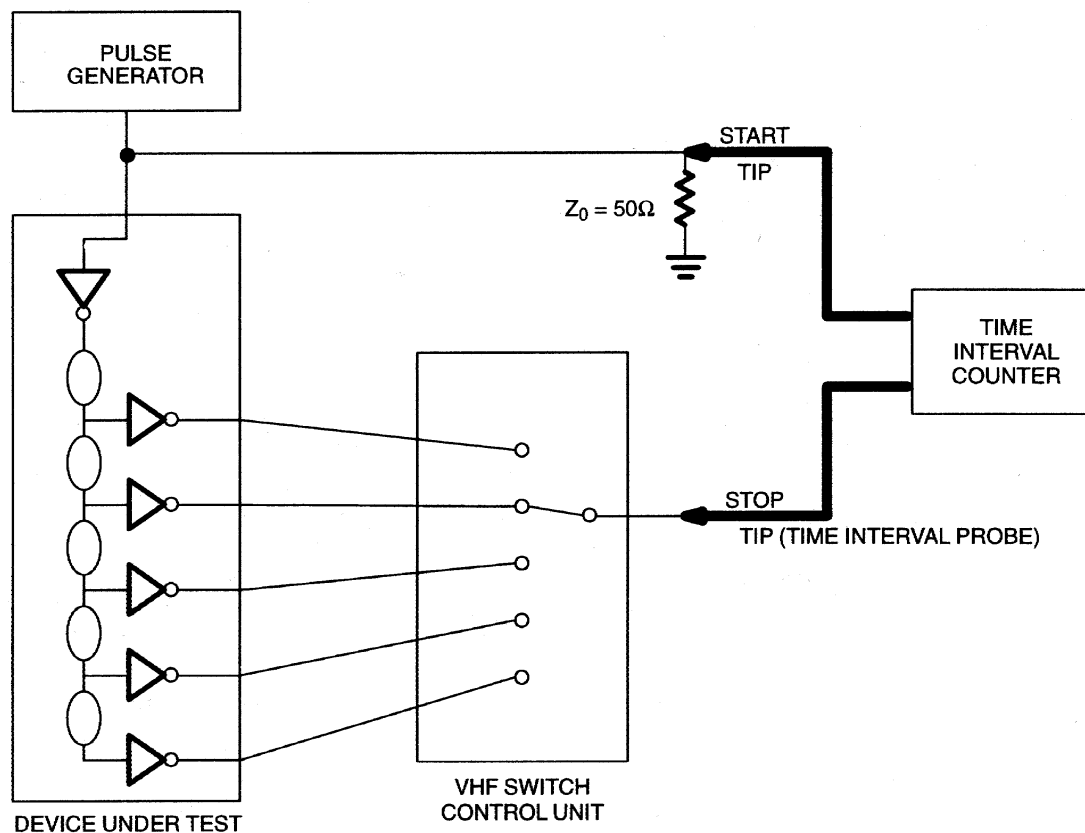


Table 1. DS1100L PART NUMBER DELAY

PART DS1100L-xxx	NOMINAL DELAYS (ns)				
	TAP 1	TAP 2	TAP 3	TAP 4	TAP 5
-20	4	8	12	16	20
-25	5	10	15	20	25
-30	6	12	18	24	30
-35	7	14	21	28	35
-40	8	16	24	32	40
-45	9	18	27	36	45
-50	10	20	30	40	50
-60	12	24	36	48	60
-75	15	30	45	60	75
-100	20	40	60	80	100
-125	25	50	75	100	125
-150	30	60	90	120	150
-175	35	70	105	140	175
-200	40	80	120	160	200
-250	50	100	150	200	250
-300	60	120	180	240	300
-500	100	200	300	400	500

**ORDERING INFORMATION**

PART	TEMP RANGE	PIN-PACKAGE
DS1100LZ-xxx	-40°C to +85°C	8 SO
DS1100LZ-xxx/T&R	-40°C to +85°C	8 SO
DS1100LZ-xxx+	-40°C to +85°C	8 SO
DS1100LZ-xxx+T	-40°C to +85°C	8 SO
DS1100LU-xxx	-40°C to +85°C	8 $\mu$ MAX
DS1100LU-xxx/T&R	-40°C to +85°C	8 $\mu$ MAX
DS1100LU-xxx+	-40°C to +85°C	8 $\mu$ MAX
DS1100LU-xxx+T	-40°C to +85°C	8 $\mu$ MAX

xxx Denotes total time delay (ns) (see Table 1).

+Denotes a lead(Pb)-free/RoHS-compliant package.

T&R and T = Tape and reel.

**PACKAGE INFORMATION**

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO (150 mils)	S8+4	<a href="#">21-0041</a>	<a href="#">90-0096</a>
8 $\mu$ MAX	U8+1	<a href="#">21-0036</a>	<a href="#">90-0092</a>

**REVISION HISTORY**

<b>REVISION DATE</b>	<b>DESCRIPTION</b>	<b>PAGES CHANGED</b>
3/11	Changed $\mu$ SOP package type to $\mu$ MAX; updated the <i>Absolute Maximum Ratings</i> section; added the customer support email address to the electrical characteristics Note 4; added the <i>Ordering Information</i> and <i>Package Information</i> tables	1–6
10/11	Added continuous power dissipation numbers to the <i>Absolute Maximum Ratings</i> section; added Note 10 to the Input-to-Tap Delay Tolerance (Delays $\leq$ 40ns) parameter in the <i>AC Electrical Characteristics</i> table	2, 3
7/15	Revised Note 10 and revised <i>AC Electrical Characteristics</i> table	2, 3

7 of 7

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

**Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000**