

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

10-Tap Silicon Delay Line

DS1110

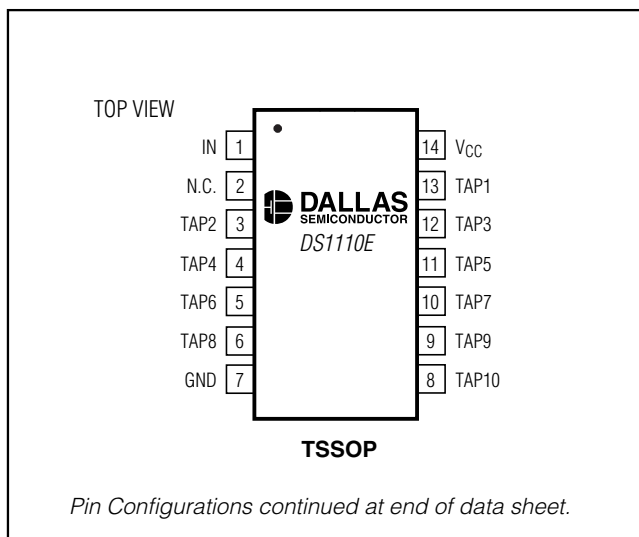
General Description

The DS1110 delay line is an improved replacement for the DS1010. It has ten equally spaced taps providing delays from 5ns to 500ns. The devices are offered in a standard 16-pin SO or 14-pin TSSOP. The DS1110 series delay lines provide a nominal accuracy of $\pm 5\%$ or $\pm 2\text{ns}$, whichever is greater, at 5V and $+25^\circ\text{C}$. The DS1110 reproduces the input logic state at the tap 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1110 is designed to produce both leading- and trailing-edge delays with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs.

Applications

- Communications Equipment
- Medical Devices
- Automated Test Equipment
- PC Peripheral Devices

Pin Configurations



Features

- ◆ All-Silicon, 5V, 10-Tap Delay Line
- ◆ Improved, Drop-In Replacement for the DS1010
- ◆ 10 Taps Equally Spaced
- ◆ Delays are Stable and Precise
- ◆ Leading- and Trailing-Edge Accuracy
- ◆ Delay Tolerance $\pm 5\%$ or $\pm 2\text{ns}$, whichever is Greater, at 5V and $+25^\circ\text{C}$
- ◆ Economical
- ◆ Auto-Insertable, Low Profile
- ◆ Low-Power CMOS
- ◆ TTL/CMOS Compatible
- ◆ Vapor Phase, IR, and Wave Solderable
- ◆ Fast-Turn Prototypes
- ◆ Delays Specified Over Commercial and Industrial Temperature Ranges
- ◆ Custom Delays Available
- ◆ Standard 16-Pin SO or 14-Pin TSSOP

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1110E-XXX	-40°C to +85°C	14 TSSOP
DS1110S-XXX	-40°C to +85°C	16 SO

Selector Guide appears at end of data sheet.

10-Tap Silicon Delay Line

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground-0.5V to +6.0V
 Operating Temperature Range-40°C to +85°C

Storage Temperature Range-55°C to +125°C
 Soldering Temperature.....See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	4.75	5.0	5.25	V
High-Level Input Voltage	V_{IH}	(Note 1)	2.4		$V_{CC} + 0.3$	V
Low-Level Input Voltage	V_{IL}	(Note 1)	-0.3		+0.8	V
Input Leakage Current	I_I	$0V \leq V_I \leq V_{CC}$	-1.0		+1.0	μA
Active Current	I_{CC}	$V_{CC} = \text{max}$, period = min (Note 2)		40	150	mA
High-Level Output Current	I_{OH}	$V_{CC} = \text{min}$, $V_{OH} = 2.3V$			-1.0	mA
Low-Level Output Current	I_{OL}	$V_{CC} = \text{min}$, $V_{OL} = 0.5V$	12			mA

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width	t_{WI}	(Note 6)	10% of tap 10			ns
Input-to-Tap Delay (Delays $\leq 40ns$)	t_{PLH} t_{PHL}	+25°C, 5.0V (Notes 3, 5, 6, 7, 9)	-2	Table 1	+2	ns
		0°C to +70°C (Notes 4-7)	-3	Table 1	+3	
		-40°C to +85°C (Notes 4-7)	-4	Table 1	+4	
Input-to-Tap Delay (Delays > 40ns)	t_{PLH} t_{PHL}	+25°C, 5.0V (Notes 3, 5, 6, 7, 9)	-5	Table 1	+5	%
		0°C to +70°C (Notes 4-7)	-8	Table 1	+8	
		-40°C to +85°C (Notes 4-7)	-13	Table 1	+13	
Power-Up Time	t_{PU}				200	ms
Input Period	Period	(Note 8)	2(t_{WI}) or 20, whichever is greater			ns

10-Tap Silicon Delay Line

DS1110

CAPACITANCE

($T_A = +25^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}			5	10	pF

Note 1: All voltages are referenced to ground.

Note 2: Measured with outputs open.

Note 3: Initial tolerances are \pm with respect to the nominal value at $+25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$ for both leading and trailing edges.

Note 4: Temperature and voltage tolerances are with respect to the actual delay measured over stated temperature range and a 4.75V to 5.25V range.

Note 5: Intermediate delay values are available on a custom basis.

Note 6: See *Test Conditions* section.

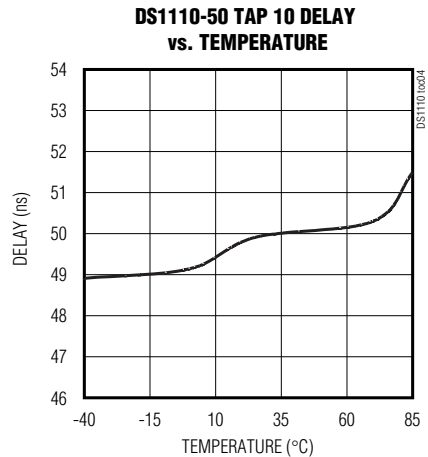
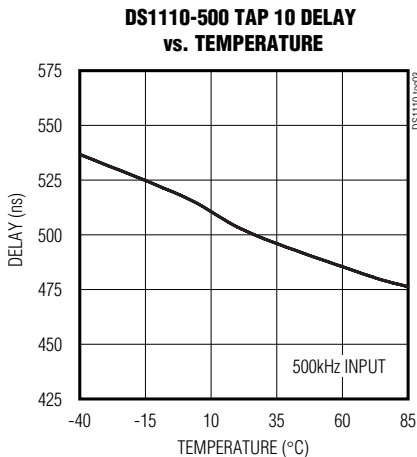
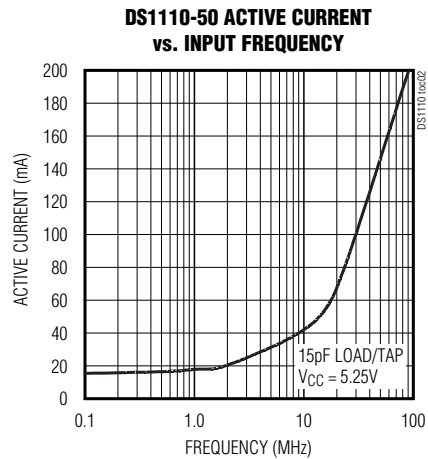
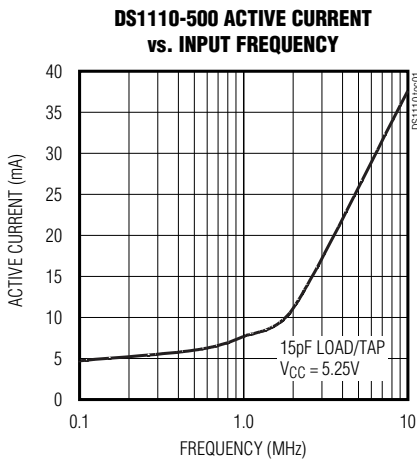
Note 7: All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if tap 1 slows down, all other taps also slow down; tap 3 can never be faster than tap 2.

Note 8: Pulse width and period specifications may be exceeded; however, accuracy is application sensitive (decoupling, layout, etc.)

Note 9: For Tap 1 delays greater than 20ns, the tolerance is $\pm 3\text{ns}$ or $\pm 5\%$, whichever is greater.

Typical Operating Characteristics

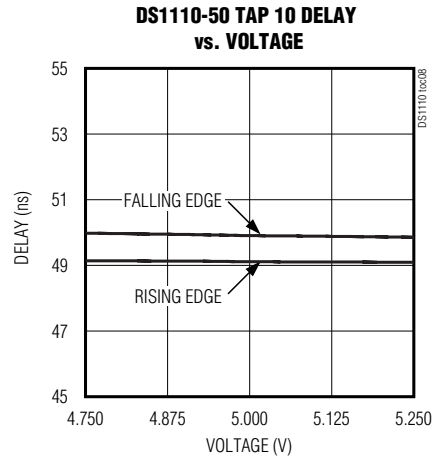
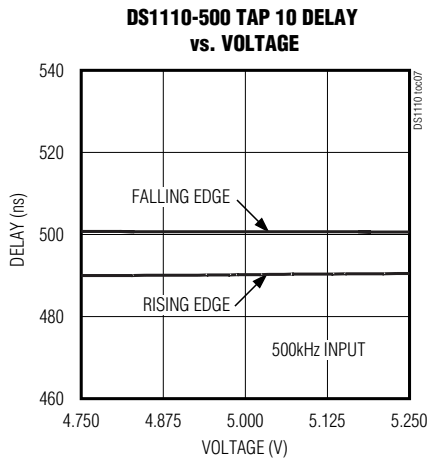
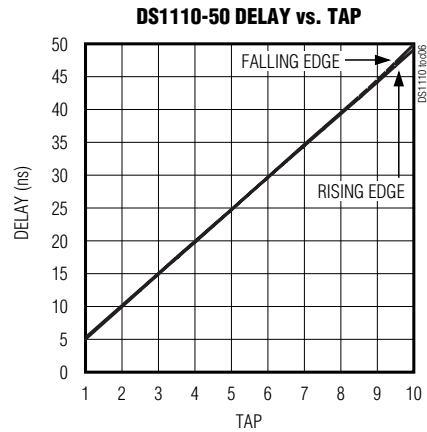
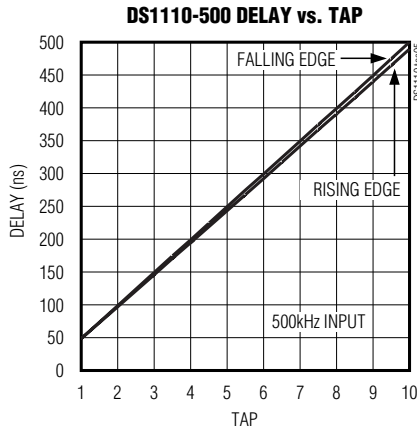
($V_{CC} = 5.0\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



10-Tap Silicon Delay Line

Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN		NAME	FUNCTION
TSSOP	SO		
1	1	IN	Input
2	2, 3, 15	N.C.	No Connection
7	8	GND	Ground
13, 3, 12, 4, 11, 5, 10, 6, 9, 8	14, 4, 13, 5, 12, 6, 11, 7, 10, 9	Tap 1–Tap 10	Tap Output Number
14	16	V _{CC}	5.0V

10-Tap Silicon Delay Line

DS1110

Detailed Description

The DS1110 delay line is an improved replacement for the DS1010. It has ten equally spaced taps providing delays from 5ns to 500ns. The devices are offered in a standard 16-pin SO or 14-pin TSSOP. The DS1110 series delay lines provide a nominal accuracy of $\pm 5\%$ or $\pm 2\text{ns}$, whichever is greater, at 5V and $+25^\circ\text{C}$. The DS1110 reproduces the input logic state at the tap 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1110 is designed to produce both leading- and trailing-edge delays with equal precision. Each tap is capable of driving up to ten 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests call 972-371-4348.

Table 1. Part Number by Delay (t_{PHL} , t_{PLH})

PART	TOTAL DELAY* (ns)	DELAY/TAP (ns)
DS1110-50	50	5
DS1110-60	60	6
DS1110-75	75	7.5
DS1110-80	80	8
DS1110-100	100	10
DS1110-125	125	12.5
DS1110-150	150	15
DS1110-175	175	17.5
DS1110-200	200	20
DS1110-250	250	25
DS1110-300	300	30
DS1110-350	350	35
DS1110-400	400	40
DS1110-450	450	45
DS1110-500	500	50

*Custom delays are available.

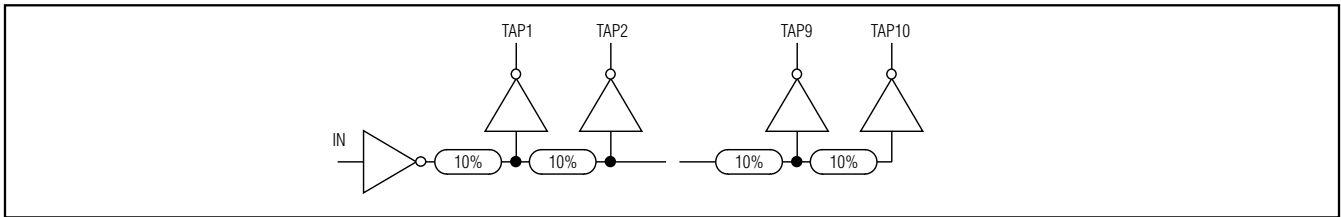


Figure 1. Logic Diagram

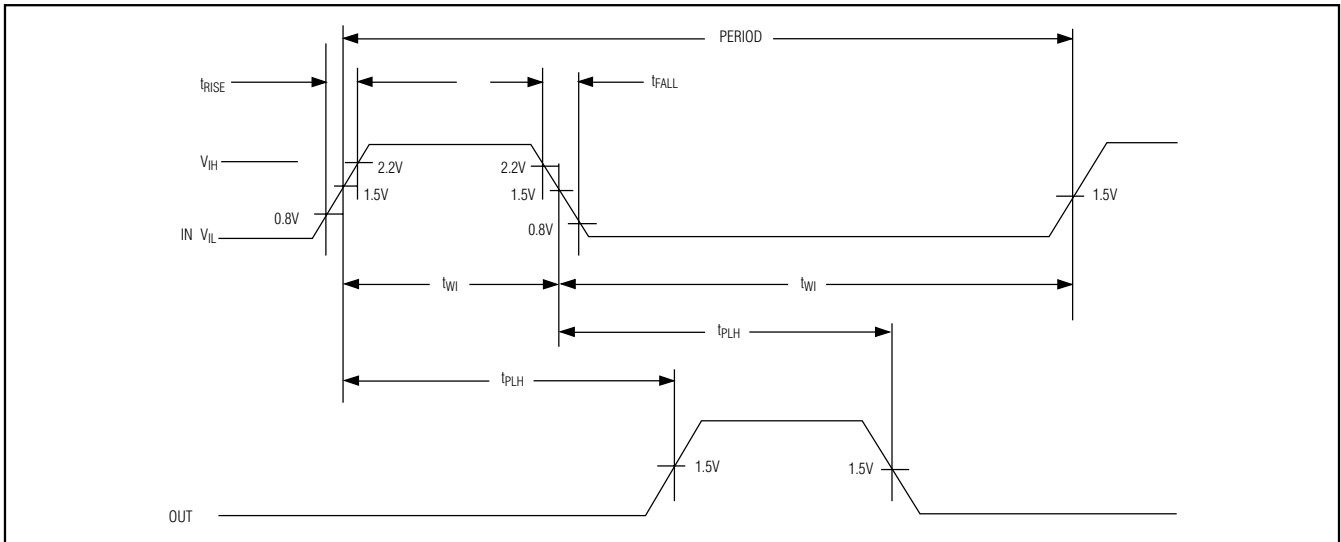


Figure 2. Timing Diagram: Silicon Delay Line

10-Tap Silicon Delay Line

Terminology

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

twl (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

tRISE (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

tFALL (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

Test Setup Description

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1110. A precision pulse generator under software control produces the input waveform. Time delays are measured by a time interval counter (20ps resolution) connected

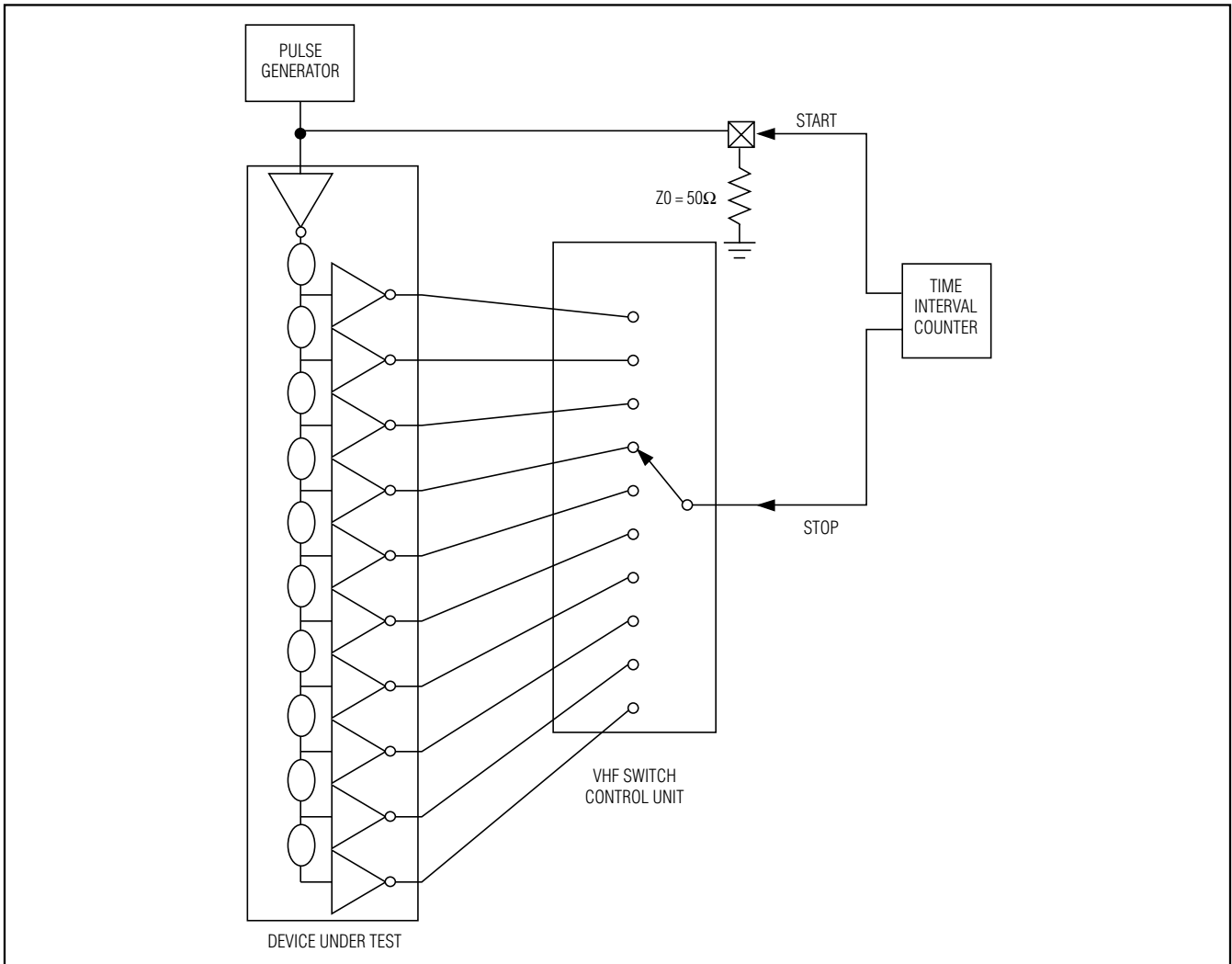


Figure 3. Test Circuit

10-Tap Silicon Delay Line

DS1110

between the input and each tap. Each tap is selected and connected to the counter by a VHF switch-control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE-488 bus.

Output

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

Chip Information

TRANSISTOR COUNT: 6813

Table 2. Test Conditions

INPUT	CONDITION
Ambient Temperature	+25°C ±3°C
Supply Voltage (V _{CC})	5.0V ±0.1V
Input Pulse	High = 3.0V ±0.1V
	Low = 0.0V ±0.1V
Source Impedance	50Ω max
Rise and Fall Time	3ns max
Pulse Width	500ns (1μs for -500ns)
Period	1μs (2μs for -500ns)

Note: The above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

Selector Guide

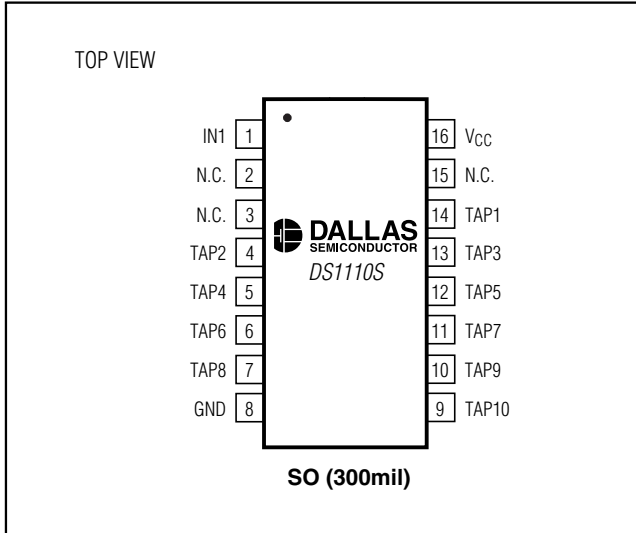
PART	TEMP RANGE	PIN-PACKAGE	TOTAL DELAY (ns)*
DS1110E-50	-40°C to +85°C	14 TSSOP	50
DS1110E-60	-40°C to +85°C	14 TSSOP	60
DS1110E-75	-40°C to +85°C	14 TSSOP	75
DS1110E-80	-40°C to +85°C	14 TSSOP	80
DS1110E-100	-40°C to +85°C	14 TSSOP	100
DS1110E-125	-40°C to +85°C	14 TSSOP	125
DS1110E-150	-40°C to +85°C	14 TSSOP	150
DS1110E-175	-40°C to +85°C	14 TSSOP	175
DS1110E-200	-40°C to +85°C	14 TSSOP	200
DS1110E-250	-40°C to +85°C	14 TSSOP	250
DS1110E-300	-40°C to +85°C	14 TSSOP	300
DS1110E-350	-40°C to +85°C	14 TSSOP	350
DS1110E-400	-40°C to +85°C	14 TSSOP	400
DS1110E-450	-40°C to +85°C	14 TSSOP	450
DS1110E-500	-40°C to +85°C	14 TSSOP	500

PART	TEMP RANGE	PIN-PACKAGE	TOTAL DELAY (ns)*
DS1110S-50	-40°C to +85°C	16 SO	50
DS1110S-60	-40°C to +85°C	16 SO	60
DS1110S-75	-40°C to +85°C	16 SO	75
DS1110S-80	-40°C to +85°C	16 SO	80
DS1110S-100	-40°C to +85°C	16 SO	100
DS1110S-125	-40°C to +85°C	16 SO	125
DS1110S-150	-40°C to +85°C	16 SO	150
DS1110S-175	-40°C to +85°C	16 SO	175
DS1110S-200	-40°C to +85°C	16 SO	200
DS1110S-250	-40°C to +85°C	16 SO	250
DS1110S-300	-40°C to +85°C	16 SO	300
DS1110S-350	-40°C to +85°C	16 SO	350
DS1110S-400	-40°C to +85°C	16 SO	400
DS1110S-450	-40°C to +85°C	16 SO	450
DS1110S-500	-40°C to +85°C	16 SO	500

*Custom delays are available.

10-Tap Silicon Delay Line

Pin Configurations (continued)



Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

8 Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600