阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

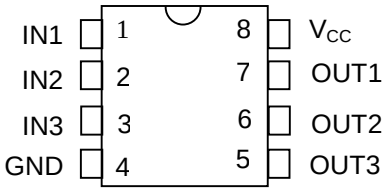
DS1033
3-in-1 Low Voltage Silicon Delay Line

www.dalsemi.com

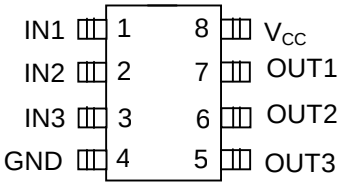
FEATURES

- All-silicon timing circuit
- Three independent buffered delays
- Initial delay tolerance ±1.5 ns
- Stable and precise over temperature and voltage
- Leading and trailing edge precision preserves the input symmetry
- Standard 8-pin DIP, 8-pin SOIC
- Vapor phasing, IR and wave solderable
- Available in Tape and Reel

PIN ASSIGNMENT



DS1033M 8-Pin DIP
See Mech. Drawings Section



DS1033Z 8-Pin SOIC (150-mil)
See Mech. Drawings Section

PIN DESCRIPTION

IN1-IN3	- Input Signals
OUT1-OUT3	- Output Signals
NC	- No Connection
V_{CC}	- Supply Voltage
GND	- Ground
(Sub)	- Internal substrate connection, do not make any external connections to these pins

DESCRIPTION

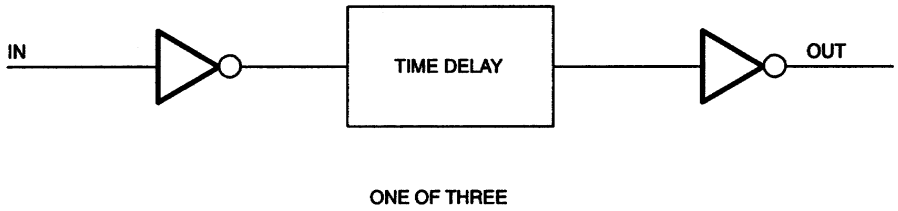
The DS1033 series is a low-power +3.3 Volt version of the DS1035. It is characterized for operation over the range of 2.7V to 3.6V.

The DS1033 series of delay lines have three independent logic buffered delays in a single package. It is available in a standard 8-pin DIP, 150-mil 8-pin mini-SOIC.

The device features precise leading and trailing edge accuracies. It has the inherent reliability of an all-silicon delay line solution. The DS1033's nominal tolerance is ±1.5 ns and an additional tolerance over temperature and voltage of ±1.0 ns for the faster delays. Detailed specifications are shown in Table 1.

Standard delay values are indicated in Table 1. Customers may contact Dallas Semiconductor at (972) 371-4348 for further information.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH} , t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns) (note 1)	INITIAL TOLERANCE (note 1)	TOLERANCE OVER TEMPERATURE AND VOLTAGE (note 2)	
			V_{CC}=3.3V ± 0.3V	V_{CC}=2.7V
DS1033-8	8/8/8	±1.5 ns	±1.0 ns	±1.5 ns
DS1033-10	10/10/10	±1.5 ns	±1.0 ns	±1.5 ns
DS1033-12	12/12/12	±1.5 ns	±1.0 ns	±1.5 ns
DS1033-15	15/15/15	±1.5 ns	±1.5 ns	±2.0 ns
DS1033-20	20/20/20	±1.5 ns	±1.5 ns	±2.5 ns
DS1033-25	25/25/25	±2.0 ns	±2.0 ns	±3.5 ns
DS1033-30	30/30/30	±2.0 ns	±2.0 ns	±5.0 ns

NOTES:

1. Nominal conditions are +25°C and V_{CC}=+3.3 volts.

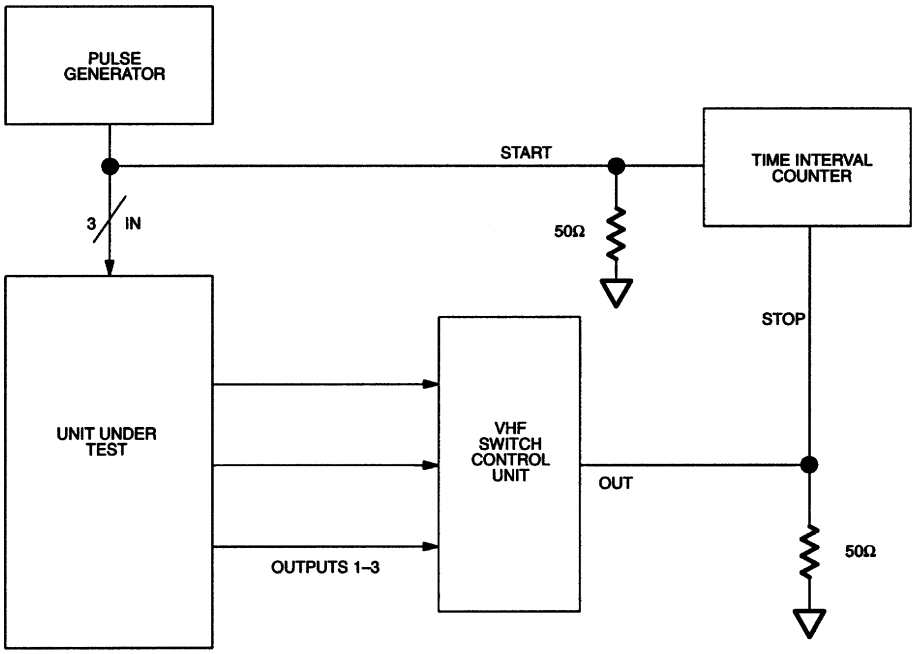
2. Temperature range of 0°C to 70°C.

3. Delay accuracy is for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1033. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1033 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1033 TEST CIRCUIT Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(T_A =0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7	3.3	3.6	V
Active Current	I_{CC}	V_{CC}=3.6V Period=1µs			25	mA
High Level Input Voltage	V_{IH}		2.0		V_{CC} +0.5	V
Low Level Input Voltage	V_{IL}		-0.5		0.8	V
Input Leakage	I_L	$0V \le V_I \le V_{CC}$	-1.0		1.0	µA
High Level Output Current	I_{OH}	V_{CC}=2.7V V_{OH}=2V			-1.0	mA
Low Level Output Current	I_{OL}	V_{CC}=2.7V V_{OL}=0.4V	8			mA

AC ELECTRICAL CHARACTERISTICS

(T_A =+25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	2
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	2
Input-to-Tap Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	
Output Rise or Fall Time	t_{OR}, t_{OF}		2.0 3.0	2.5 3.5	ns ns	3 4
Power-up Time	t_{PU}			100	ms	

CAPACITANCE

(T_A =+25°C)

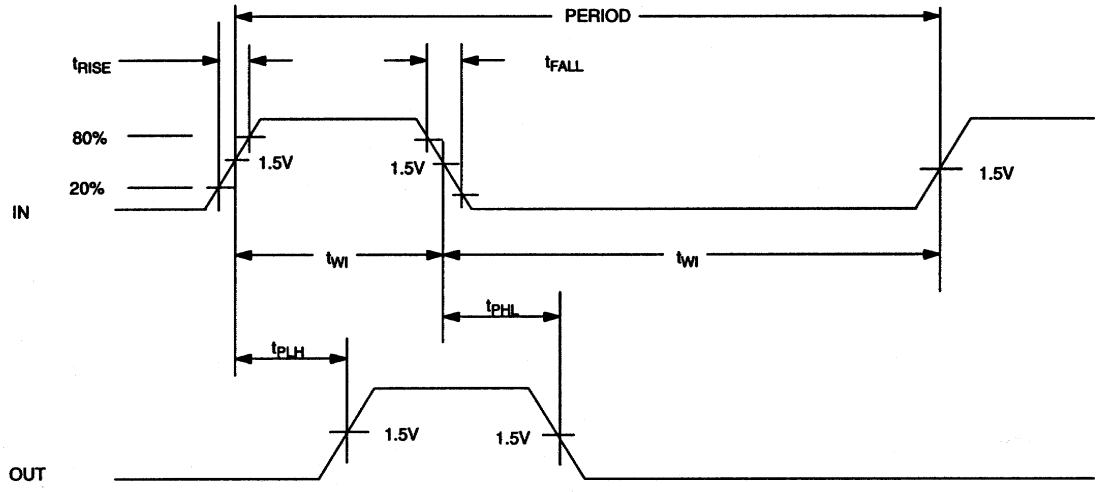
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 3.3V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω max.
Rise and Fall Time: 3.0 ns max. - Measured between 0.6V and 2.4V.
Pulse Width: 500 ns
Pulse Period: 1 µs
Output Load Capacitance: 15 pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.

Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

TIMING DIAGRAM



NOTES:

1. All voltages are referenced to ground.

2. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application-sensitive with respect to de-coupling, layout, etc.

3. V_{CC}=3.3V ± 10%.

4. V_{CC}=2.7V.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI}(Pulse Width): The elapsed time on the pulse between the 1.5 volt point on the leading edge and the 1.5 volt point on the trailing edge, or the 1.5 volt point on the trailing edge and the 1.5 volt point on the leading edge.

t_{RISE}(Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL}(Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH}(Time Delay, Rising): The elapsed time between the 1.5 volt point on the leading edge of the input pulse and the 1.5 volt point on the leading edge of the output pulse.

t_{PHL}(Time Delay, Falling): The elapsed time between the 1.5 volt point on the falling edge of the input pulse and the 1.5 volt point on the falling edge of the output pulse.