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19-6078; Rev 11/11

DS1248/DS1248P
1024K NV SRAM with Phantom Clock

FEATURES

- Real-Time Clock (RTC) Keeps Track of Hundredths of Seconds, Minutes, Hours, Days, Date of the Month, Months, and Years
- 128K x 8 NV SRAM Directly Replaces Volatile Static RAM or EEPROM
- Embedded Lithium Energy Cell Maintains Calendar Operation and Retains RAM Data
- Watch Function is Transparent to RAM Operation
- Automatic Leap Year Compensation Valid Up to 2100
- Full 10% Operating Range
- Over 10 Years of Data Retention in the Absence of Power
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- DIP Module Only

  Standard 32-Pin JEDEC Pinout
- Underwriters Laboratories (UL) Recognized (www.maxim-ic.com/qa/info/ul/)
- PowerCap Module Board Only

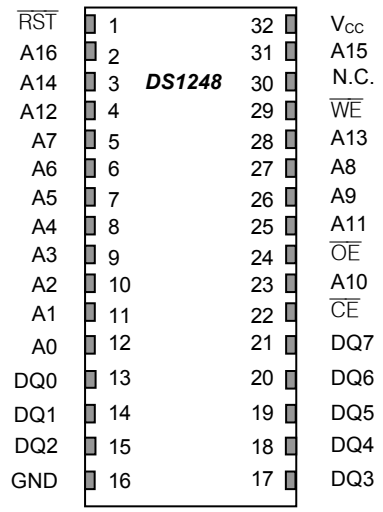
  Surface Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal

  Replaceable Battery (PowerCap)

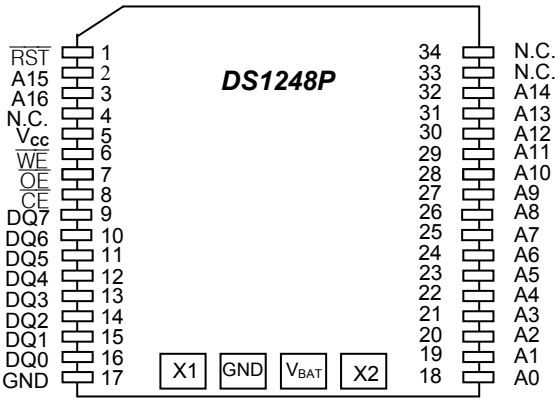
  Pin-for-Pin Compatible with DS1244P and DS1251P

PIN CONFIGURATIONS

TOP VIEW



Encapsulated DIP (740-mil Flush)



PowerCap Module Board (Uses DS9034PCX+ PowerCap)

ORDERING INFORMATION

PART	TEMP RANGE	V_{CC} RANGE	PIN-PACKAGE
DS1248Y-70+	0°C to +70°C	5V ±10%	32 EDIP
DS1248Y-70IND+	-40°C to +85°C	5V ±10%	32 EDIP
DS1248YP-70+	0°C to +70°C	5V ±10%	34 PowerCap*
DS1248W-120+	0°C to +70°C	3.3V ±10%	32 EDIP
DS1248W-120IND+	-40°C to +85°C	3.3V ±10%	32 EDIP
DS1248WP-120+	0°C to +70°C	3.3V ±10%	34 PowerCap*
DS1248WP-120IND+	-40°C to +85°C	3.3V ±10%	34 PowerCap*

+ Denotes a lead(Pb)-free/RoHS-compliant package.
** DS9034PCX+ or DS9034I-PCX+ (PowerCap) required. Must be ordered separately.*

DETAILED DESCRIPTION

The DS1248 1024K NV SRAM with phantom clock is a fully static, nonvolatile RAM (organized as 128K words by 8 bits) with a built-in real-time clock. The DS1248 has a self-contained lithium energy source and control circuitry, which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and writes protection is unconditionally enabled to prevent garbled data in both the memory and real-time clock.

PACKAGES

The DS1248 is available in two packages: 32-pin DIP and 34-pin PowerCap module. The 32-pin DIP style module integrates the crystal, lithium energy source, and silicon in one package. The 34-pin PowerCap module board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1248P after completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery because of the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap module board and PowerCap are ordered separately and shipped in separate containers.

PIN DESCRIPTION

PIN		NAME	FUNCTION
EDIP	PowerCap		
1	1	$\overline{RST}$	Active-Low Reset Input. This pin has an internal pullup resistor connected to V_{CC}.
2	3	A16	Address Inputs
3	32	A14	
4	30	A12	
5	25	A7	
6	24	A6	
7	23	A5	
8	22	A4	
9	21	A3	
10	20	A2	
11	19	A1	
12	18	A0	
23	28	A10	
25	29	A11	
26	27	A9	
27	26	A8	
28	31	A13	
31	2	A15	
13	16	DQ0	Data In/Data Out
14	15	DQ1	
15	14	DQ2	
17	13	DQ3	
18	12	DQ4	
19	11	DQ5	
20	10	DQ6	
21	9	DQ7	
22	8	$\overline{CE}$	Active-Low Chip-Enable Input
24	7	$\overline{OE}$	Active-Low Output-Enable Input
29	6	$\overline{WE}$	Active-Low Write-Enable Input
30	4, 33, 34	N.C.	No Connect
32	5	V_{CC}	Power-Supply Input
16	17	GND	Ground

RAM READ MODE

The DS1248 executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (chip enable) is active (low). The unique address specified by the 17 address inputs (A0–A16) defines which of the 128k bytes of data is to be accessed. Valid data will be available to the eight data-output drivers within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (output enable) access times and states are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$, rather than address access.

RAM WRITE MODE

The DS1248 is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The 5V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. However, when V_{CC} is below the power-fail point, V_{PF} (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. When V_{CC} falls below the battery switch point, V_{SO} (battery supply level), device power is switched from the V_{CC} pin to the backup battery. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels.

The 3.3V device is fully accessible and data can be written or read only when V_{CC} is greater than V_{PF}. When V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{BAT}, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BAT}, the device power is switched from V_{CC} to the backup supply (V_{BAT}) when V_{CC} drops below V_{BAT}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels.

All control, data, and address signals must be powered down when V_{CC} is powered-down.

PHANTOM CLOCK OPERATION

Communication with the phantom clock is established by pattern recognition on a serial bit stream of 64 bits, which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses that occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the phantom clock, and memory access is inhibited.

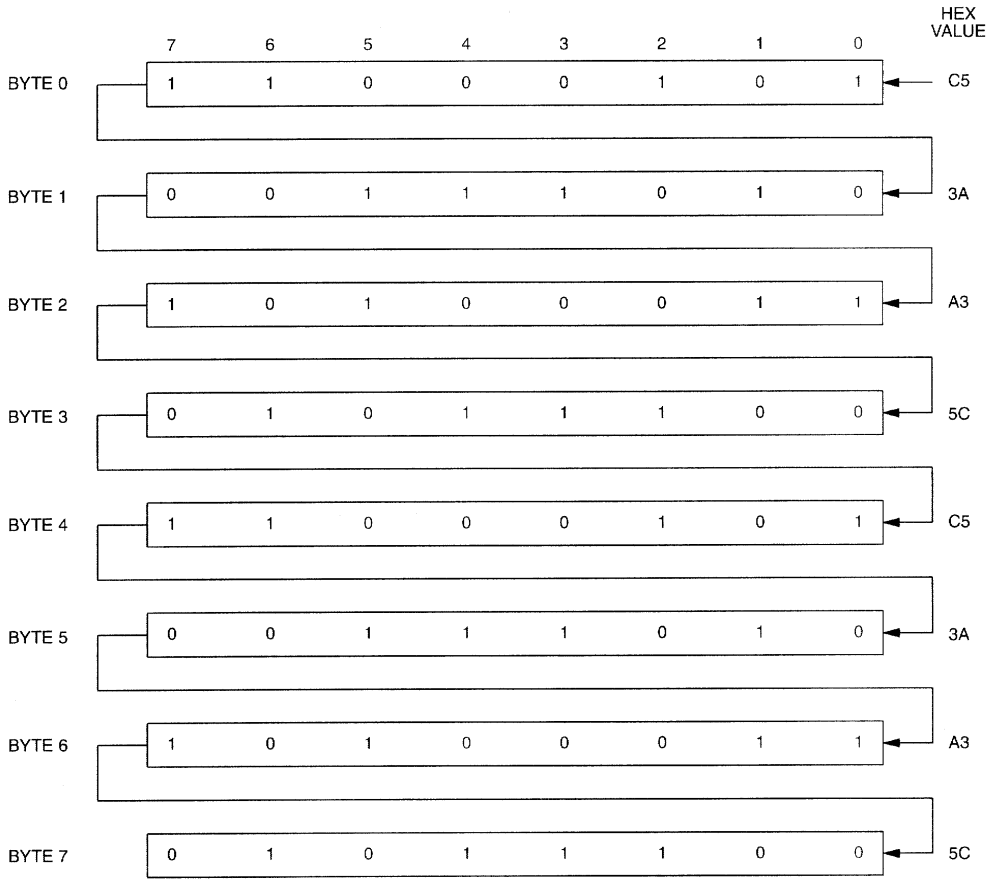
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable, output enable, and write enable. Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the phantom clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 write cycles are used only to gain access to the phantom clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the phantom clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a phantom clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (Figure 1). With a correct match for 64 bits, the phantom clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the phantom clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the phantom clock.

PHANTOM CLOCK REGISTER INFORMATION

The phantom clock information is contained in eight registers of 8 bits, each of which is sequentially accessed 1 bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the phantom clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

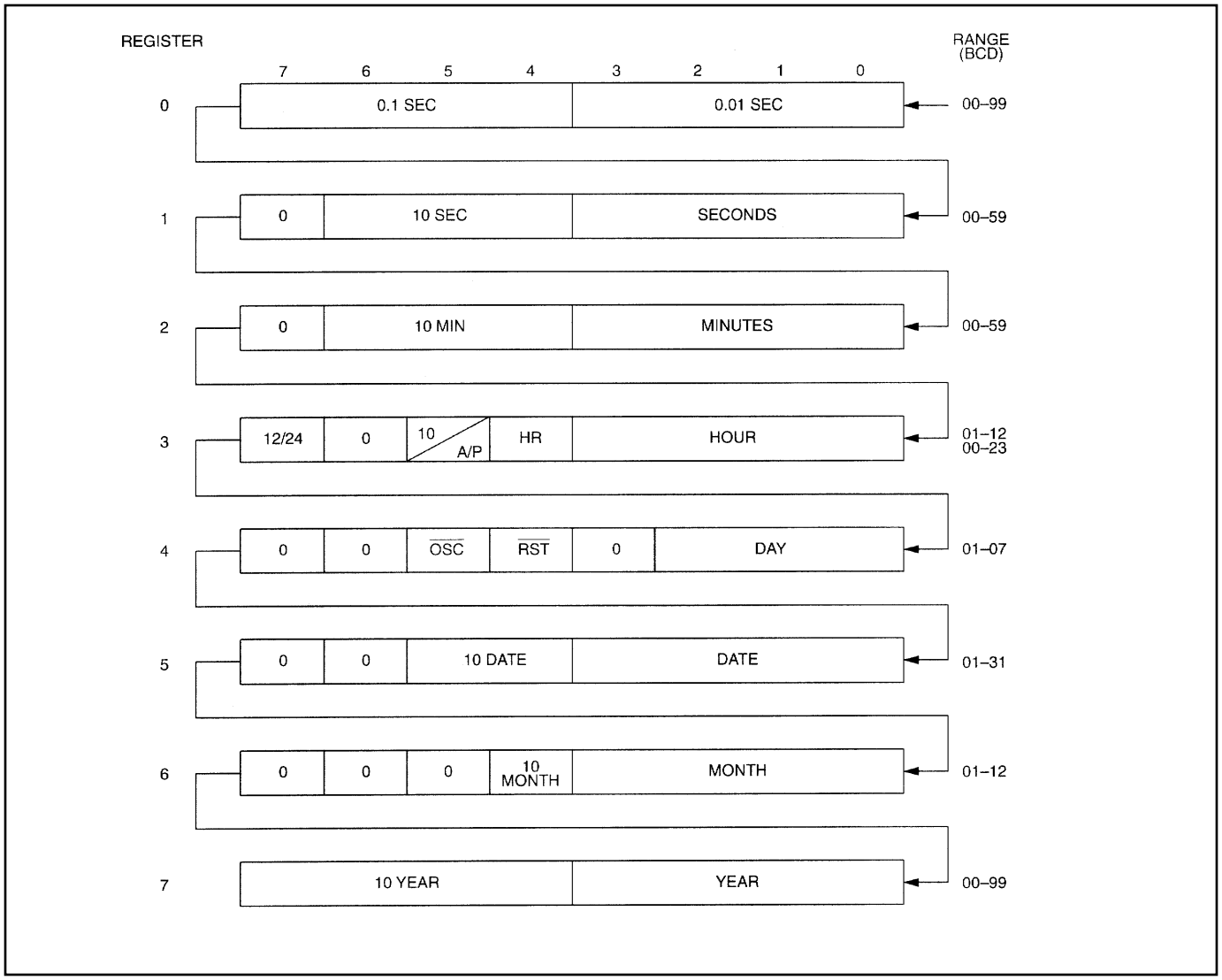
Data contained in the phantom clock register is in binary-coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

Figure 1. Phantom Clock Register Definition



NOTE: THE PATTERN RECOGNITION IN HEX IS C5, 3A, A3, 5C, C5, 3A, A3, 5C. THE ODDS OF THIS PATTERN BEING ACCIDENTALLY DUPLICATED AND CAUSING INADVERTENT ENTRY TO THE PHANTOM CLOCK IS LESS THAN 1 IN 10^{19}. THIS PATTERN IS SENT TO THE PHANTOM CLOCK LSB TO MSB.

Figure 2. Phantom Clock Register Definition



AM/PM/12/24-MODE

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20–23 hours).

OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{RST}$ and oscillator functions. Bit 4 controls the $\overline{RST}$ (pin 1). When the $\overline{RST}$ bit is set to logic 1, the $\overline{RST}$ input pin is ignored. When the $\overline{RST}$ bit is set to logic 0, a low input on the $\overline{RST}$ pin will cause the phantom clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits, which will always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

BATTERY LONGEVITY

The DS1248 has a lithium power source that is designed to provide energy for clock activity and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1248 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1248 is shipped from Maxim with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery-backup operation. Actual life expectancy of the DS1248 will be much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.
See "Conditions of Acceptability" at www.maxim-ic.com/TechSupport/QA/ntrl.htm

CLOCK ACCURACY (DIP MODULE)

The DS1248 is guaranteed to keep time accuracy to within ±1 minute per month at +25°C. The clock is calibrated at the factory by Maxim using special calibration nonvolatile tuning elements and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary.

CLOCK ACCURACY (POWERCAP MODULE)

The DS1248P and DS9034PCX are each individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ±1.53 minutes per month (35ppm) at +25°C.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground (5V product)……..-0.3V to +6.0V
(3.3V product)…… …..-0.3V to +4.6V

Storage Temperature Range
EDIP .....-40ºC to +85ºC
PowerCap .....-55°C to +125°C
Lead Temperature (soldering, 10s) ..... +260°C
Note: EDIP is wave or hand-soldered only.
Soldering Temperature (reflow, PowerCap) .....+260°C

This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

OPERATING RANGE

RANGE	TEMP RANGE (NONCONDENSING)	V_{CC} (V)
Commercial	0°C to +70°C	3.3 ±10% or 5 ±10%
Industrial	-40°C to +85°C	3.3 ±10% or 5 ±10%

RECOMMENDED OPERATING CONDITIONS

Over the Operating Range

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{CC} = 5V ±10%	V_{IH}	2.2		V_{CC} + 0.3	V	11
	V_{CC} = 3.3V ±10%		2.0		V_{CC} + 0.3		
Logic 0	V_{CC} = 5V ±10%	V_{IL}	-0.3		+0.8	V	11
	V_{CC} = 3.3V ±10%		-0.3		+0.6		

DC ELECTRICAL CHARACTERISTICS

Over the Operating Range (5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current at 2.4V	I_{OH}	-1.0			mA	
Output Current at 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 70ns	I_{CC01}			85	mA	
Write Protection Voltage	V_{PF}	4.25	4.37	4.50	V	11
Battery Switchover Voltage	V_{SO}		V_{BAT}		V	11

DC ELECTRICAL CHARACTERISTICS

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current at 2.4V	I_{OH}	-1.0			mA	
Output Current at 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5	7	mA	
Standby Current $\overline{CE} = V_{CC}$ - 0.5V	I_{CCS2}		2.0	3.0	mA	
Operating Current t_{CYC} = 70ns	I_{CC01}			50	mA	
Write Protection Voltage	V_{PF}	2.80	2.86	2.97	V	11
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	11

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS

Over the Operating Range (5V)

PARAMETER	SYMBOL	DS1248Y-70		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	70		ns	
Access Time	t_{ACC}		70	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High-Z from Deselection	t_{OD}		25	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	70		ns	
Write Pulse Width	t_{WP}	50		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	0		ns	
Output High-Z from $\overline{WE}$	t_{ODW}		25	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	30		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	5		ns	4

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS

Over the Operating Range (5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	65			ns	
$\overline{CE}$ Access Time	t_{CO}			55	ns	
$\overline{OE}$ Access Time	t_{OE}			55	ns	
$\overline{CE}$ to Output Low-Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low-Z	t_{OEE}	5			ns	
$\overline{CE}$ to Output High-Z	t_{OD}			25	ns	5
$\overline{OE}$ to Output High-Z	t_{ODO}			25	ns	5
Read Recovery	t_{RR}	10			ns	
Write Cycle Time	t_{WC}	65			ns	
Write Pulse Width	t_{WP}	55			ns	3
Write Recovery	t_{WR}	10			ns	10
Data Setup Time	t_{DS}	30			ns	4
Data Hold Time	t_{DH}	0			ns	4
$\overline{CE}$ Pulse Width	t_{CW}	60			ns	
$\overline{RST}$ Pulse Width	t_{RST}	65			ns	

POWER-DOWN/POWER-UP TIMING

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from $V_{PF(max)}$ to $V_{PF(min)}$($\overline{CE}$ at V_{PF})	t_F	300			µs	
V_{CC} Slew from $V_{PF(min)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Slew from $V_{PF(max)}$ to $V_{PF(min)}$($\overline{CE}$ at V_{PF})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}	1.5		2.5	ms	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time	t_{DR}	10			years	9

Warning: Under no circumstances are negative undershoots of any amplitude allowed when device is in battery-backup mode.

MEMORY AC ELECTRICAL CHARACTERISTICS

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	DS1248W-120		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	120		ns	
Access Time	t_{ACC}		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High-Z from Deselection	t_{OD}		40	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	120		ns	
Write Pulse Width	t_{WP}	90		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	20		ns	10
Output High-Z from $\overline{WE}$	t_{ODW}		40	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	50		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		ns	4

PHANTOM CLOCK AC ELECTRICALCHARACTERISTICS

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low-Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low-Z	t_{OEE}	5			ns	
$\overline{CE}$ to Output High-Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High-Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	3
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	45			ns	4
Data Hold Time	t_{DH}	0			ns	4
$\overline{CE}$ Pulse Width	t_{CW}	105			ns	
$\overline{RST}$ Pulse Width	t_{RST}	120			ns	

POWER-DOWN/POWER-UP TIMING

Over the Operating Range (3.3V)

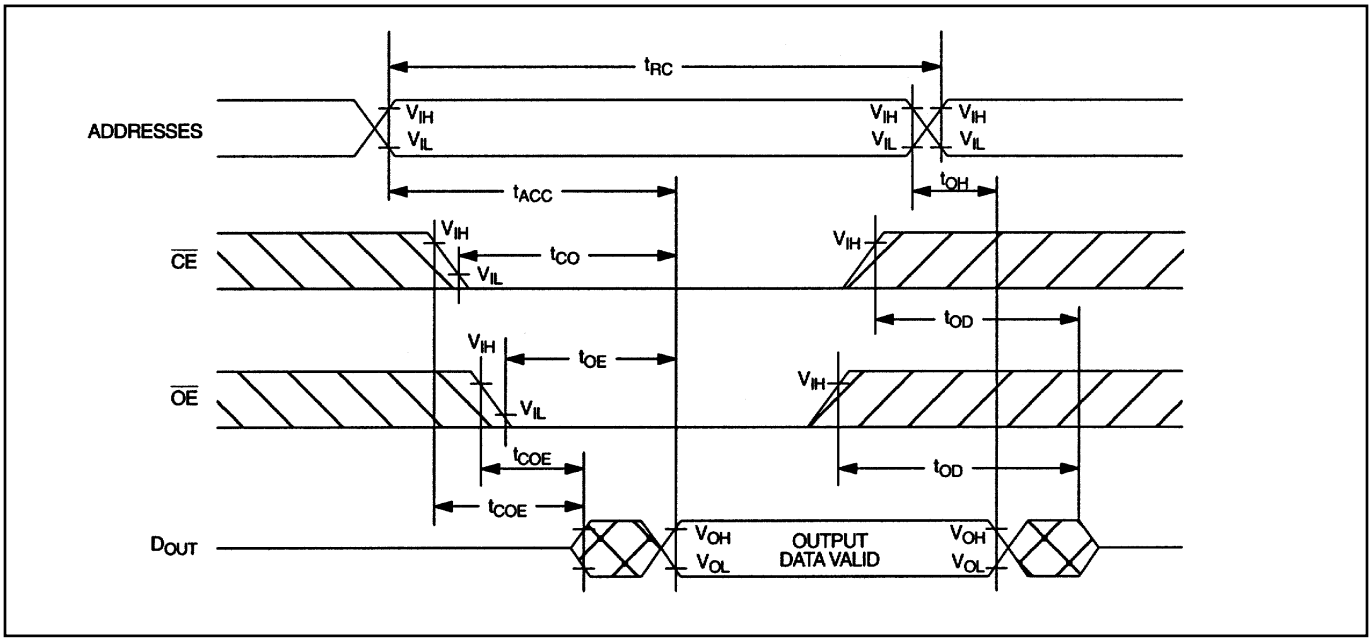
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from $V_{PF(MAX)}$ to $V_{PF(MIN)}$($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from $V_{PF(MAX)}$ to $V_{PF(MIN)}$($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}	1.5		2.5	ms	

(T_A = +25°C)

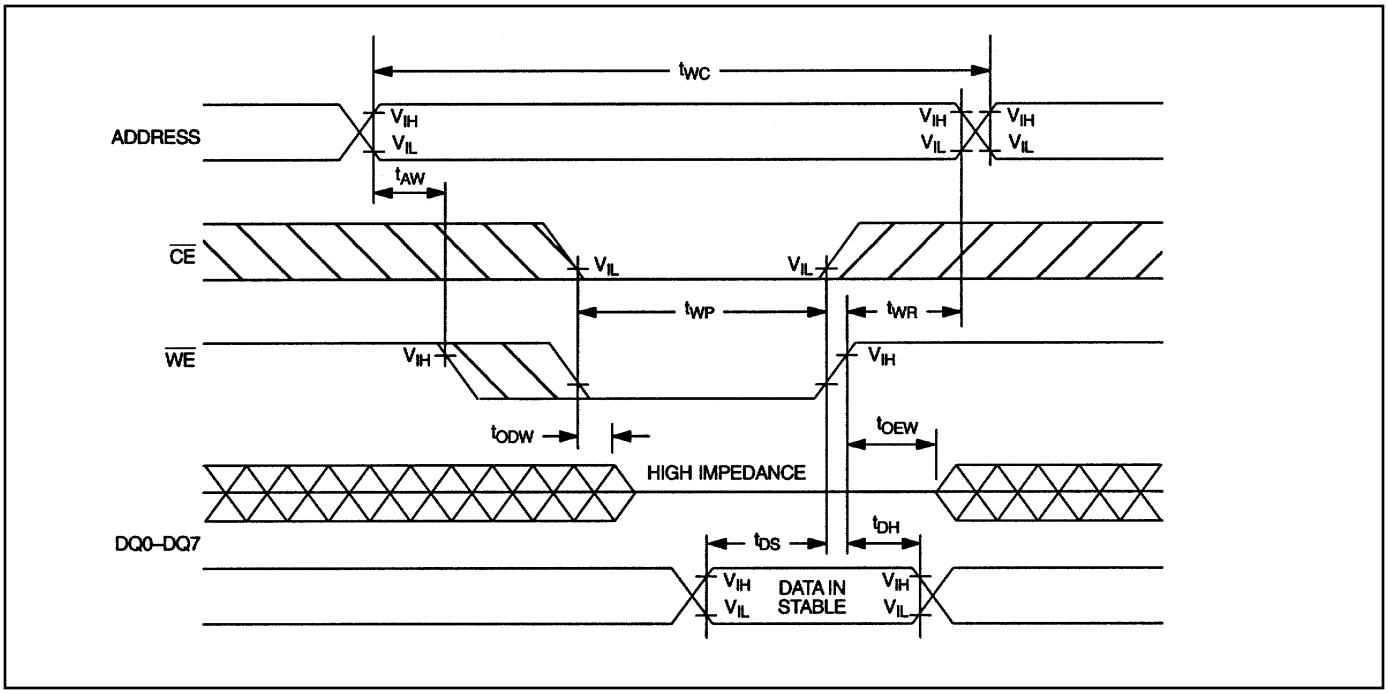
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time	t_{DR}	10			years	9

Warning: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

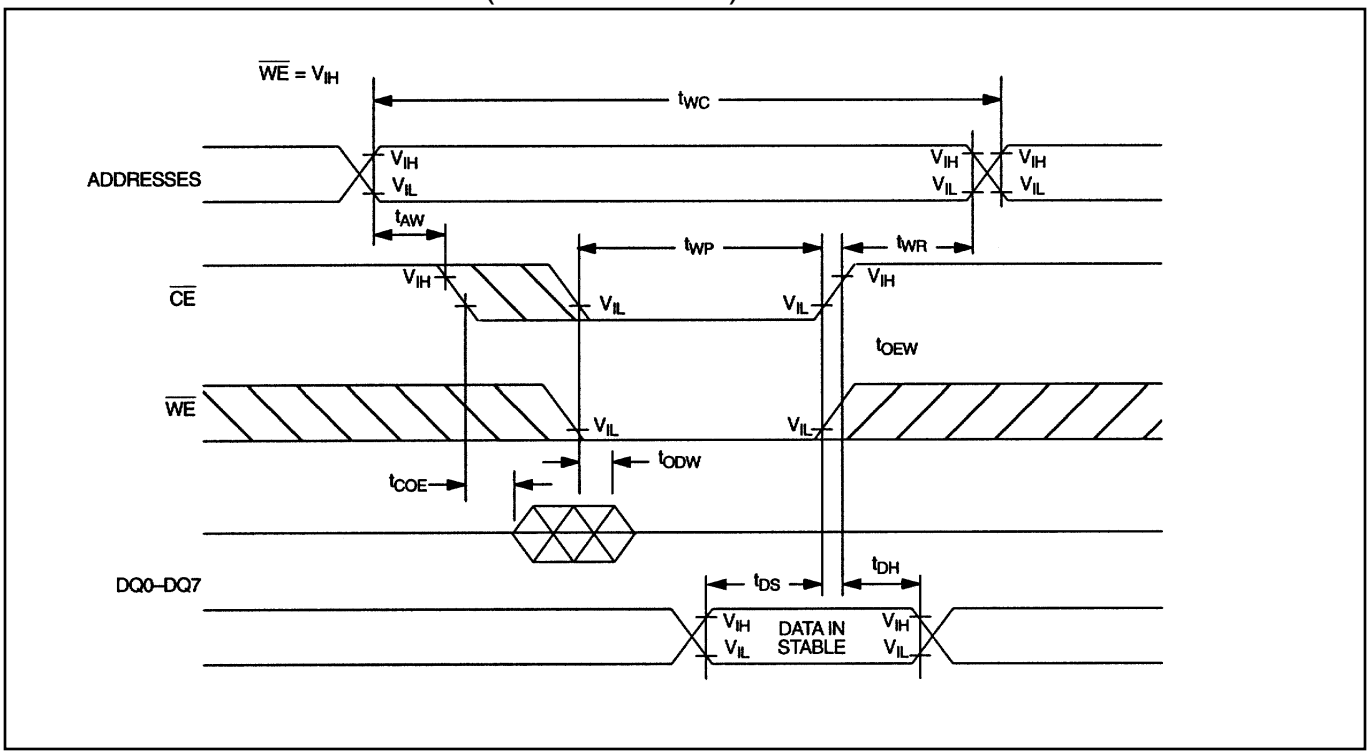
MEMORY READ CYCLE (Note 1)



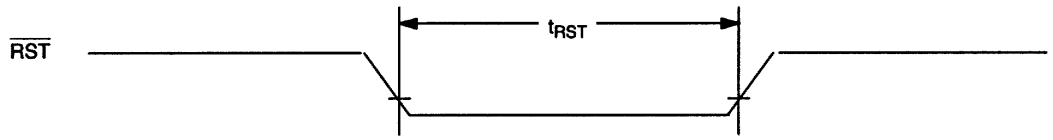
MEMORY WRITE CYCLE 1 (Notes 2, 6, and 7)



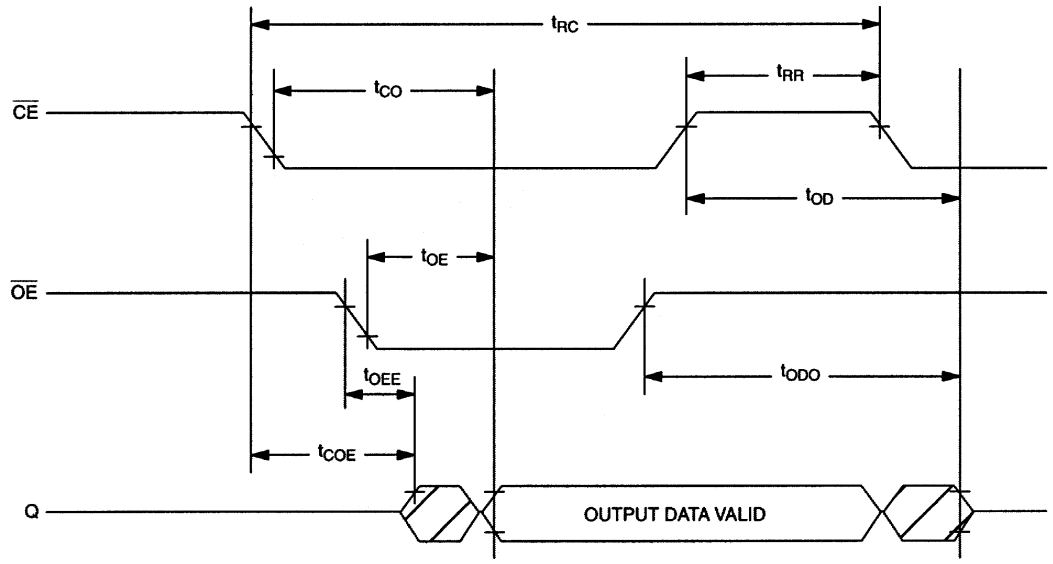
MEMORY WRITE CYCLE 2 (Notes 2 and 8)



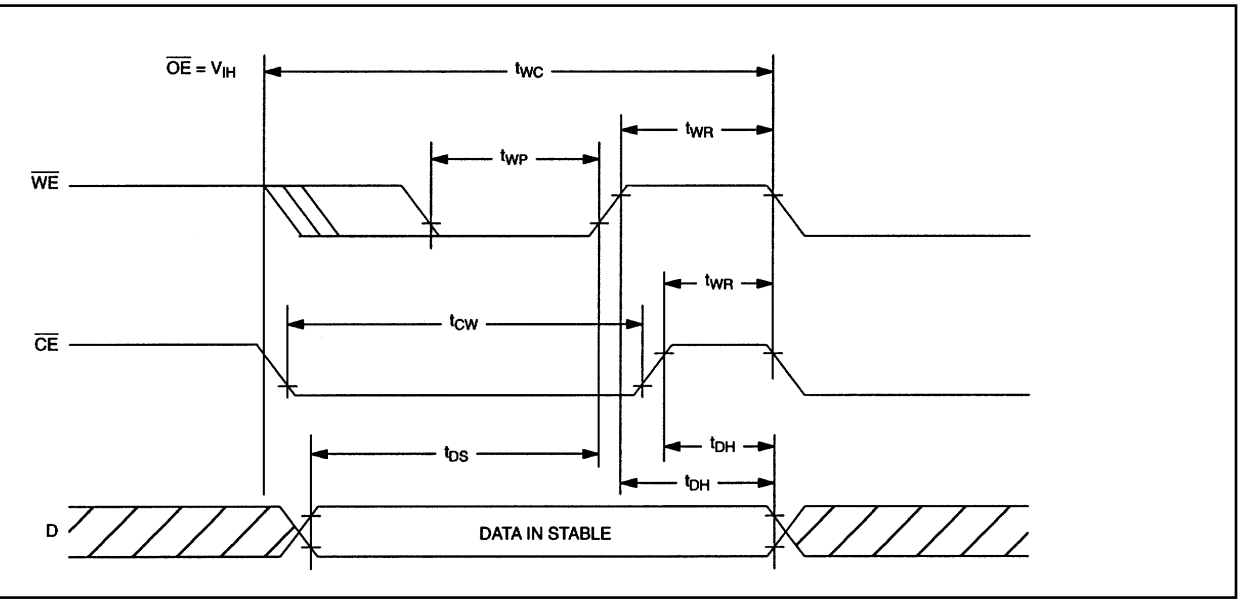
RESET FOR PHANTOM CLOCK



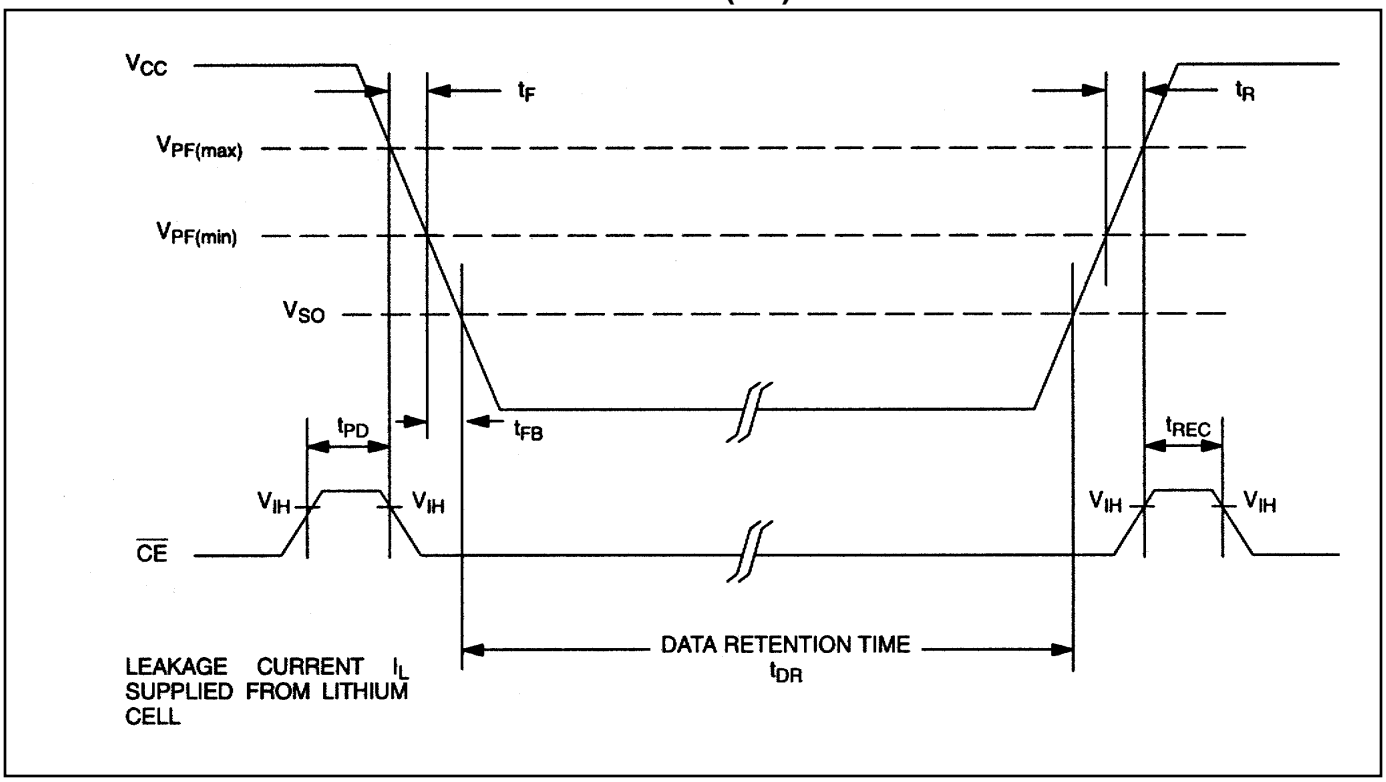
READ CYCLE TO PHANTOM CLOCK



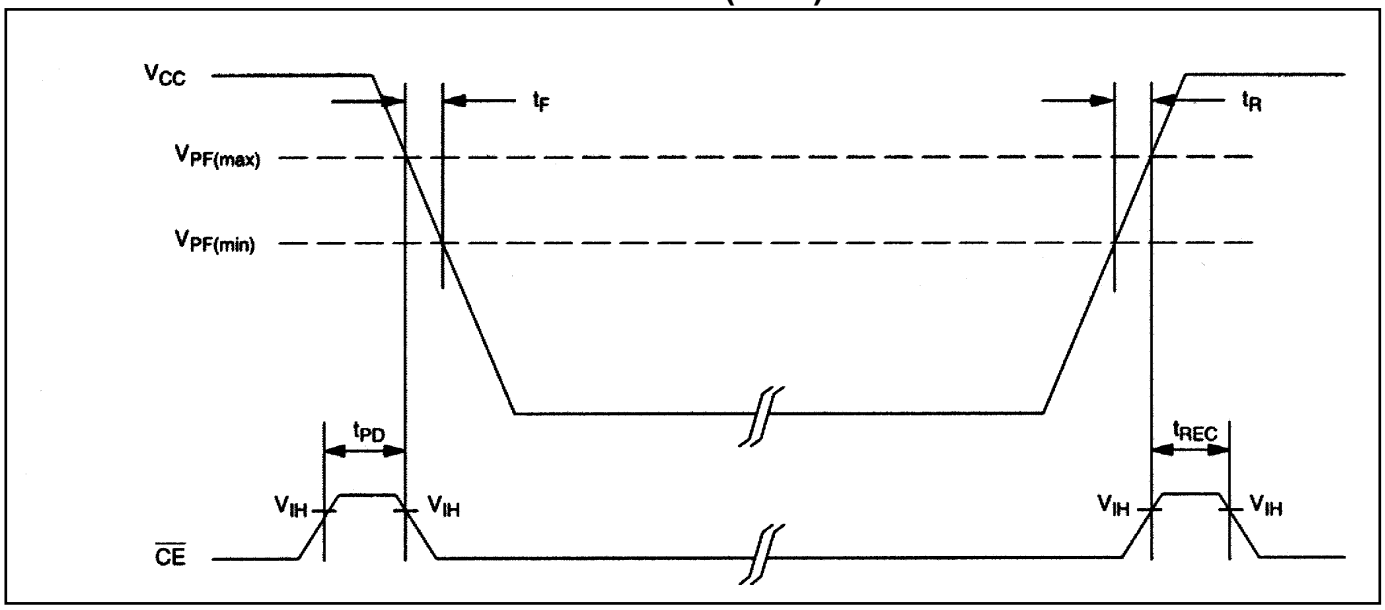
WRITE CYCLE TO PHANTOM CLOCK



POWER-DOWN/POWER-UP CONDITION (5V)



POWER-DOWN/POWER-UP CONDITION (3.3V)



AC TEST CONDITIONS

Output Load: 50pF + 1TTL Gate
Input Pulse Levels: 0 to 3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) $\overline{WE}$ is high for a read cycle.
2) $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{CE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3) t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5) These parameters are sampled with a 50pF load and are not 100% tested.
6) If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high-impedance state during this period.
7) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
8) If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9) The expected t_{DR} is defined as cumulative time in the absence of V_{CC} with the clock oscillator running.
10) t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11) Voltages are referenced to ground.
12) $\overline{RST}$ (Pin 1) has an internal pullup resistor.
13) RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used. See the PowerCap package drawing for details regarding the PowerCap package.

PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 EDIP	MDT32+2	21-0245	—
34 PWRCP	PC2+3	21-0246	—

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
11/11	Updated the *Features*, *Ordering Information*, *AM/PM/12/24-MODE*, *Absolute Maximum Ratings*, and *Package Information* sections	1, 2, 7, 9, 18

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