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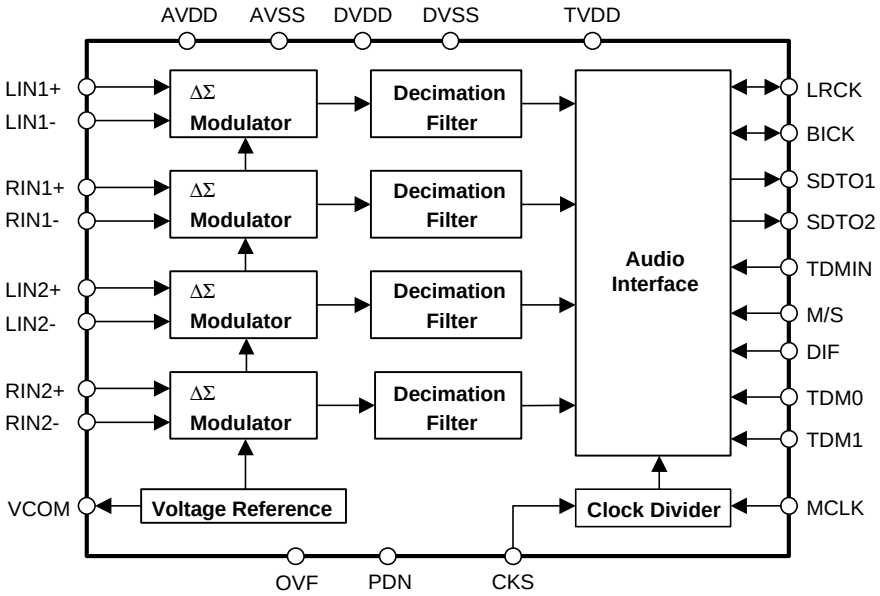
AK5384
107dB 24-Bit 96kHz 4-Channel ADC

GENERAL DESCRIPTION

The AK5384 is a 4-channel A/D Converter with wide sampling rate of 8kHz ~ 96kHz and is suitable for Multi-channel audio system. The AK5384 achieves high accuracy and low cost by using Enhanced dual bit ΔΣ techniques. The AK5384 supports master mode and TDM format. Therefore, the AK5384 is suitable for multi-channel audio system.

FEATURES

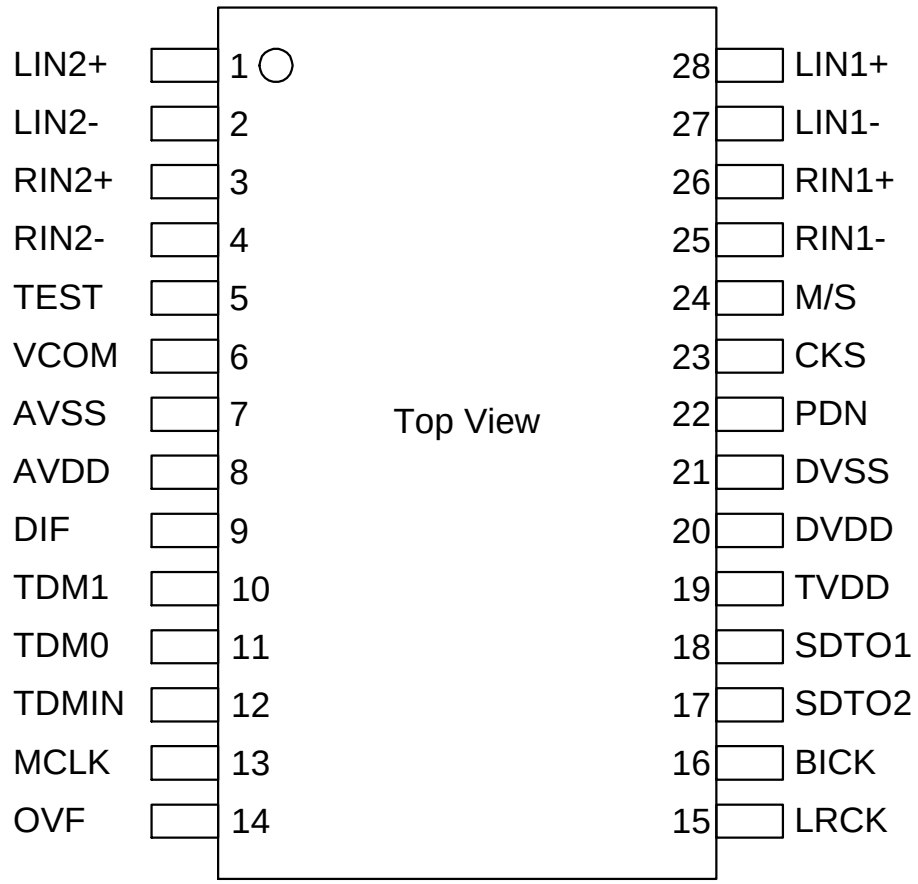
- **4-Channel ΔΣ ADC**
- **Differential Inputs**
- **Digital HPF for DC-Offset Cancel**
- **S/(N+D): 100dB@5V for 48kHz**
- **DR: 107dB@5V for 48kHz**
- **S/N: 107dB@5V for 48kHz**
- **Sampling Rate Ranging from 8kHz to 96kHz**
- **Master Clock:**
  - **256fs/384fs/512fs/768fs (~ 48kHz)**
  - **256fs/384fs (~ 96kHz)**
- **TTL Digital Input Level**
- **Output format: 24bit MSB justified, I^2S or TDM**
- **Cascade TDM Interface**
- **Master & Slave Mode**
- **Overflow Flag**
- **Power Supply: 4.75 to 5.25V**
- **Power Supply for output buffer: 3.0 to 5.25V**
- **Ta = -40 ~ 85°C**
- **28pin VSOP**



■ Ordering Guide

AK5384VF	–40 ~ +85°C	28pin VSOP (0.65mm pitch)
AKD5384	Evaluation Board for AK5384	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN2+	I	ADC2 Lch Positive Analog Input Pin
2	LIN2−	I	ADC2 Lch Negative Analog Input Pin
3	RIN2+	I	ADC2 Rch Positive Analog Input Pin
4	RIN2−	I	ADC2 Rch Negative Analog Input Pin
5	TEST	I	Test Pin (Connected to AVSS)
6	VCOM	O	Common Voltage Output Pin, AVDD/2 Normally connected to AVSS with a 0.1μF ceramic capacitor in parallel with an electrolytic capacitor less than 2.2μF.
7	AVSS	-	Analog Ground Pin
8	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
9	DIF	I	Audio Interface Format Pin "L" : 24bit MSB justified, "H" : 24bit I^2S Compatible
10	TDM1	I	TDM I/F BICK Frequency Select Pin "L" : 256fs, "H" : 128fs
11	TDM0	I	TDM I/F Format Enable Pin "L" : Normal Mode, "H" : TDM Mode
12	TDMIN	I	TDM Data Input Pin
13	MCLK	I	Master Clock Input Pin
14	OVF	O	Analog Input Overflow Detect Pin This pin goes to "H" if one of four analog inputs overflows.
15	LRCK	I/O	Output Channel Clock Pin "L" Output in Master Mode at Power-down mode.
16	BICK	I/O	Audio Serial Data Clock Pin "L" Output in Master Mode at Power-down mode.
17	SDTO2	O	ADC2 Audio Serial Data Output Pin "L" Output at Power-down mode.
18	SDTO1	O	ADC1 Audio Serial Data Output Pin "L" Output at Power-down mode.
19	TVDD	-	Output Buffer Power Supply Pin, 3.0 ~ 5.25V
20	DVDD	-	Digital Power Supply Pin, 4.75 ~ 5.25V
21	DVSS	-	Digital Ground Pin
22	PDN	I	Power-Down Mode Pin When "L", the circuit is in power-down mode. The AK5384 should always be reset upon power-up.
23	CKS	I	Master Clock Select Pin "L" : 256fs, "H" : 512fs This pin is enabled in Master Mode.
24	M/S	I	Master / Slave Mode Pin "L" : Slave Mode, "H" : Master Mode
25	RIN1−	I	ADC1 Rch Negative Analog Input Pin
26	RIN1+	I	ADC1 Rch Positive Analog Input Pin
27	LIN1−	I	ADC1 Lch Negative Analog Input Pin
28	LIN1+	I	ADC1 Lch Positive Analog Input Pin

Note: All digital input pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	−0.3	6.0	V
	Digital	DVDD	−0.3	6.0	V
	Output buffer	TVDD	−0.3	6.0	V
	|AVSS – DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage		VINA	−0.3	AVDD+0.3	V
Digital Input Voltage					
(Except BICK, LRCK pins)		VIND1	−0.3	DVDD+0.3	V
(BICK, LRCK pins)		VIND2	−0.3	TVDD+0.3	V
Ambient Temperature (Powered applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	5.25	V
	Output buffer	TVDD	3.0	5.0	5.25	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD, DVDD and TVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=TVDD=5.0V; AVSS=DVSS=0V; fs=48kHz, 96kHz; I/F format=Mode 0;
Signal Frequency=1kHz; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz;
unless otherwise specified)

Parameter		min	typ	max	Units
ADC Analog Input Characteristics:					
Resolution				24	Bits
S/(N+D) (−1dBFS)	fs=48kHz	88	100		dB
	fs=96kHz	82	94		dB
DR (−60dBFS)	fs=48kHz, A-weighted	100	107		dB
	fs=96kHz	94	102		dB
S/N	fs=48kHz, A-weighted	100	107		dB
	fs=96kHz	94	102		dB
Interchannel Isolation		90	110		dB
DC Accuracy:					
Interchannel Gain Mismatch			0.1	0.5	dB
Gain Drift			100	150	ppm/°C
Input Voltage	(Note 4)	±2.7	±2.9	±3.1	Vpp
Input Resistance		18	26		kΩ
		11	16		kΩ
Power Supply Rejection	(Note 5)		50	-	dB
Power Supplies					
Power Supply Current (AVDD+DVDD+TVDD)					
Normal Operation (PDN pin = "H", fs=48kHz)	(Note 6)		43	65	mA
Normal Operation (PDN pin = "H", fs=96kHz)	(Note 6)		55	83	mA
Power-down mode (PDN pin = "L")	(Note 7)		10	100	μA

Note 4. This value is the full scale (0dB) of the input voltage. This voltage is input to LIN(RIN)+ and LIN(RIN)− pin, and is proportional to AVDD. (Vin = 0.58 × AVDD)
Note 5. PSR is applied to AVDD, DVDD and TVDD with 1kHz, 50mVpp.
Note 6. AVDD=28mA; DVDD=15mA@48kHz&5V, DVDD=26mA@96kHz&5V(typ).
Note 7. All digital input pins are fixed to DVDD or DVSS.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; AVDD, DVDD=4.75 ~ 5.25V; TVDD=3.0 ~ 5.25V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	–0.005dB	PB	0		21.5	kHz
	–0.02dB		-	21.768	-	kHz
	–0.06dB		-	22.0	-	kHz
	–6.0dB		-	24.0	-	kHz
Stopband (Note 8)		SB	26.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 9)		GD		27.6		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR		1.0		Hz
	–0.5dB			2.9		Hz
	–0.1dB			6.5		Hz

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD, DVDD=4.75 ~ 5.25V; TVDD=3.0 ~ 5.25V; fs=96kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	–0.005dB	PB	0		43.0	kHz
	–0.02dB		-	43.536	-	kHz
	–0.06dB		-	44.0	-	kHz
	–6.0dB		-	48.0	-	kHz
Stopband (Note 8)		SB	53.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 9)		GD		27.6		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR		2.0		Hz
	–0.5dB			5.8		Hz
	–0.1dB			13.0		Hz

Note 8. The passband and stopband frequencies scale with fs.

Note 9. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.75 ~ 5.25V; TVDD=3.0 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (TVDD=3.0 ~ 3.6V)	VIH	2.2	-	-	V
Low-Level Input Voltage (TVDD=3.0 ~ 3.6V)	VIL	-	-	0.8	V
High-Level Input Voltage (TVDD=3.6 ~ 5.25V)	VIH	2.7	-	-	V
Low-Level Input Voltage (TVDD=3.6 ~ 5.25V)	VIL	-	-	0.5	V
High-Level Output Voltage (Iout=−100μA)	VOH	TVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=100μA)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.75 ~ 5.25V; TVDD=3.0 ~ 5.25V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Master Clock 256fs:	fCLK	2.048	12.288	24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
384fs:	fCLK	3.072	18.432	36.864	MHz
Pulse Width Low	tCLKL	11			ns
Pulse Width High	tCLKH	11			ns
512fs:	fCLK	4.096	24.576	24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
768fs:	fCLK	6.144	36.864	36.864	MHz
Pulse Width Low	tCLKL	11			ns
Pulse Width High	tCLKH	11			ns
LRCK Timing (Slave Mode)					
Normal mode (TDM1="L", TDM0="L")					
LRCK Frequency	fs	8		96	kHz
Duty Cycle	Duty	45		55	%
TDM256 MODE (TDM1="L", TDM0="H")					
LRCK Frequency	fs	8		48	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 MODE (TDM1="H", TDM0="H")					
LRCK Frequency	fs	8		96	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
LRCK Timing (Master Mode)					
Normal mode (TDM1="L", TDM0="L")					
LRCK Frequency	fs	8		96	kHz
Duty Cycle	Duty		50		%
TDM256 MODE (TDM1="L", TDM0="H")					
LRCK Frequency	fs	8		48	kHz
"H" time (Note 10)	tLRH		1/8fs		ns
TDM128 MODE (TDM1="H", TDM0="H")					
LRCK Frequency	fs	8		96	kHz
"H" time (Note 10)	tLRH		1/4fs		ns

Note 10. "L" time at I^2S format.

Parameter		Symbol	min	typ	max	Units
Audio Interface Timing (Slave mode)						
Normal mode (TDM1="L", TDM0="L")						
BICK Period		tBCK	160			ns
BICK Pulse Width Low		tBCKL	65			ns
Pulse Width High		tBCKH	65			ns
LRCK Edge to BICK "↑"	(Note 11)	tLRB	30			ns
BICK "↑" to LRCK Edge	(Note 11)	tBLR	30			ns
LRCK to SDTO1/2 (MSB) (Except I^2S mode)		tLRS			35	ns
BICK "↓" to SDTO1/2		tBSD			35	ns
TDM256 mode (TDM1="L", TDM0="H")						
BICK Period		tBCK	81			ns
BICK Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
LRCK Edge to BICK "↑"	(Note 11)	tLRB	20			ns
BICK "↑" to LRCK Edge	(Note 11)	tBLR	20			ns
BICK "↓" to SDTO1/2		tBSD			20	ns
TDM128 mode (TDM1="H", TDM0="H")						
BICK Period		tBCK	81			ns
BICK Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
LRCK Edge to BICK "↑"	(Note 11)	tLRB	20			ns
BICK "↑" to LRCK Edge	(Note 11)	tBLR	20			ns
BICK "↓" to SDTO1	(Note 12)	tBSD			20	ns
Audio Interface Timing (Master mode)						
Normal mode (TDM1="L", TDM0="L")						
BICK Frequency		fBCK		64fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	−20		20	ns
BICK "↓" to SDTO1/2		tBSD	−40		40	ns
TDM256 mode (TDM1="L", TDM0="H")						
BICK Frequency		fBCK		256fs		Hz
BICK Duty	(Note 13)	dBCK		50		%
BICK "↓" to LRCK		tMBLR	−12		12	ns
BICK "↓" to SDTO1/2		tBSD	−20		20	ns
TDM128 mode (TDM1="H", TDM0="H")						
BICK Frequency		fBCK		128fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	−12		12	ns
BICK "↓" to SDTO1	(Note 12)	tBSD	−20		20	ns
Power-Down & Reset Timing						
PDN Pulse Width	(Note 14)	tPD	150			ns
PDN "↑" to SDTO1/2 valid	(Note 15)	tPDV		516		1/fs

Note 11. BICK rising edge must not occur at the same time as LRCK edge.

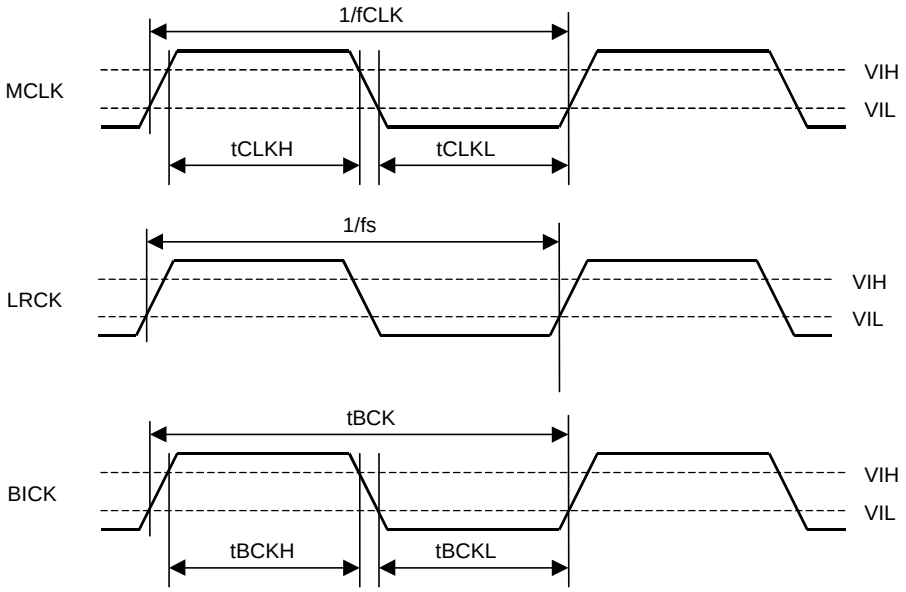
Note 12. SDTO2 output is fixed to "L".

Note 13. This value is MCLK=512fs. Duty cycle is not guaranteed when MCLK=256fs/384fs.

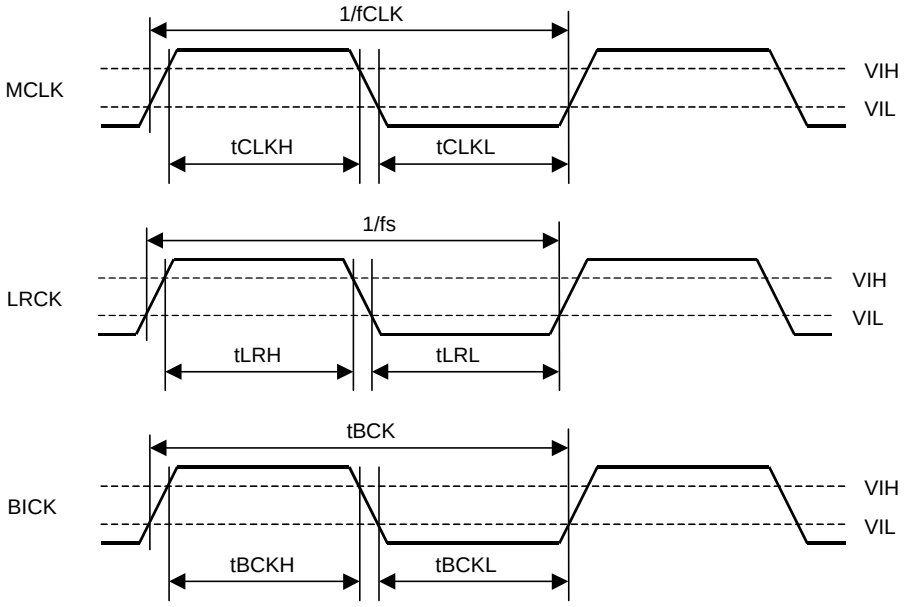
Note 14. The AK5384 can be reset by bringing the PDN pin = "L".

Note 15. This cycle is the number of LRCK rising edges from the PDN pin = "H".

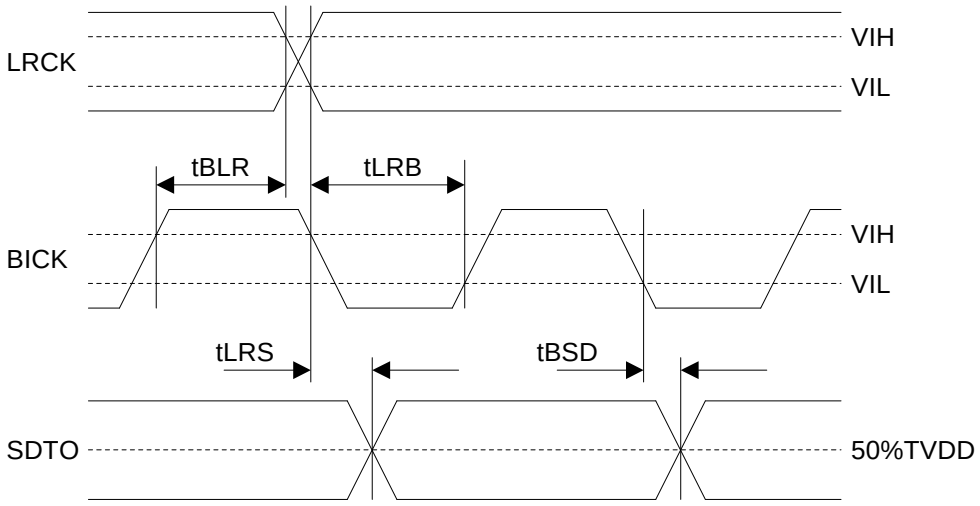
■ Timing Diagram



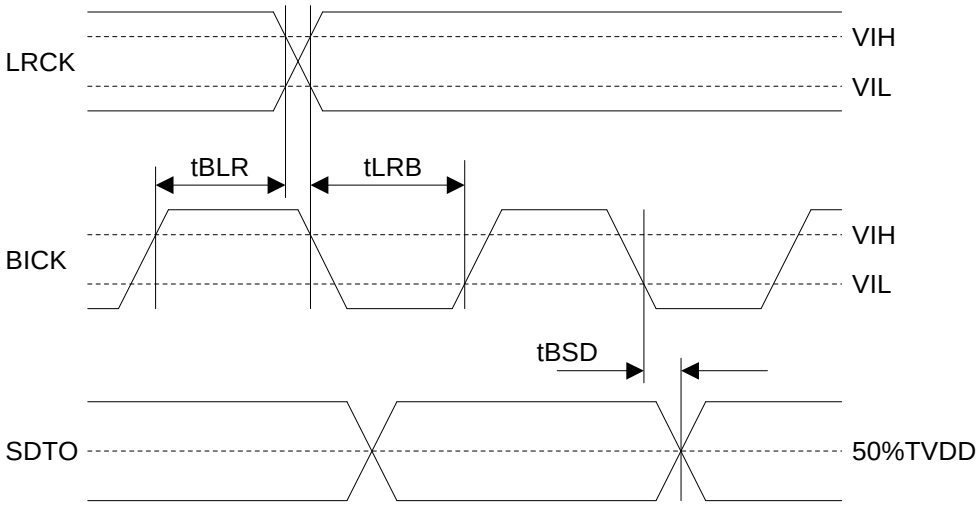
Clock Timing (TDM0 pin = “L”)



Clock Timing (TDM0 pin = “H”)

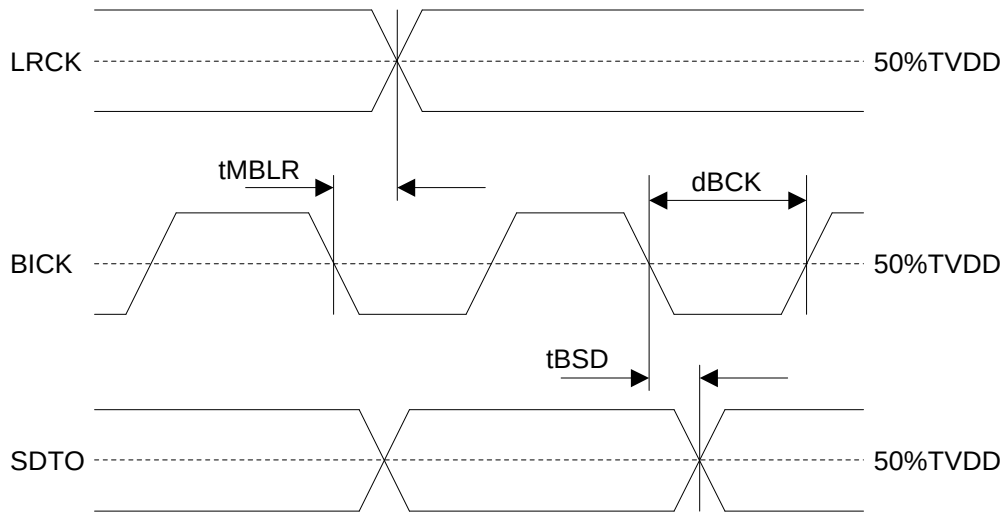


Audio Interface Timing (Slave mode, TDM0 pin = "L")

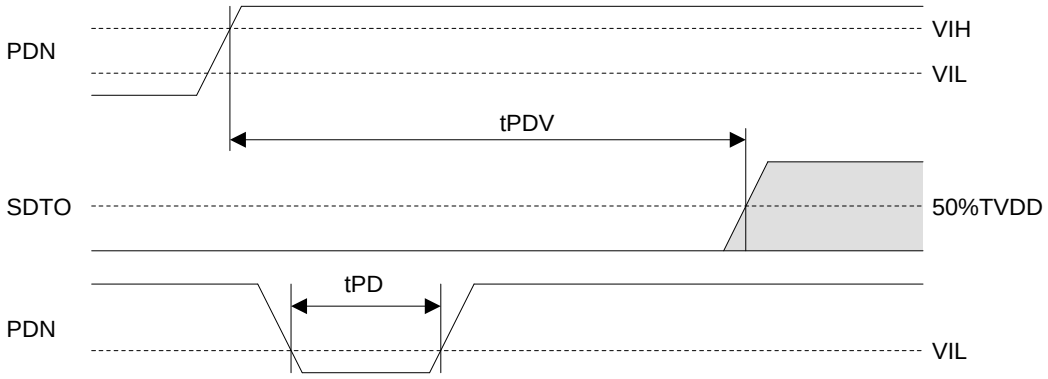


Audio Interface Timing (Slave mode, TDM0 pin = "H")

Note: SDTO shows SDTO1 and SDTO2.



Audio Interface Timing (Master mode)



Power Down & Reset Timing

Note: SDTO shows SDTO1 and SDTO2.

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK5384 are MCLK(256fs/384fs/512fs/768fs), BICK(48fs~), LRCK(1fs) in slave mode (M/S pin = "L"). MCLK should be synchronized with LRCK but the phase is not critical. When 384fs, 512fs or 768fs clock is input to MCLK pin, the internal master clock becomes 256fs(=384fs x 2/3=512fs x 1/2=768fs x 1/3) automatically. Table 1 illustrates standard audio word rates and corresponding frequencies used in the AK5384.

In master mode (M/S pin = "H"), MCLK select 256fs or 512fs by CKS pin. But 384fs and 768fs are not supported. 512fs does not support 96kHz sampling.

All external clocks (MCLK, BICK, LRCK) should always be present whenever the AK5384 is in normal operation mode (PDN pin = "H"). If these clocks are not provided, the AK5384 may draw excess current and may fall into unpredictable operation. This is because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK5384 should be in the power-down mode (PDN pin = "L"). After exiting reset at power-up etc., the AK5384 is in the power-down mode until MCLK and LRCK are input. In master mode, the master clock (MCLK) must be provided unless PDN pin = "L".

fs	MCLK				BICK	
	256fs	384fs	512fs	768fs	64fs	128fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.576MHz	2.0480MHz	4.0960MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz	5.6448MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz	6.1440MHz
96.0kHz	24.5760MHz	36.8640MHz	N/A	N/A	6.1440MHz	N/A

Table 1. System clock example (Slave mode)

CKS	MCLK	
	8kHz ≤ fs ≤ 48kHz	48kHz < fs ≤ 96kHz
L	256fs	256fs
H	512fs	N/A

Table 2. Master clock frequency select (Master mode)

■ Audio Interface Format

12 types of audio data interface can be selected by the TDM1-0, M/S and DIF pins as shown in Table 3. The audio data format can be selected by the DIF pin. In all formats the serial data is MSB-first, 2's compliment format. The SDTO1/2 is clocked out on the falling edge of BICK.

In normal mode, Mode 0-1 are the slave mode, and BICK is available up to 128fs at fs=48kHz. BICK outputs 64fs clock in Mode 2-3.

In TDM256 mode, the serial data of all ADC (four channels) is output from the SDTO1/2 pins. BICK should be fixed to 256fs. In the slave mode, "H" time and "L" time of LRCK should be 1/256fs at least. In the master mode, "H" time ("L" time at I^2S mode) of LRCK is 1/8fs typically. TDM256 mode does not support 96kHz sampling.

In TDM128 mode, the serial data of all ADC (four channels) is output from the SDTO1 pin. The SDTO2 output is fixed to "L". BICK should be fixed to 128fs. In the slave mode, "H" time and "L" time of LRCK should be 1/128fs at least. In the master mode, "H" time ("L" time at I^2S mode) of LRCK is 1/4fs typically. TDM128 mode supports up to 96kHz sampling.

Mode		TDM1	TDM0	M/S	DIF	SDTO	LRCK		BICK	
								I/O		I/O
0	Normal	L	L	L	L	24bit, MSB justified	H/L	I	48-128fs	I
1					H	24bit, I^{2}S Compatible	L/H	I	48-128fs	I
2				H	L	24bit, MSB justified	H/L	O	64fs	O
3					H	24bit, I^{2}S Compatible	L/H	O	64fs	O
4	TDM256	L	H	L	L	24bit, MSB justified	↑	I	256fs	I
5					H	24bit, I^{2}S Compatible	↓	I	256fs	I
6				H	L	24bit, MSB justified	↑	O	256fs	O
7					H	24bit, I^{2}S Compatible	↓	O	256fs	O
8	TDM128	H	H	L	L	24bit, MSB justified	↑	I	128fs	I
9					H	24bit, I^{2}S Compatible	↓	I	128fs	I
10				H	L	24bit, MSB justified	↑	O	128fs	O
11					H	24bit, I^{2}S Compatible	↓	O	128fs	O
12	N/A	H	L	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 3. Audio Interface Formats

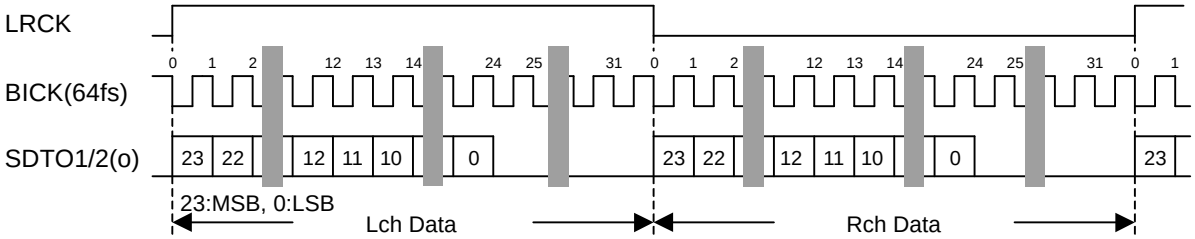


Figure 1. Mode 0, 2 Timing (Normal mode, MSB justified)

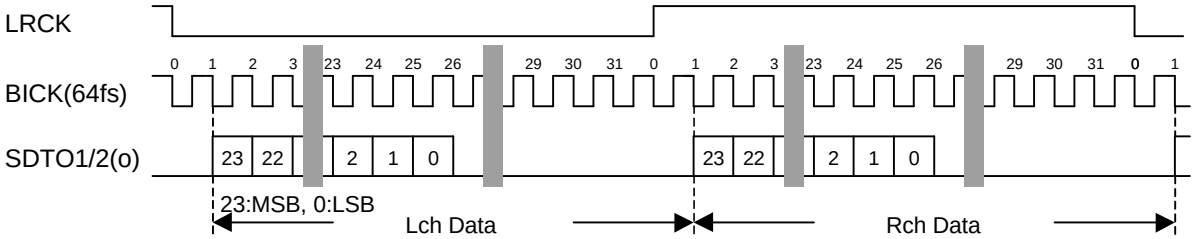


Figure 2. Mode 1, 3 Timing (Normal mode, I^{2}S Compatible)

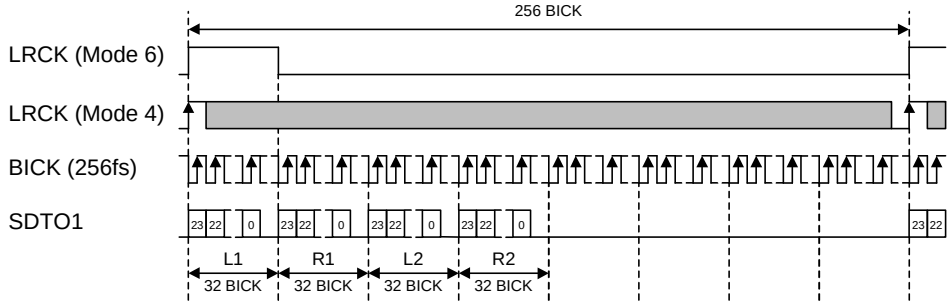


Figure 3. Mode 4, 6 Timing (TDM256 mode, MSB justified)

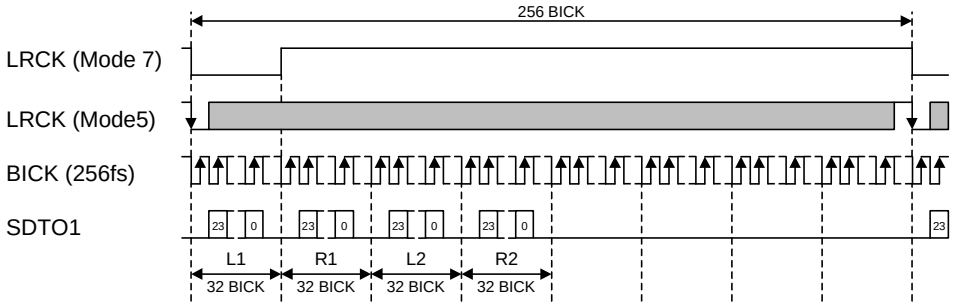


Figure 4. Mode 5, 7 Timing (TDM256 mode, I^{2}S Compatible)

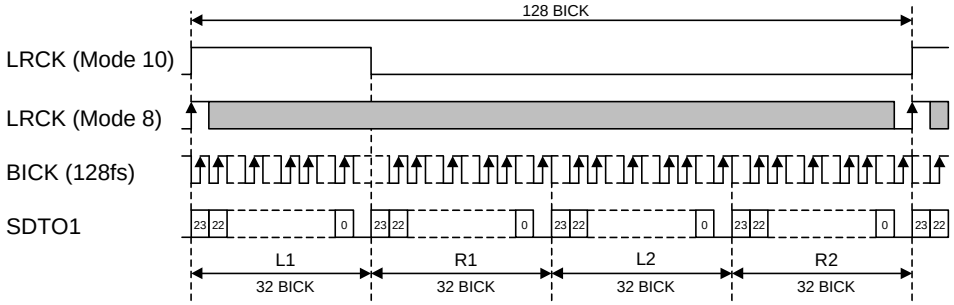


Figure 5. Mode 8, 10 Timing (TDM128 mode, MSB justified)

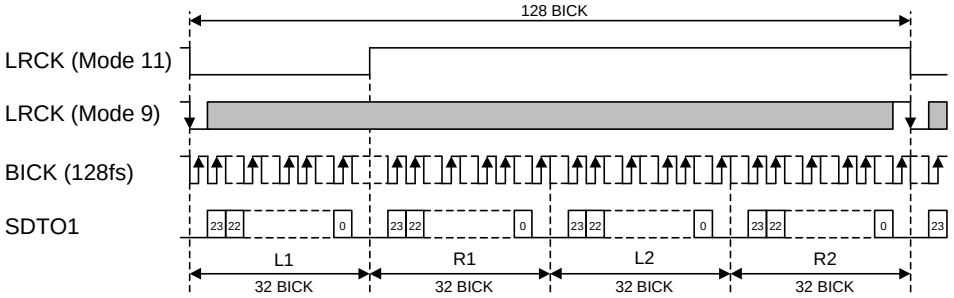


Figure 6. Mode 9, 11 Timing (TDM128 mode, I^{2}S Compatible)

■ Master Mode and Slave Mode

The M/S pin selects either master or slave mode. M/S pin = "H" selects master mode and "L" selects slave mode. The AK5384 outputs BICK and LRCK in master mode. In slave mode, MCLK, BICK and LRCK are input externally.

M/S pin	Mode	BICK, LRCK
L	Slave Mode	BICK = Input LRCK = Input
H	Master Mode	BICK = Output LRCK = Output

Table 4. Master mode/Slave mode

■ Digital High Pass Filter

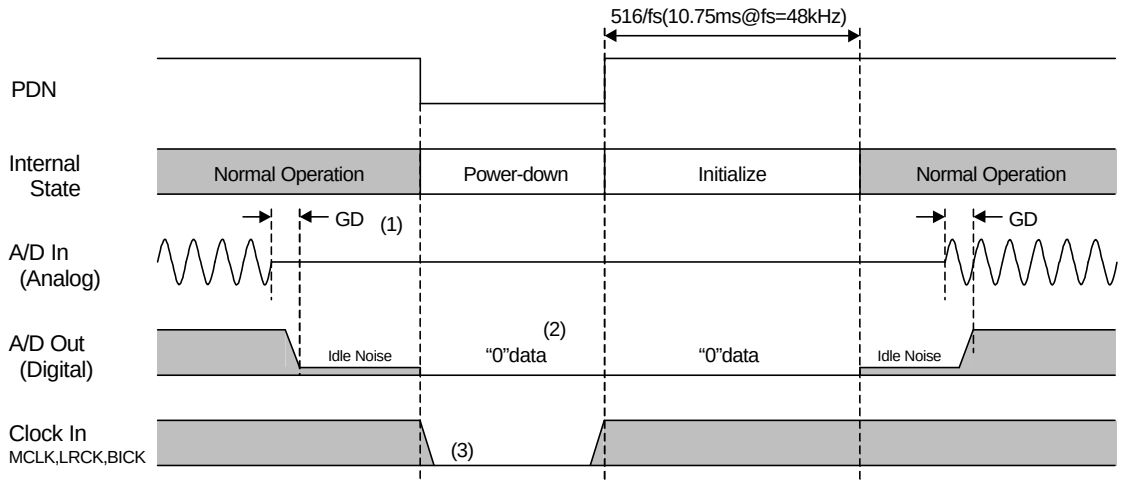
The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz(@fs=48kHz) and scales with sampling rate (fs).

■ Overflow Detection

The AK5384 has overflow detect function for analog input. OVF pin goes to "H" if one of 4-channels overflows (more than −0.3dBFS). OVF output for overflowed analog input has the same group delay as ADC (GD=27.6/fs=575μs@fs=48kHz). OVF is "L" for 516/fs (=10.75ms@fs=48kHz) after PDN pin = "↑", and then overflow detection is enabled.

■ Power down

The AK5384 is placed in the power-down mode by bringing PDN pin "L" and the digital filter is also reset at the same time. This reset should always be done after power-up. In the power-down mode, the VCOM are AVSS level. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO1/2 becomes available after 516 cycles of LRCK clock. During initialization, the ADC digital data outputs of both channels are forced to a 2's complement "0". The ADC outputs settle in the data corresponding to the input signals after the end of initialization (Settling approximately takes the group delay time).



Notes:
(1) Digital output corresponding to analog input has the group delay (GD).
(2) ADC output is "0" data at the power-down state.
(3) When the external clocks (MCLK, BICK, LRCK) are stopped, the AK5384 should be in the power-down state.

Figure 7. Power-down/up sequence example

■ System Reset

The AK5384 should be reset once by bringing PDN pin "L" after power-up. The internal timing starts clocking by the rising edge (falling edge at I^2S mode) of LRCK upon exiting from reset.

■ Cascade TDM Mode

The AK5384 supports cascading of up to two devices in a daisy chain configuration at TDM256 mode. In this mode, SDTO2 pin of device #1 is connected to TDMIN pin of device #2. SDTO1 pin of device #2 can output 8ch TDM data multiplexed with 4ch TDM data of device #1 and 4ch TDM data of device #2. Figure 8 shows a connection example of a daisy chain.

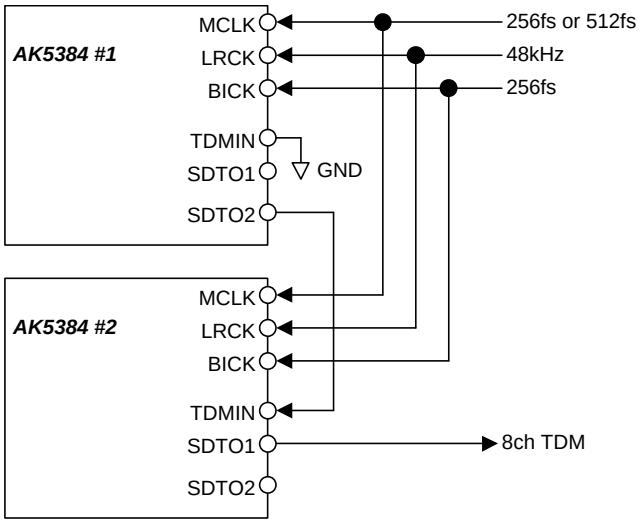


Figure 8. Cascade TDM Connection Diagram

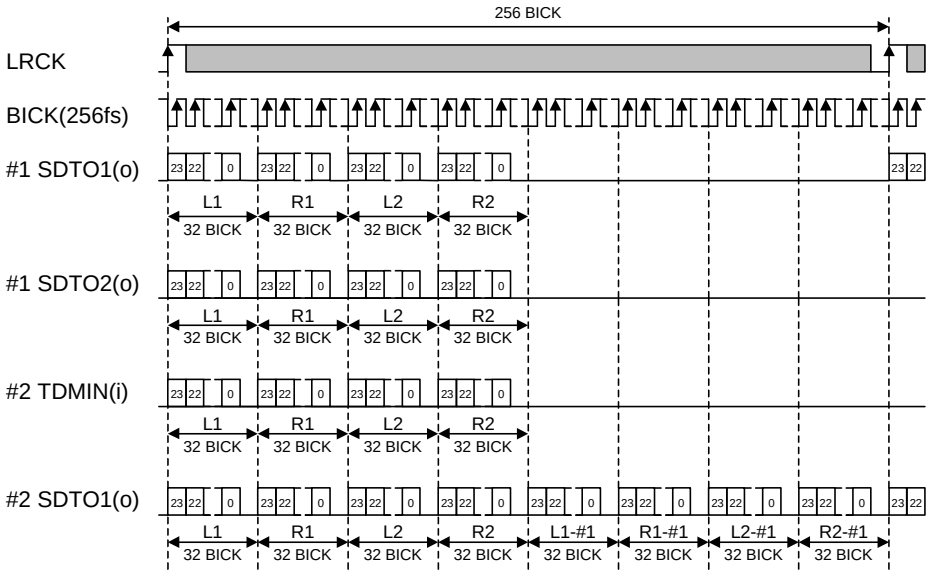
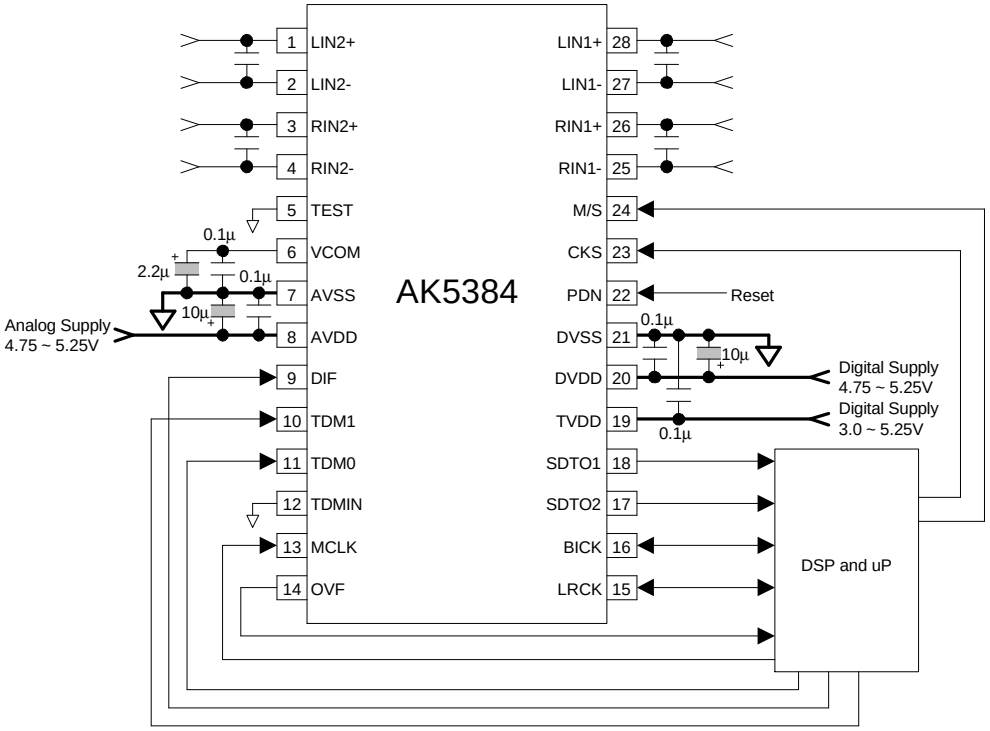


Figure 9. Cascade TDM Timing

SYSTEM DESIGN

Figure 10 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Note:

- AVSS and DVSS of the AK5384 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins should not be left floating.

Figure 10. Typical Connection Diagram (Normal mode)

1. Grounding and Power Supply Decoupling

The AK5384 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from the analog supply in the system. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK5384 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5384 as possible, with the small value ceramic capacitor being the closest.

2. Voltage Reference Inputs

The differential voltage between AVDD and AVSS sets the analog input range. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2μF parallel with a 0.1μF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5384.

3. Analog Inputs

The AK5384 accepts +5V supply voltage. Any voltage which exceeds the upper limit of AVDD+0.3V and lower limit of AVSS–0.3V and any current beyond 10mA for the analog input pins (LIN+/–, RIN+/–) should be avoided. Excessive currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution specially in case of using ±15V in other analog circuits.

The analog inputs are differential and internally biased to the common voltage (AVDD/2) with 26kΩ(typ). The input signal range between LIN(RIN)+ and LIN(RIN)– scales with the supply voltage and nominally ±0.58 x AVDD. The AK5384 can accept input voltages from AVSS to AVDD. The ADC output data format 2's compliment. The internal HPF removes the DC offset.

The AK5384 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs.

4. External Analog Inputs Circuit

Figure 11 shows an input buffer circuit example 1. The input level of this circuit is 5.7Vpp (AK5384: typ. ±2.9Vpp).

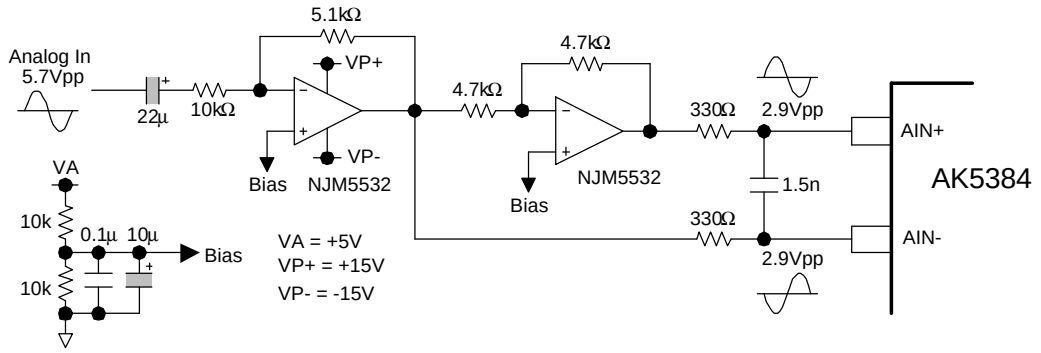


Figure 11. Input buffer circuit example 1 (DC coupled single-end input)

Figure 12 shows an input buffer circuit example 2. The input level of this circuit is 5.7Vpp (AK5384: typ. ±2.9Vpp).

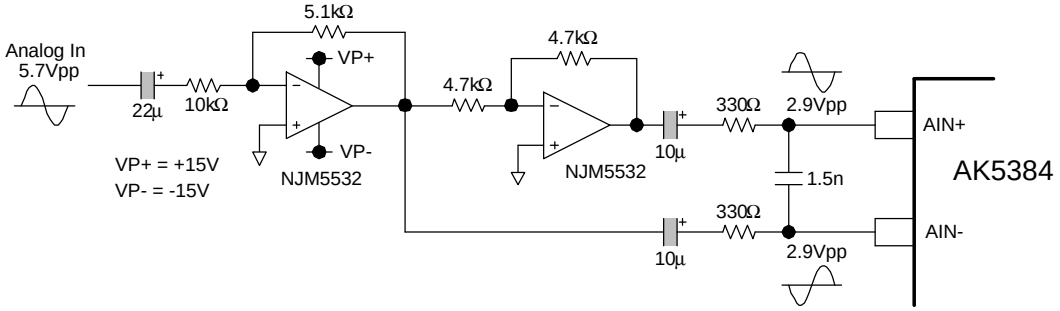


Figure 12. Input buffer circuit example 2 (AC coupled single-end input)

Figure 13 shows an input buffer circuit example 3. The input level of this circuit is 2.9Vpp (AK5384: typ. 2.9Vpp).

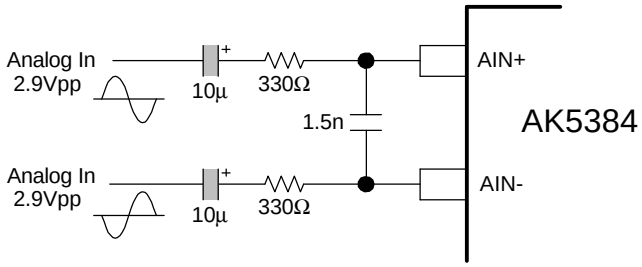
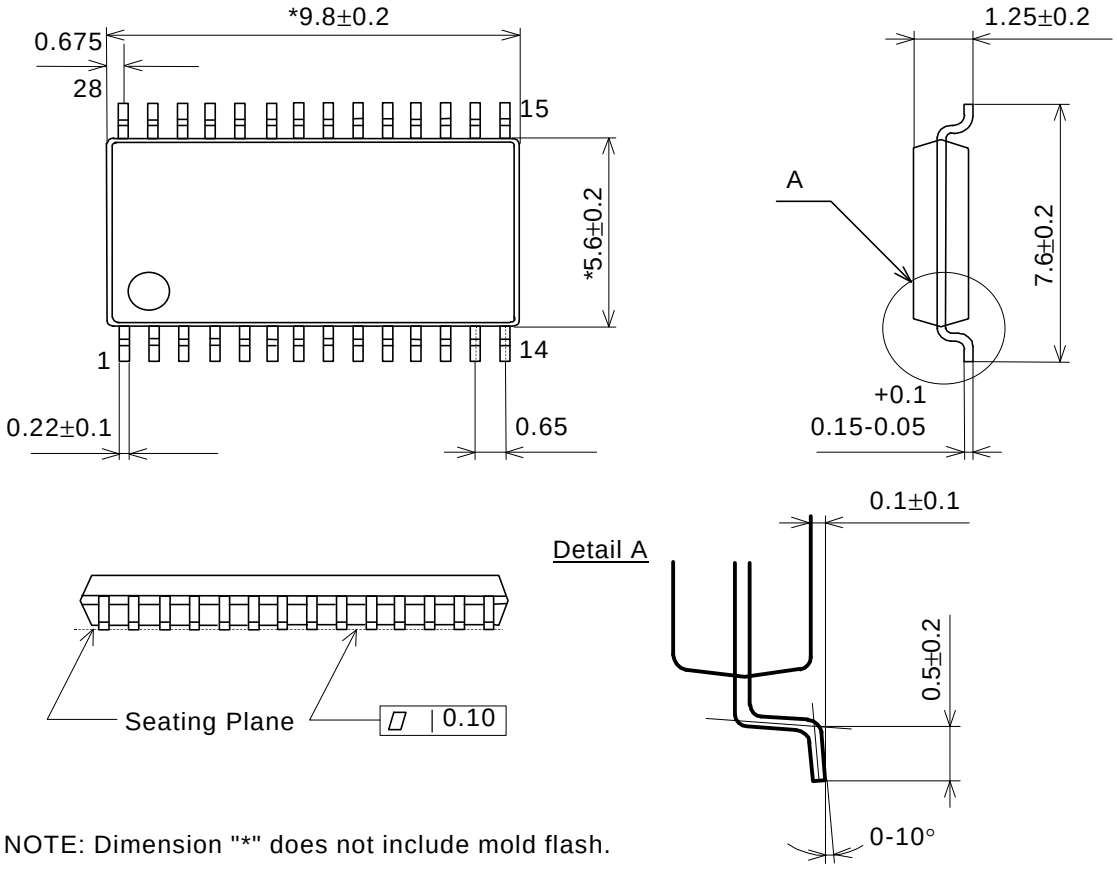


Figure 13. Input buffer circuit example 3 (Differential input)

PACKAGE

28pin VSOP (Unit: mm)

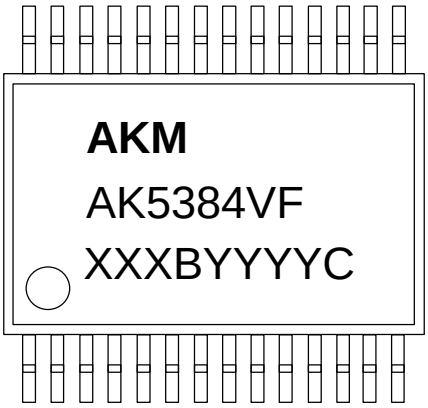


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXBYYYYC Date code identifier

XXXB :Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C : Alpha character)

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