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AK5386

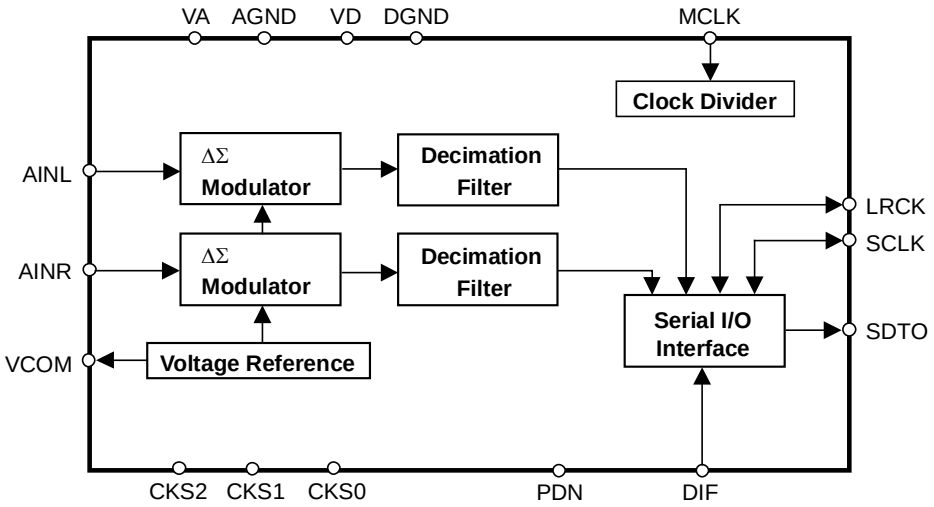
Single-ended 24-Bit 192kHz ΔΣ ADC

GENERAL DESCRIPTION

The AK5386 is a stereo A/D Converter with wide sampling rate of 8kHz ~ 216kHz and is suitable for consumer to professional audio system. The AK5386 achieves high accuracy and low cost by using Enhanced dual bit ΔΣ techniques. The AK5386 requires no external components because the analog inputs are single-ended. The audio interface has two formats (MSB justified, I^2S) and can correspond to various systems like DVD Recorder, AV Receiver, PC Sound card and Music Instrument recording.

FEATURES

- ☐ **Single-ended Input**
- ☐ **Digital HPF for DC-Offset cancel**
- ☐ **S/(N+D): 96dB**
- ☐ **DR: 110dB**
- ☐ **S/N: 110dB**
- ☐ **Linear Phase Digital Anti-Alias Filtering**
  - **Passband: 0 ~ 21.768kHz (@ fs=48kHz)**
  - **Passband Ripple: ±0.005dB**
  - **Stopband Attenuation: 80dB**
- ☐ **Master Clock: 512fs/768fs (Normal Speed)**
  256fs/384fs (Double Speed)
  128fs/192fs (Quad Speed)
- ☐ **Sampling Frequency:**
  - **Normal Speed: 8kHz ~ 54kHz (512fs)**
    8kHz ~ 48kHz (768fs)
  - **Double Speed: 54kHz ~ 108kHz (256fs)**
    48kHz ~ 96kHz (384fs)
  - **Quad Speed: 108kHz ~ 216kHz (128fs)**
    96kHz ~ 192kHz (192fs)
- ☐ **Master / Slave Mode**
- ☐ **Audio Interface: 24bit MSB justified / I^2S selectable**
- ☐ **Input level: CMOS**
- ☐ **Power Supply:**
  - **Analog: 4.5 ~ 5.5V**
  - **Digital: 2.7 ~ 3.6V (Normal Speed)**
    3.0 ~ 3.6V (Double Speed, Quad Speed)
- ☐ **Ta = –40 ~ 85°C**
- ☐ **Small 16pin TSSOP Package**
- ☐ **AK5357/58/59/81 Pin-compatible**



Block Diagram

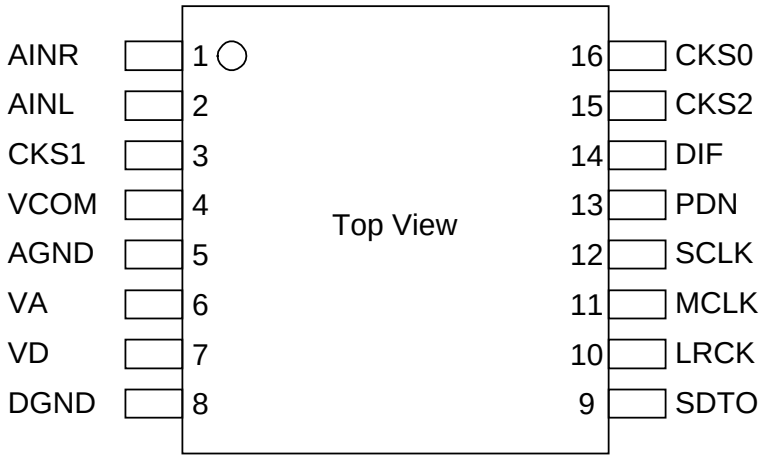
■ Compatibility with AK5357, AK5358, AK5359, AK5381 and AK5386

	AK5357	AK5358	AK5381	AK5359	AK5386
fs	4kHz to 96kHz	8kHz to 96kHz	4kHz to 96kHz	8kHz to 216kHz	8kHz to 216kHz
S/(N+D)	88dB	92dB	96dB	94dB	96dB
DR	102dB	102dB	106dB	102dB	110dB
MCLK @ 48kHz	256/512/384/768fs	256/512/384/768fs	256/512/384/768fs	256/512/384/768fs	512/768fs
VIH @ TTL Level Mode	2.2V	2.2V	2.4V	Not Available	Not Available
VA(Analog Supply)	2.7 to 5.5V	4.5 to 5.5V	4.5 to 5.5V	4.5 to 5.5V	4.5 to 5.5V
VD (Digital Supply)	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V 3.0 to 5.5V@ fs=96kHz	2.7 to 5.5V	2.7 to 3.6V 3.0 to 3.6V @ fs=96k, 192kHz
HPF Disable	Available	Not Available	Available	Available	Available
Operating Temperature	ET: –20~+85°C VT: –40~+85°C	ET: –20~+85°C	ET: –20~+85°C VT: –40~+85°C XT: –40~+85°C	ET: –20~+85°C VT: –40~+85°C	VT: –40~+85°C

■ Ordering Guide

AK5386VT	–40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD5386	Evaluation Board for AK5386	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1	AINR	I	Rch Analog Input Pin
2	AINL	I	Lch Analog Input Pin
3	CKS1	I	Mode Select 1 Pin
4	VCOM	O	Common Voltage Output Pin, VA/2 Bias voltage of ADC input.
5	AGND	-	Analog Ground Pin
6	VA	-	Analog Power Supply Pin, 5V
7	VD	-	Digital Power Supply Pin, 3.3V
8	DGND	-	Digital Ground Pin
9	SDTO	O	Audio Serial Data Output Pin "L" Output at Power-down mode.
10	LRCK	I/O	Output Channel Clock Pin "L" Output in Master Mode at Power-down mode.
11	MCLK	I	Master Clock Input Pin
12	SCLK	I/O	Audio Serial Data Clock Pin "L" Output in Master Mode at Power-down mode.
13	PDN	I	Power Down & Reset Mode Pin "H": Power up, "L": Power down & Reset The AK5386 must be reset once upon power-up.
14	DIF	I	Audio Interface Format Pin "H": 24bit I^2S Compatible, "L": 24bit MSB justified
15	CKS2	I	Mode Select 2 Pin
16	CKS0	I	Mode Select 0 Pin

Note: Do not allow all digital input pins except for analog input pins (AINL and AINR pins) to float.

■ Handling of Unused Pin

The unused input pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	AINL	This pin should be open.
	AINR	This pin should be open.

ABSOLUTE MAXIMUM RATINGS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	VA	–0.3	6.0	V
(Note 2)	Digital	VD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (AINL, AINR, CKS1 pins)		VINA	–0.3	VA+0.3	V
Digital Input Voltage (Note 3)		VIND	–0.3	VD+0.3	V
Ambient Temperature (powered applied)		Ta	-40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AGND and DGND must be connected to the same analog ground plane.
Note 3. DIF, PDN, SCLK, MCLK, LRCK, CKS0 and CKS2 pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	VA	4.5	5.0	5.5	V
(Note 4)	Digital: Normal Speed	VD	2.7	3.3	3.6	V
	Double/Quad Speed	VD	3.0	3.3	3.6	V

Note 4. The power up sequence between VA and VD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=5.0V, VD=3.3V; AGND=DGND=0V; fs=48kHz, 96kHz, 192kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz, 40Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics:						
Resolution					24	Bits
Input Voltage		(Note 5)	2.7	3.0	3.3	Vpp
S/(N+D)	fs=48kHz	–1dBFS	86	96	-	dB
	BW=20kHz	–60dBFS	-	47	-	dB
	fs=96kHz	–1dBFS	86	92	-	dB
	BW=40kHz	–60dBFS	-	42	-	dB
	fs=192kHz	–1dBFS	-	90	-	dB
	BW=40kHz	–60dBFS	-	42	-	dB
DR (–60dBFS with A-weighted)			102	110	-	dB
S/N (A-weighted)			102	110	-	dB
Input Resistance			4	6	-	kΩ
Interchannel Isolation			95	115	-	dB
Interchannel Gain Mismatch			-	0.1	0.5	dB
Gain Drift			-	100	-	ppm/°C
Power Supply Rejection		(Note 6)	-	50	-	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")						
VA			-	20	30	mA
VD	(fs=48kHz)		-	7	11	mA
VD	(fs=96kHz)		-	10	15	mA
VD	(fs=192kHz)		-	10	15	mA
Power down mode (PDN pin = "L")		(Note 7)				
VA+VD			-	10	100	μA

Note 5. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage.
Vin = 0.6 x VA (Vpp).
Note 6. PSR is applied to VA and VD with 1kHz, 50mVpp.
Note 7. All digital input pins are held VD or DGND.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=–40 ~ 85°C; VA=4.5 ~ 5.5V; VD=2.7 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	±0.02dB	PB	0	-	21.768	kHz
	–0.1dB		-	221.	-	kHz
	–0.2dB		-	22.3	-	kHz
	–3.0dB		-	23.5	-	kHz
Stopband		SB	26.5	-	-	kHz
Passband Ripple		PR	-	-	±0.005	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 9)		GD	-	29.4	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR	-	1.0	-	Hz
	–0.1dB		-	6.5	-	Hz

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=–40 ~ 85°C; VA=4.5 ~ 5.5V; VD=3.0 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	±0.02dB	PB	0	-	43.536	kHz
	–0.1dB		-	44.3	-	kHz
	–0.2dB		-	44.6	-	kHz
	–3.0dB		-	47.0	-	kHz
Stopband		SB	53.0	-	-	kHz
Passband Ripple		PR	-	-	±0.005	dB
Stopband Attenuation		SA	80	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 9)		GD	-	29.4	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR	-	2.0	-	Hz
	–0.1dB		-	13.0	-	Hz

FILTER CHARACTERISTICS (fs=192kHz)

(Ta=–40 ~ 85°C; VA=4.5 ~ 5.5V; VD=3.0 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	±0.1dB	PB	0	-	43.8	kHz
	–0.2dB		-	52.9	-	kHz
	–3.0dB		-	90.1	-	kHz
Stopband		SB	112	-	-	kHz
Passband Ripple		PR	-	-	±0.005	dB
Stopband Attenuation		SA	72	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 9)		GD	-	16.5	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3dB	FR	-	4.0	-	Hz
	–0.1dB		-	26.0	-	Hz

Note 8. The passband and stopband frequencies scale with fs. For example, PB (±0.02dB) at fs=48kHz is 0.4535 × fs. The reference frequency of these response is 1kHz.

Note 9. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DC CHARACTERISTICS

(Ta=–40 ~ 85°C; VA=4.5 ~ 5.5V; VD=2.7 ~ 3.6V at Normal Speed, VD=3.0 ~ 3.6V at Double/Quad Speed)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%VD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%VD	V
High-Level Output Voltage	(Iout=–1mA)	VOH	VD–0.5	-	-	V
Low-Level Output Voltage	(Iout=1mA)	VOL	-	-	0.5	V
Input Leakage Current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS (Normal Speed)

(Ta=–40 ~ 85°C; VA=4. 5 ~ 5.5V; VD=2.7 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency: 512fs		fCLK	4.096	-	27.648	MHz
768fs		fCLK	6.144	-	36.864	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK						
Frequency: 512fs		fs	8	-	54	kHz
768fs		fs	8	-	48	kHz
Duty Cycle	Slave mode		45	-	55	%
	Master mode		-	50	-	%
Audio Interface Timing						
Slave mode						
SCLK Period		tSCK	1/128fs	-	-	ns
SCLK Pulse Width Low		tSCKL	60	-	-	ns
Pulse Width High		tSCKH	60	-	-	ns
LRCK Edge to SCLK "↑"	(Note 10)	tLRSH	20	-	-	ns
SCLK "↑" to LRCK Edge	(Note 10)	tSHLR	20	-	-	ns
LRCK to SDTO (MSB) (Except I^2S mode)		tLRS	-	-	40	ns
SCLK "↓" to SDTO		tSSD	-	-	40	ns
Master mode						
SCLK Frequency		fSCK	-	64fs	-	Hz
SCLK Duty		dSCK	-	50	-	%
SCLK "↓" to LRCK		tMSLR	–20	-	40	ns
SCLK "↓" to SDTO		tSSD	–20	-	40	ns
Reset Timing						
PDN Pulse Width	(Note 11)	tPD	150	-	-	ns
PDN "↑" to SDTO valid at Slave Mode	(Note 12)	tPDV	-	4132	-	1/fs
PDN "↑" to SDTO valid at Master Mode	(Note 12)	tPDV	-	4129	-	1/fs

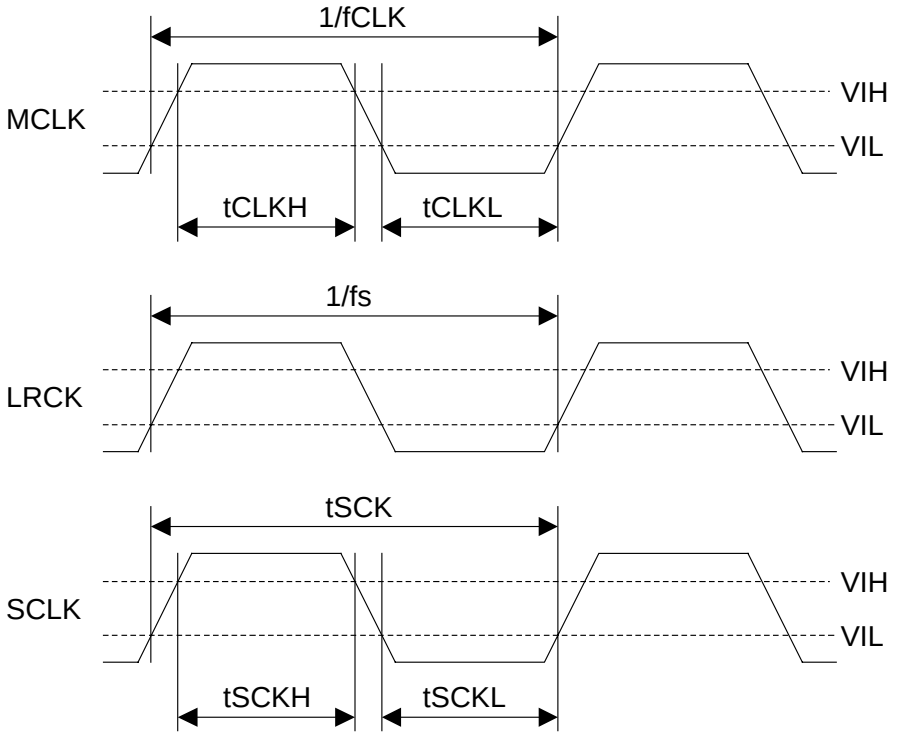
SWITCHING CHARACTERISTICS (Double / Quad Speed)

(Ta=–40 ~ 85°C; VA=4. 5 ~ 5.5V; VD=3.0 ~ 3.6V; C_L=20pF)

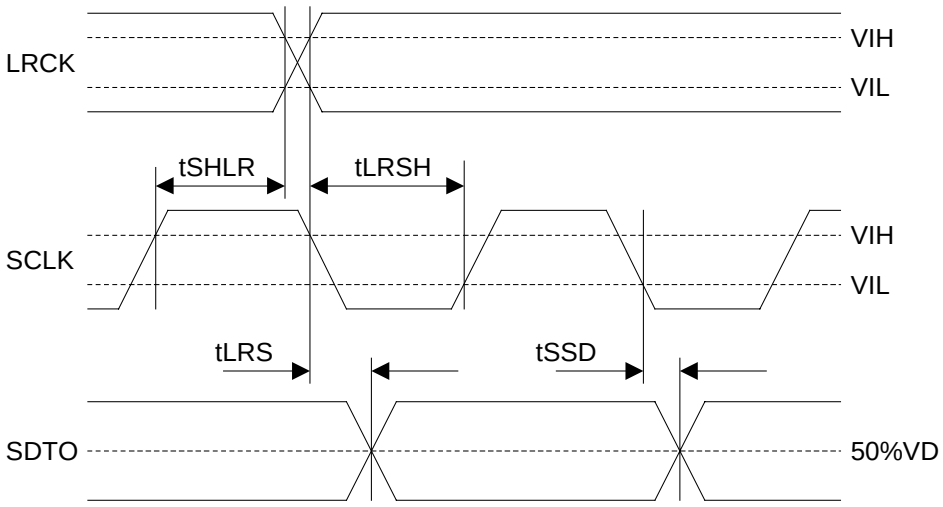
Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
Frequency: 128fs, 256fs			fCLK	13.824	-	27.648	MHz
192fs, 384fs			fCLK	18.432	-	36.864	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK							
	Frequency:	Double Speed: 256fs	fs	54	-	108	kHz
		384fs	fs	48	-	96	kHz
		Quad Speed: 128fs	fs	108	-	216	kHz
		192fs	fs	96	-	192	kHz
	Duty Cycle	Slave mode		45	-	55	%
		Master mode		-	50	-	%
Audio Interface Timing							
	Slave mode						
	SCLK Period: Double Speed		tSCK	1/128fs	-	-	ns
	Quad Speed		tSCK	1/64fs	-	-	ns
	SCLK Pulse Width Low		tSCKL	33	-	-	ns
	Pulse Width High		tSCKH	33	-	-	ns
	LRCK Edge to SCLK "↑"	(Note 10)	tLRSH	20	-	-	ns
	SCLK "↑" to LRCK Edge	(Note 10)	tSHLR	20	-	-	ns
	LRCK to SDTO (MSB) (Except I^2S mode)		tLRS	-	-	20	ns
	SCLK "↓" to SDTO		tSSD	-	-	20	ns
	Master mode						
	SCLK Frequency		fSCK	-	64fs	-	Hz
	SCLK Duty		dSCK	-	50	-	%
	SCLK "↓" to LRCK		tMSLR	–20	-	20	ns
	SCLK "↓" to SDTO		tSSD	–20	-	20	ns
Reset Timing							
PDN Pulse Width		(Note 11)	tPD	150	-	-	ns
PDN "↑" to SDTO valid at Slave Mode		(Note 12)	tPDV	-	4132	-	1/fs
PDN "↑" to SDTO valid at Master Mode		(Note 12)	tPDV	-	4129	-	1/fs

Note 10. SCLK rising edge must not occur at the same time as LRCK edge.
Note 11. The AK5386 can be reset by bringing the PDN pin = "L"
Note 12. This cycle is the number of LRCK rising edges from the PDN pin = "H".

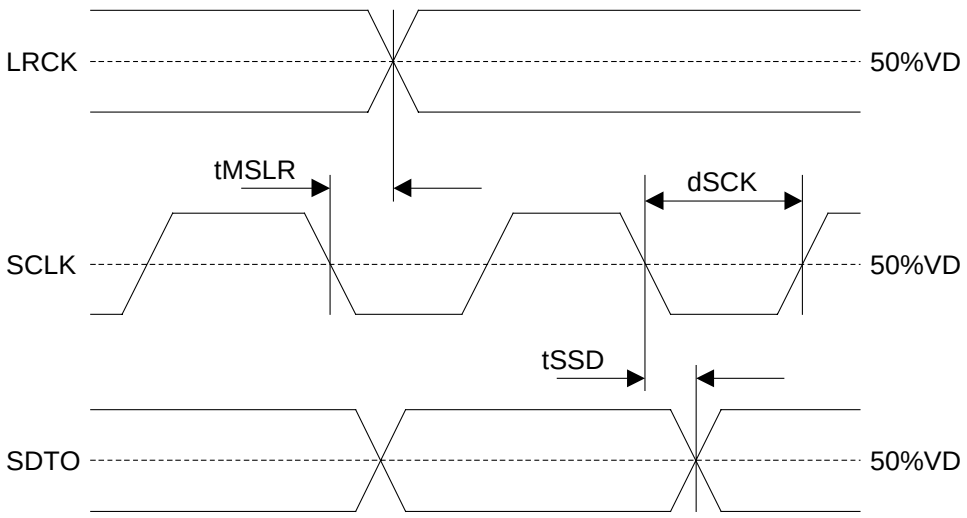
■ **Timing Diagram**



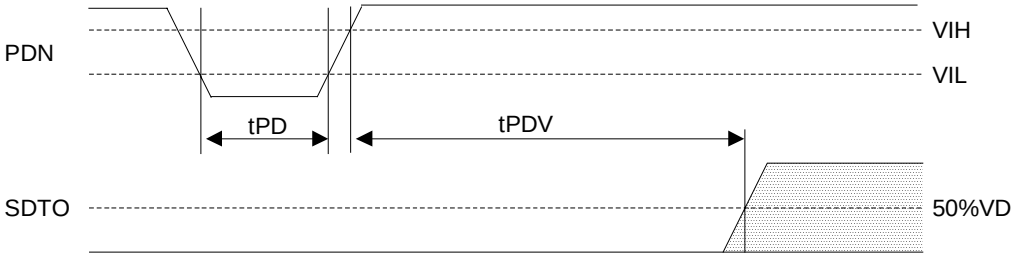
Clock Timing



Audio Interface Timing (Slave mode)



Audio Interface Timing (Master mode)



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

MCLK, SCLK and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. MCLK frequency, SCLK frequency, HPF (ON or OFF) and master/slave are selected by CKS2-0 pins as shown in Table 3. When MCLK is 192fs, 384fs or 768fs, the sampling frequency does not support variable pitch.

All external clocks (MCLK, SCLK and LRCK) must be present unless PDN pin = "L". If these clocks are not provided, the AK5386 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK5386 in power-down mode (PDN pin = "L"). In master mode, the master clock (MCLK) must be provided unless PDN pin = "L".

fs	MCLK					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	N/A	N/A	N/A	N/A	16.384MHz	24.576MHz
44.1kHz	N/A	N/A	N/A	N/A	22.5792MHz	33.8688MHz
48kHz	N/A	N/A	N/A	N/A	24.576MHz	36.864MHz
96kHz	N/A	N/A	24.576MHz	36.864MHz	N/A	N/A
192kHz	24.576MHz	36.864MHz	N/A	N/A	N/A	N/A

Table 1. System Clock Example

Mode	Sampling Frequency	MCLK
Normal Speed	8kHz ≤ fs ≤ 54kHz	512fs
	8kHz ≤ fs ≤ 48kHz	768fs
Double Speed	54kHz < fs ≤ 108kHz	256fs
	48kHz < fs ≤ 96kHz	384fs
Quad Speed	108kHz < fs ≤ 216kHz	128fs
	96kHz < fs ≤ 192kHz	192fs

Table 2. Sampling Frequency Range

CKS2 pin	CKS1 pin	CKS0 pin	HPF	Master/Slave	MCLK	SCLK
L	L	L	ON	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	≥ 48fs or 32fs (Note 13)
L	L	H	OFF	Slave	128/192fs (Quad Speed) 256/384fs (Double Speed) 512/768fs (Normal Speed)	≥ 48fs or 32fs (Note 13)
L	H	L	ON	Master	256fs (Double Speed)	64fs
L	H	H	ON	Master	512fs (Normal Speed)	64fs
H	L	L	ON	Master	128fs (Quad Speed)	64fs
H	L	H	ON	Master	192fs (Quad Speed)	64fs
H	H	L	ON	Master	384fs (Double Speed)	64fs
H	H	H	ON	Master	768fs (Normal Speed)	64fs

Table 3. Mode Select

Note 13. SDTO outputs 16bit data at SCLK=32fs.

■ Audio Interface Format

Two kinds of data formats can be chosen with the DIF pin (Table 4). In both modes, the serial data is in MSB first, 2's complement format. The SDTO is clocked out on the falling edge of SCLK. The audio interface supports both master and slave modes. In master mode, SCLK and LRCK are output with the SCLK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

Mode	DIF pin	SDTO	LRCK	SCLK	Figure
0	L	24bit, MSB justified	H/L	≥ 48fs or 32fs	Figure 1
1	H	24bit, I^2S Compatible	L/H	≥ 48fs or 32fs	Figure 2

Table 4. Audio Interface Format

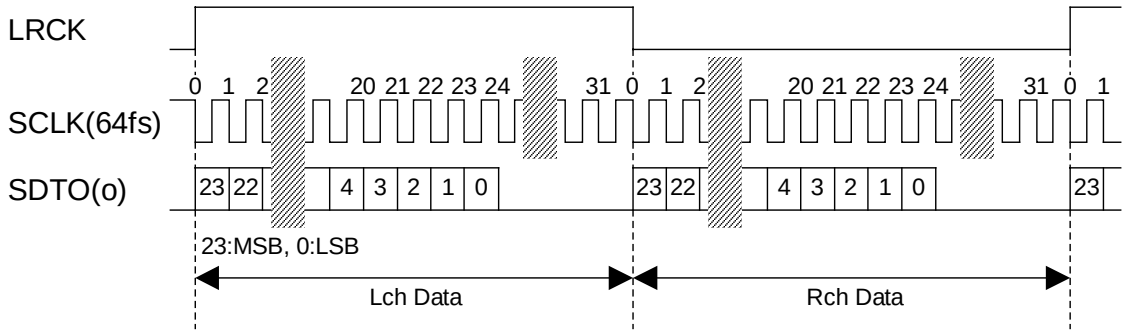


Figure 1. Mode 0 Timing

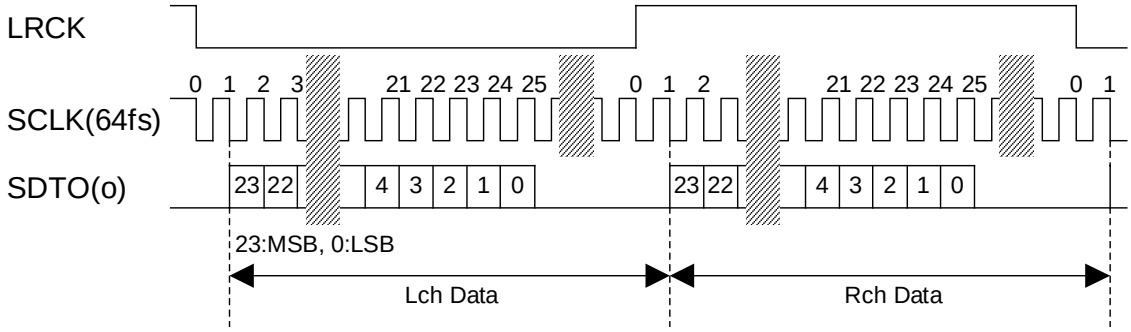


Figure 2. Mode 1 Timing

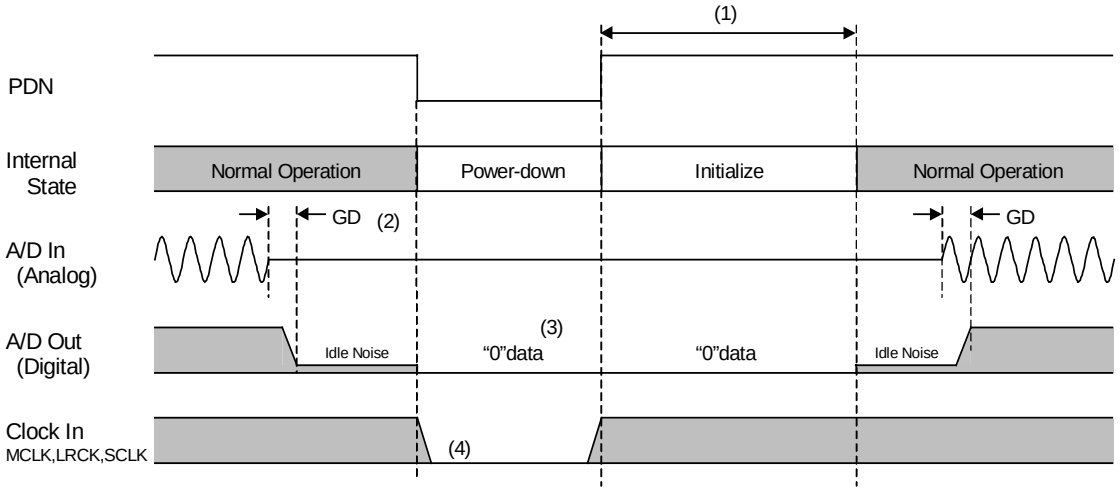
■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and scales with sampling rate (fs).

HPF is controlled by CKS2-0 pins (Table 3). If HPF setting (ON/OFF) is changed at operating, click noise occurs by changing DC offset. It is recommended that HPF setting is changed at PDN pin = "L".

■ Power down

The AK5386 is placed in the power-down mode by bringing PDN pin "L" and the digital filter is also reset at the same time. This reset should always be done after power-up. In the power-down mode, the VCOM are AGND level. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO becomes available after 4129 cycles of LRCK clock in master mode or 4132 cycles of LRCK clock in slave mode. During initialization, the ADC digital data outputs of both channels are forced to a 2's complement "0". The ADC outputs settle in the data corresponding to the input signals after the end of initialization (Settling approximately takes the group delay time).



Notes:
(1) 4132/fs in slave mode and 4129/fs in master mode.
(2) Digital output corresponding to analog input has the group delay (GD).
(3) A/D outputs "0" data at the power-down state.
(4) When the external clocks (MCLK, SCLK and LRCK) are stopped, the AK5386 should be in the power-down state.

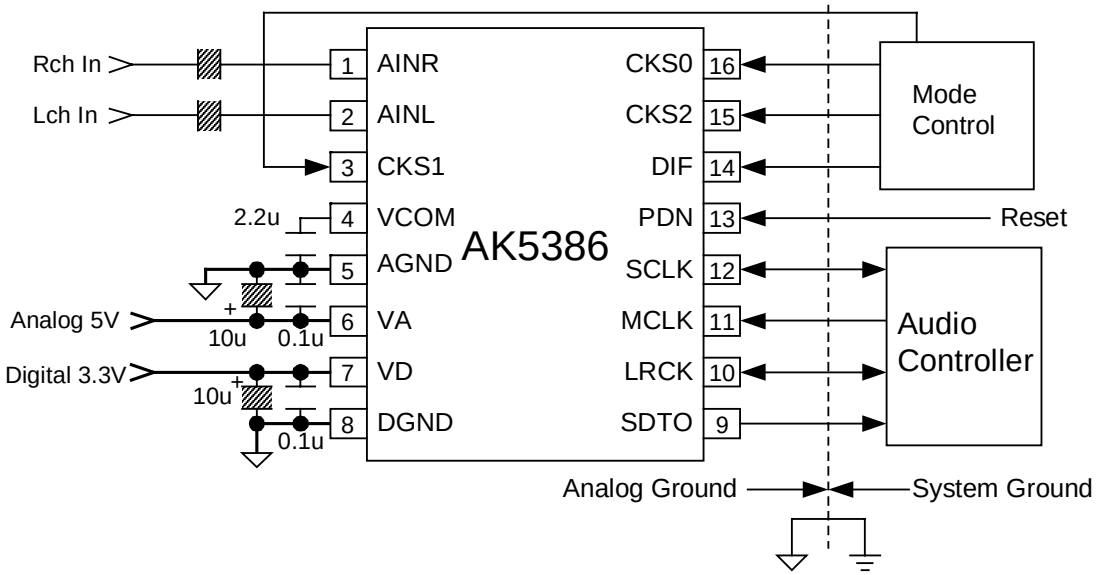
Figure 3. Power-down/up sequence example

■ System Reset

The AK5386 should be reset once by bringing PDN pin "L" after power-up. In slave mode, the internal timing starts clocking by the rising edge (falling edge at mode 1) of LRCK after exiting from reset and power down state by MCLK. The AK5386 is power down state until LRCK is input. In master mode, the internal timing starts when MCLK is input.

SYSTEM DESIGN

Figure 4 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Notes:
- AGND and DGND of the AK5386 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins should not be left floating.
- The CKS1 pin should be connected to VA or AGND.

Figure 4. Typical Connection Diagram

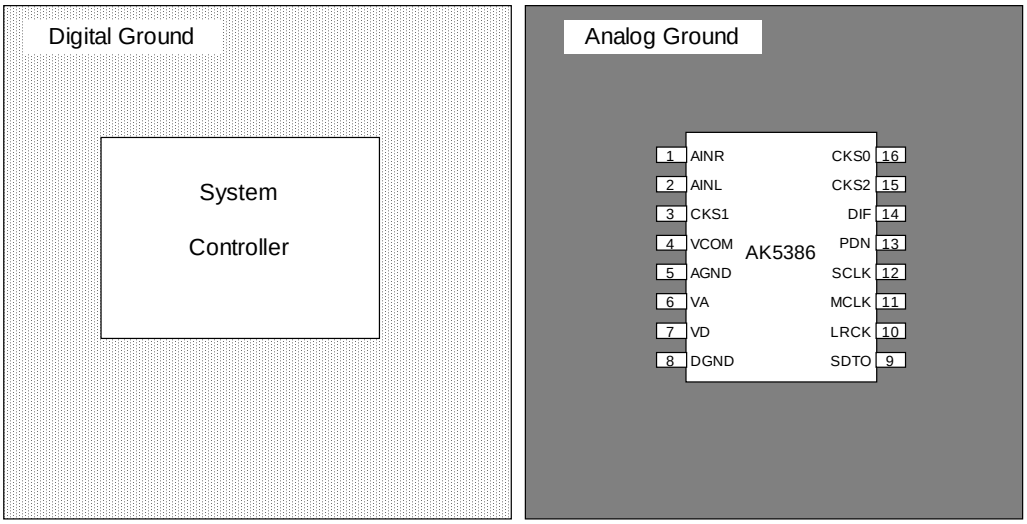


Figure 5. Ground Layout

Note: AGND and DGND must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK5386 requires careful attention to power supply and grounding arrangements. To minimize coupling from digital noise, decoupling capacitors should be connected to VA and VD respectively. VA is supplied from the analog supply in the system, and VD is supplied from the digital supply in the system. The power up sequence is not critical between VA and VD. **AGND and DGND of the AK5386 must be connected to one analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5386 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The voltage input to VA sets the analog input range. VCOM are 50%VA and normally connected to AGND with a 0.1μF ceramic capacitor. A capacitor 2.2μF attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VA and VCOM pins in order to avoid unwanted coupling into the AK5386.

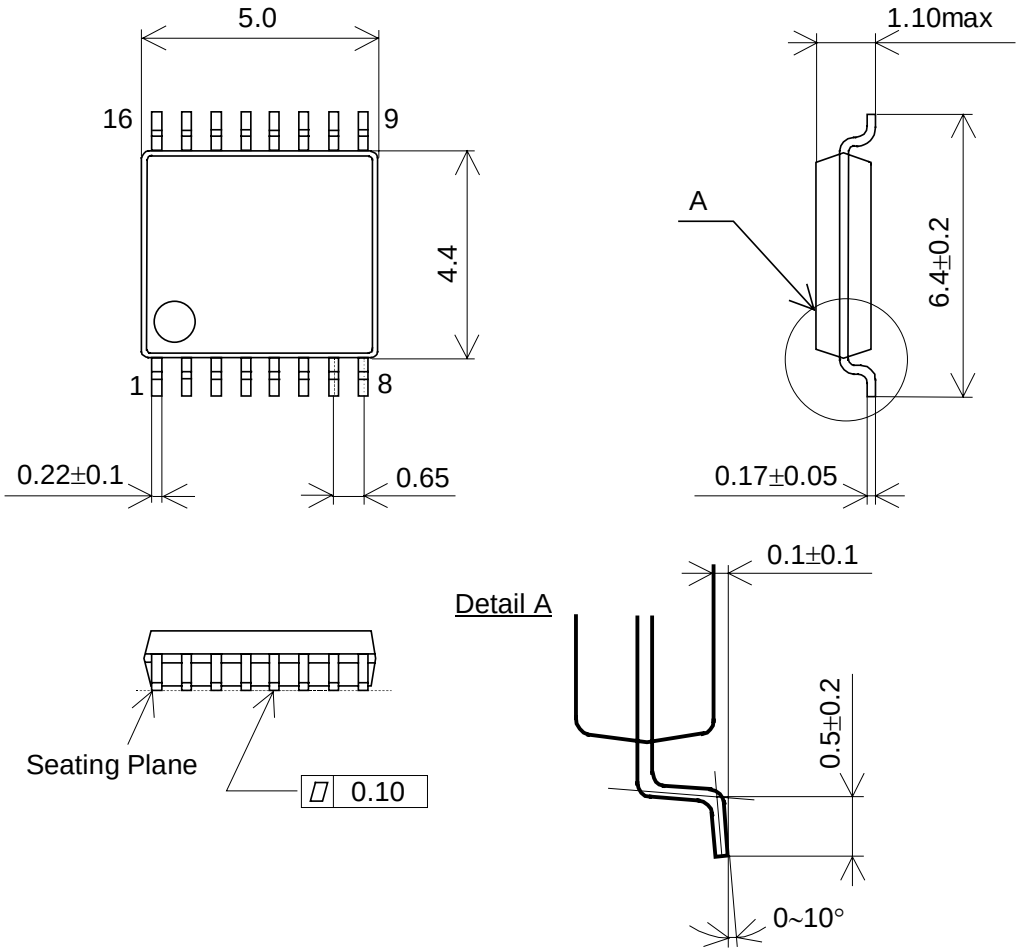
3. Analog Inputs

The ADC inputs are single-ended and internally biased to the common voltage (50%VA) with 6kΩ (typ, @fs=48kHz, 96kHz, 192kHz) resistance. The input signal range scales with the supply voltage and nominally 0.6xVA Vpp (typ). The ADC output data format is 2's complement. The internal HPF removes the DC offset.

The AK5386 samples the analog inputs at 128fs (@ fs=48kHz), 64fs (@ fs=96kHz) or 32fs(@ fs=192kHz). The digital filter rejects noise above the stop band except for multiples of 64fs or 32fs. The AK5386 includes an anti-aliasing filter (RC filter) to attenuate a noise around 128fs, 64fs or 32fs.

PACKAGE

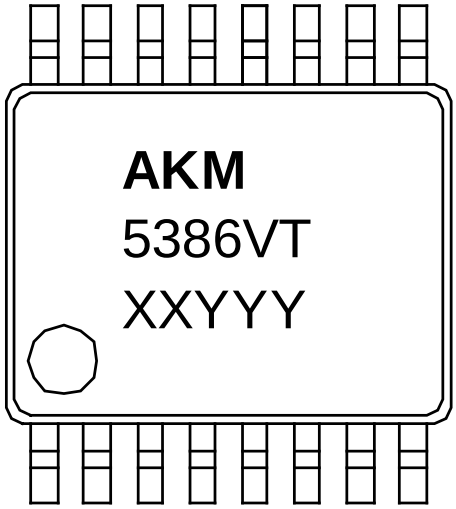
16pin TSSOP (Unit: mm)



■ **Material & Lead finish**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code: XXYYY (5 digits)
   XX: Lot#
   YYY: Date Code
3) Marketing Code: 5386VT

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/12/13	00	First Edition		

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