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AK4440

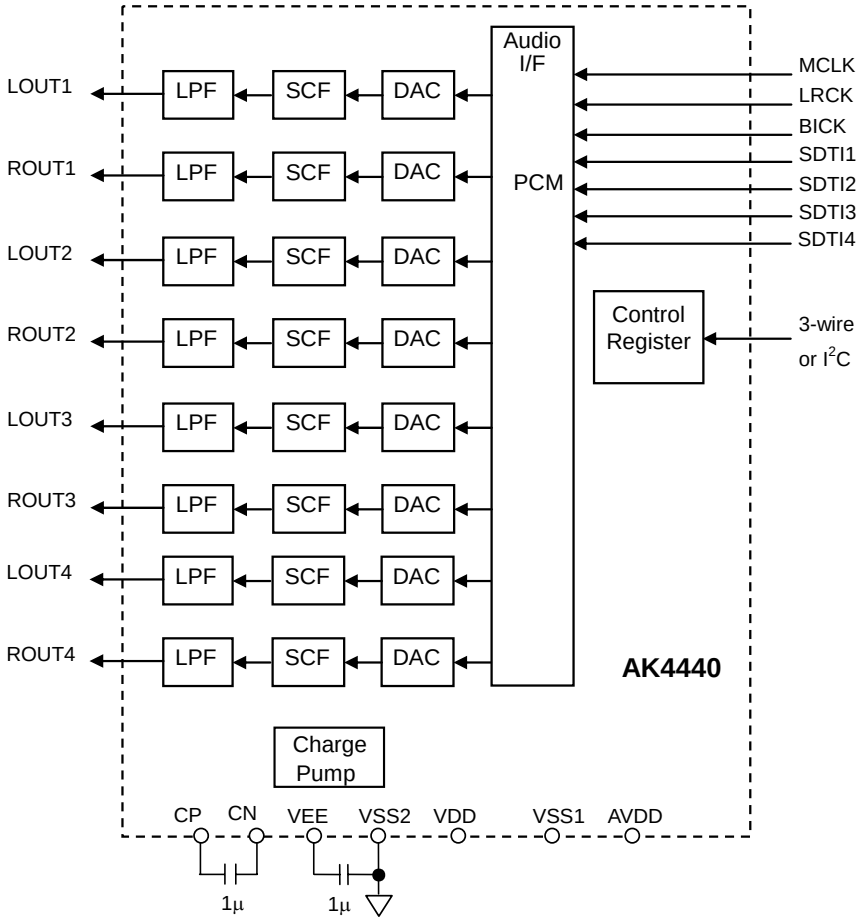
192kHz 24-Bit 8ch DAC with 2Vrms Output

GENERAL DESCRIPTION

The AK4440 is a 5V 24-bit 8ch DAC with an integrated 2Vrms output buffer. A charge pump in the buffer develops an internal negative power supply rail that enables a ground-referenced 2Vrms output. Using AKM's multi bit modulator architecture, the AK4440 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4440 integrates a combination of switched-capacitor and continuous-time filters, increasing performance for systems with excessive clock jitter. The 24-bit word length and 192kHz sampling rate make this part ideal for a wide range of consumer audio applications, such as DVD/BD, AV receiver, Home theater systems and set-top boxes. The AK4440 is offered in a space saving 30pin VSOP package.

FEATURES

- **Sampling Rate Ranging from 8kHz to 192kHz**
- **128 times Oversampling (Normal Speed Mode)**
- **64 times Oversampling (Double Speed Mode)**
- **32 times Oversampling (Quad Speed Mode)**
- **24Bit 8 times FIR Digital Filter with Slow roll-off option**
- **Switched-Capacitor Filter with High Tolerance to Clock Jitter**
- **Single Ended 2Vrms Output Buffer**
- **Digital De-emphasis Filter: 32kHz, 44.1kHz or 48kHz**
- **Soft mute**
- **Control I/F: 3-wire Serial and I^2C Bus**
- **Audio I/F format: MSB justified, LSB justified (16bit, 20bit, 24bit), I^2S, TDM**
- **Master clock: 256fs, 384fs, 512fs or 768fs or 1152fs (Normal Speed Mode)**
  128fs, 192fs, 256fs or 384fs (Double Speed Mode)
  128fs or 192fs (Quad Speed Mode)
- **THD+N: -93dB**
- **Dynamic Range: 105dB**
- **Automatic Power-on Reset Circuit**
- **Power Supply: +4.5 to +5.5V**
- **Ta = -20 to 85°C**
- **Small Package: 30 pin VSOP (9.7mm x 7.6mm)**

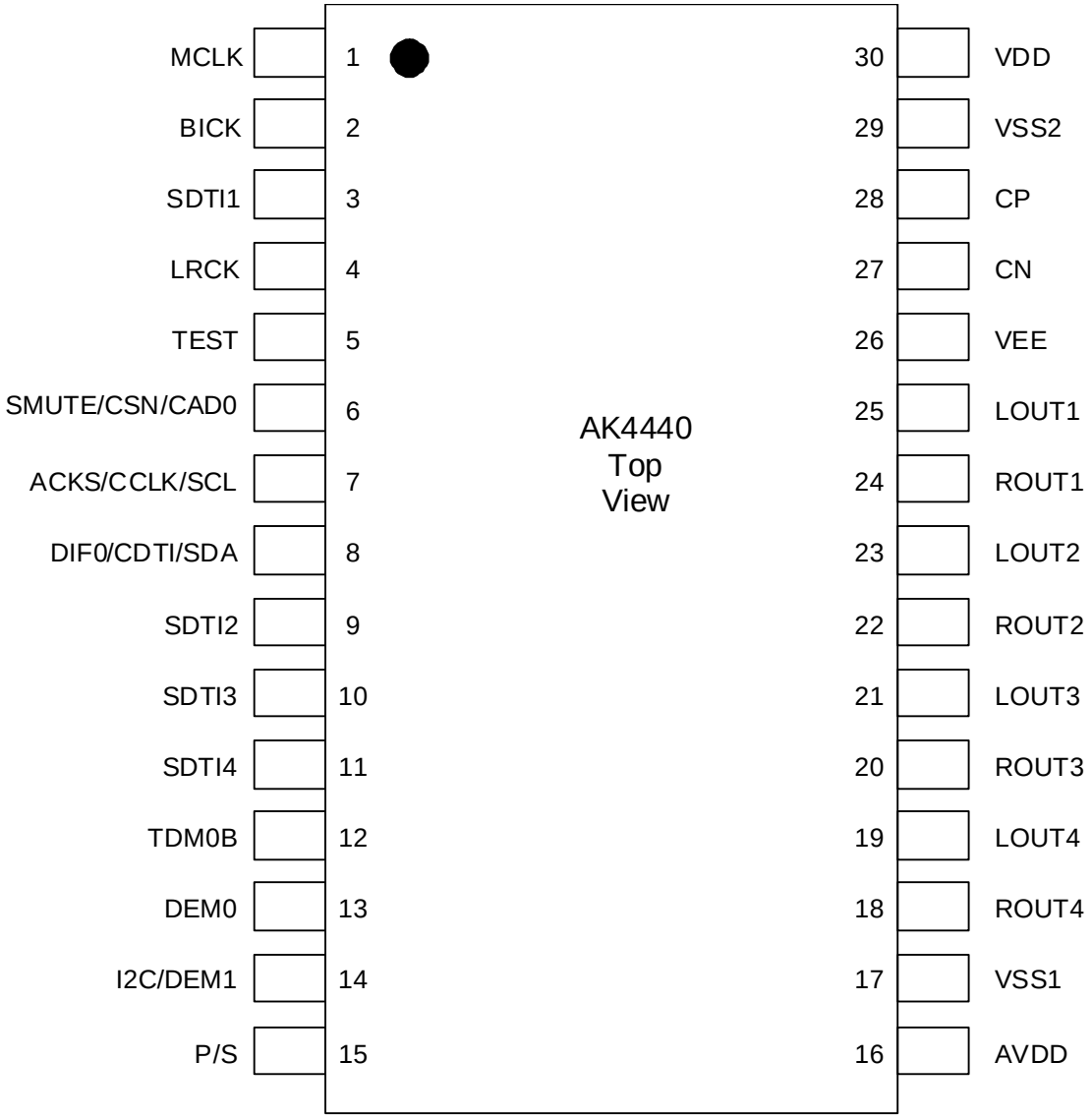


Block Diagram

■ Ordering Guide

AK4440EF	-20 ~ +85°C	30pin VSOP
AKD4440	Evaluation Board for AK4440	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI1	I	DAC1 Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	TEST	O	TEST pin. This pin should be open.
6	SMUTE	I	Soft Mute Pin in parallel mode "H": Enable, "L": Disable
	CSN	I	Chip Select Pin in serial 3-wire mode
	CAD0	I	Chip Address Pin in serial I^2C mode
7	ACKS	I	Auto Setting Mode Pin in parallel mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock Pin in serial 3-wire mode
	SCL		Control Data Clock Pin in serial I^2C mode
8	DIF0	I	Audio Data Interface Format Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial 3-wire mode
	SDA	I/O	Control Data Pin in serial I^2C mode
9	SDTI2	I	DAC2 Audio Serial Data Input Pin
10	SDTI3	I	DAC3 Audio Serial Data Input Pin
11	SDTI4	I	DAC4 Audio Serial Data Input Pin
12	TDM0B	I	TDM I/F Format Mode in parallel control mode "L": TDM256 mode, "H": Normal mode
13	DEM0	I	De-emphasis Filter Enable Pin in parallel mode
14	I2C	I	Control Mode Select Pin in serial mode "L": 3-wire Serial, "H": I^2C Bus
	DEM1	I	De-emphasis Filter Enable Pin in parallel mode
15	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin, typ 100kΩ) "L": Serial control mode, "H": Parallel control mode
16	AVDD	-	DAC Analog Power Supply Pin: 4.5V~5.5V
17	VSS1	-	Ground Pin
18	ROUT4	O	DAC4 Rch Analog Output Pin
19	LOUT4	O	DAC4 Lch Analog Output Pin
20	ROUT3	O	DAC3 Rch Analog Output Pin
21	LOUT3	O	DAC3 Lch Analog Output Pin
22	ROUT2	O	DAC2 Rch Analog Output Pin
23	LOUT2	O	DAC2 Lch Analog Output Pin
24	ROUT1	O	DAC1 Rch Analog Output Pin
25	LOUT1	O	DAC1 Lch Analog Output Pin
26	VEE	O	Negative Voltage Output Pin Connect to VSS2 with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the VSS2 pin. Non polarity capacitors can also be used.
27	CN	I	Negative Charge Pump Capacitor Terminal Pin Connect to CP with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.
28	CP	I	Positive Charge Pump Capacitor Terminal Pin Connect to CN with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.

PIN/FUNCTION (Continued)

No.	Pin Name	I/O	Function
29	VSS2	-	Ground Pin
30	VDD	-	Charge Pump and DAC Digital Power Supply Pin: 4.5V~5.5V

Note: All input pins except for the P/S pin should not be left floating.

■ Handling of Unused Pin

The following tables illustrate recommended states for open pins:

Classification	Pin Name	Setting
Analog	LOUT4-1, ROUT4-1	Leave open.
Digital	SDTI4-1	Connect to VSS2.
	DEM0, TDM0B (Serial control mode)	Connect to VDD or VSS2.
	TEST	Leave open.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	+6.0	V
	AVDD	-0.3	+6.0	V
Input Current (any pins except supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS1 and VSS2 must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	+4.5	+5.0	+5.5	V
	AVDD		VDD		

Note 3. VDD and AVDD are the same voltage.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=AVDD = +5.0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data; Measurement frequency=20Hz ~ 20kHz; R_L ≥5kΩ; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				24	Bits
Dynamic Characteristics (Note 4)					
THD+N (0dBFS)	fs=44.1kHz, BW=20kHz		-93	-84	dB
	fs=96kHz, BW=40kHz		-92	-	dB
	fs=192kHz, BW=40kHz		-92	-	dB
Dynamic Range (-60dBFS with A-weighted, Note 5)		98	105		dB
S/N (A-weighted, Note 6)		98	105		dB
Interchannel Isolation (1kHz)		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
DC Accuracy					
DC Offset (at output pin)		-60	0	+60	mV
Gain Drift			100		ppm/°C
Output Voltage (Note 7)		1.97	2.12	2.27	Vrms
Load Capacitance (Note 8)				25	pF
Load Resistance		5			kΩ
Power Supplies					
Power Supply Current: (Note 9)					
Power Supply Current: (Note 9)					
Normal Operation (fs≤96kHz)			80	110	mA
Normal Operation (fs=192kHz)			85	120	mA
Power-Down Mode (Note 10)			20	100	μA

Note 4. Measured by Audio Precision (System Two). Refer to the evaluation board manual.
Note 5. 98dB for 16bit input data
Note 6. S/N does not depend on input data size.
Note 7. Full-scale voltage (0dB). Output voltage is proportional to the voltage of AVDD,
AOUT (typ.@0dB) = 2.12Vrms × VDD/5.
Note 8. In case of driving capacitive load, inset a resistor between the output pin and the capacitive load.
Note 9. The current into VDD and AVDD.
Note 10. The P/S pin is tied to VDD and the all other digital inputs including clock pins (MCLK, BICK and LRCK) are tied to VSS2.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = 4.5 ~ 5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "0")

Parameter			Symbol	min	typ	max	Units
Digital filter							
Passband	±0.05dB	(Note 11)	PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband		(Note 11)	SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay		(Note 12)	GD	-	19.3	-	1/fs
Digital Filter + SCF + LPF							
Frequency Response	20.0kHz	Fs=44.1kHz	FR	-	±0.05	-	dB
	40.0kHz	Fs=96kHz	FR	-	±0.05	-	dB
	80.0kHz	Fs=192kHz	FR	-	±0.05	-	dB

Note 11. The passband and stopband frequencies scale with fs(system sampling rate). For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note 12. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = 4.5~5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "1")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.04dB	(Note 13)	PB	0		8.1	kHz
	-3.0dB			-	18.2	-	kHz
Stopband		(Note 13)	SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay		(Note 12)	GD	-	19.3	-	1/fs
Digital Filter + SCF + LPF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0.1/-4.3	-	dB
	40.0kHz	fs=96kHz	FR	-	+0.1/-3.3	-	dB
	80.0kHz	fs=192kHz	FR	-	+0.1/-3.7	-	dB

Note 13. The passband and stopband frequencies scale with fs. For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; VDD=AVDD = 4.5 ~ 5.5V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	2.2	-	-	V
Low-Level Input Voltage		VIL	-	-	0.8	V
Low-Level Output Voltage						V
DIF0/CDTI/SDA	(Iout = 3mA)	VOL	-		0.4	V
Input Leakage Current	(Note 14)	Iin	-	-	± 10	μA

Note 14. The current of the P/S pin is not included. The P/S pin has an internal pull-up resistor (typ.100kΩ).

SWITCHING CHARACTERISTICS

(Ta = 25°C; VDD=AVDD= +4.5 ~ +5.5V; C_L = 20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency	fCLK	2.048		36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Normal Mode (TDM0= "0", TDM1= "0")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	60		96	kHz
Quad Speed Mode	fsq	120		192	kHz
Duty Cycle	Duty	45		55	%
TDM256 mode (TDM0= "1", TDM1= "0")					
Normal Speed Mode	fsn	8		48	kHz
High time	tLRH	1/256fs			ns
Low time	tLRL	1/256fs			ns
TDM128 mode (TDM0= "1", TDM1= "1")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	60		96	kHz
High time	tLRH	1/128fs			ns
Low time	tLRL	1/128fs			ns
Audio Interface Timing					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	30			ns
Pulse Width High	tBCKH	30			ns
BICK "↑" to LRCK Edge (Note 15)	tBLR	20			ns
LRCK Edge to BICK "↑" (Note 15)	tLRB	20			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
Control Interface Timing (3-wire Serial control mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN High Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 16)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

Note 15. BICK rising edge must not occur at the same time as LRCK edge.
Note 16. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 17. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

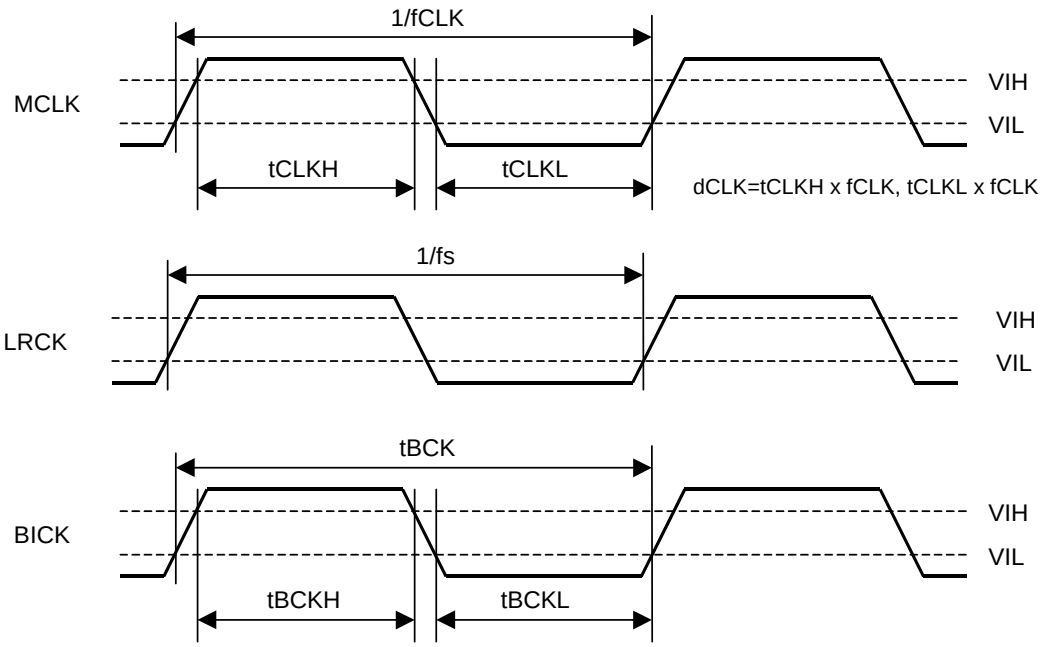


Figure 1. Clock Timing

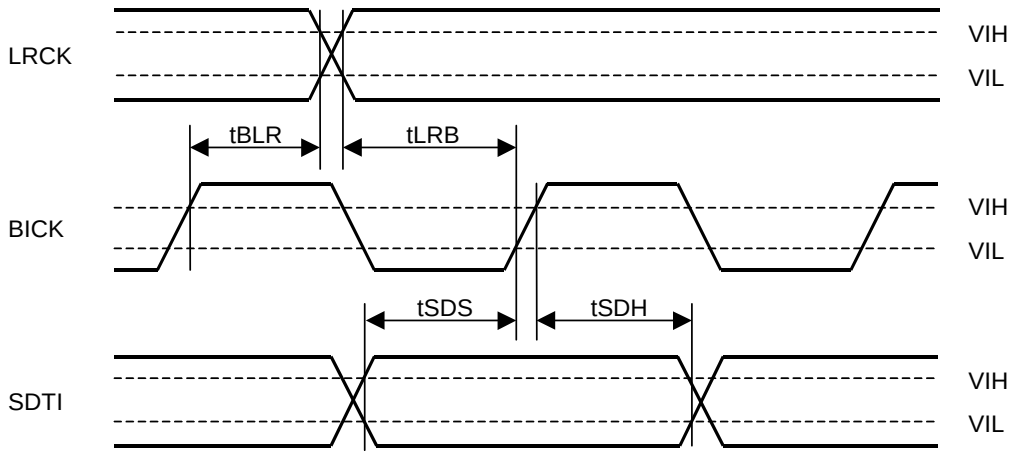


Figure 2. Audio Serial Interface Timing

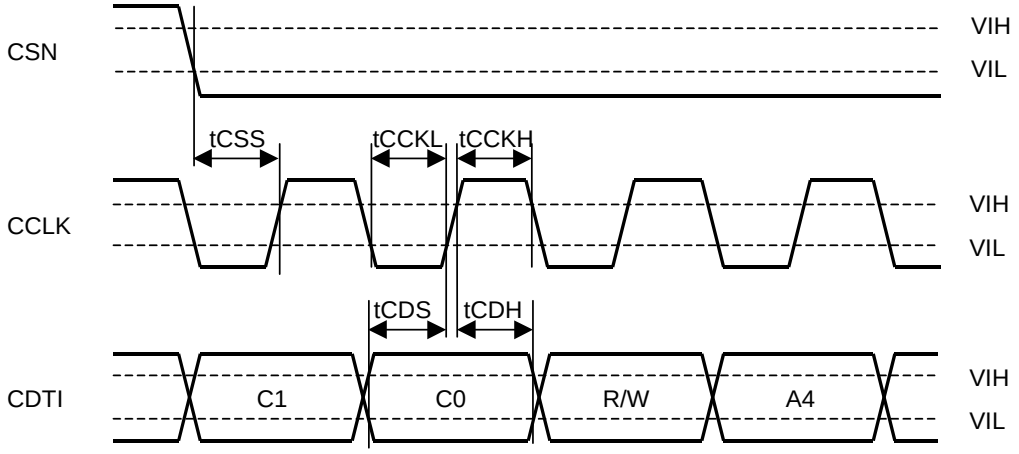


Figure 3. WRITE Command Input Timing

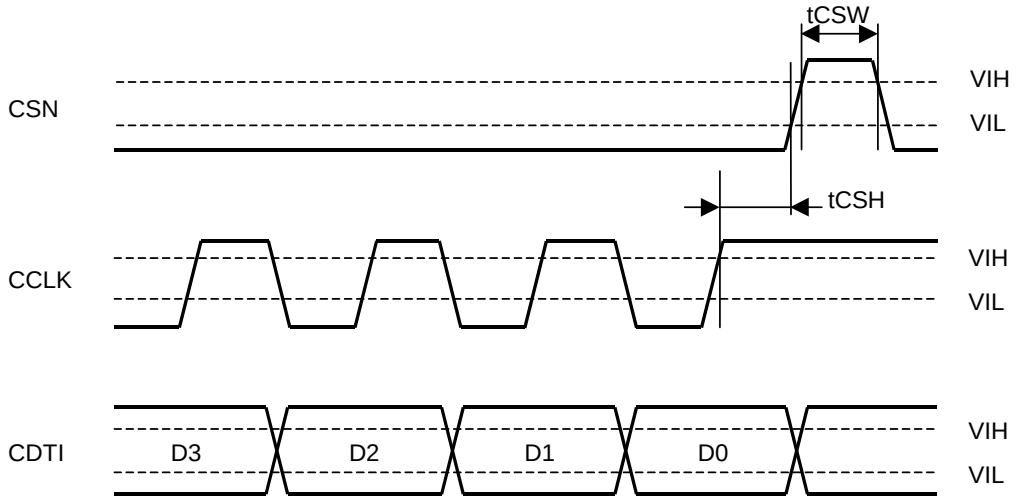


Figure 4. WRITE Data Input Timing

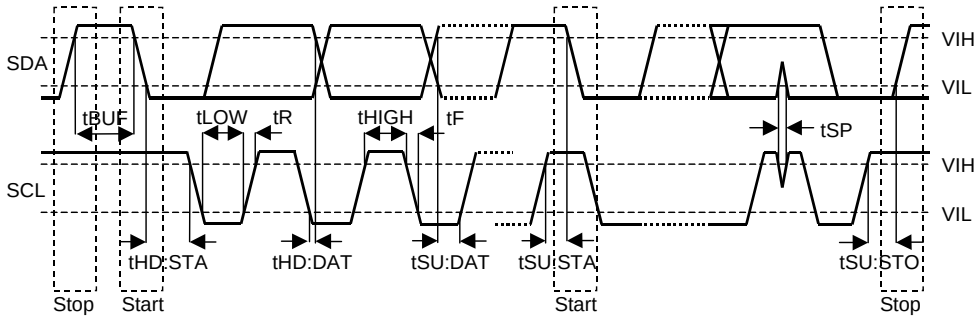


Figure 5. I^{2}C Bus mode Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4440, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit = "0": Register 00H), the sampling speed is set by DFS1-0 bits (Table 1). The frequency of MCLK for each sampling speed is set automatically. (Table 2~Table 4) In auto setting mode (ACKS bit = "1": Default), as MCLK frequency is detected automatically (Table 5), and the internal master clock becomes the appropriate frequency (Table 6), it is not necessary to set DFS1-0 bits.

In parallel control mode, the sampling speed can be set by only the ACKS pin. When ACKS pin = "L", the AK4440 operates by Normal Speed Mode. When ACKS pin = "H", auto setting mode is enabled. The parallel control mode does not support 128fs and 192fs of double speed mode.

The AK4440 is automatically placed in power saving mode when MCLK, LRCK and BICK stop during normal operation mode, and the analog output is forced to 0V(typ). When MCLK, LRCK and BICK are input again, the AK4440 is powered up. After power-up, the AK4440 is in the power-down mode until MCLK, LRCK and BICK are input.

DFS1 bit	DFS0 bit	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	(default)
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

LRCK	MCLK					BICK
fs	256fs	384fs	512fs	768fs	1152fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	36.8640MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	N/A	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	N/A	3.0720MHz

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode) (N/A: Not available)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	11.2896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 5. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)							Sampling Speed
Fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
88.2kHz	-	-	22.5792	33.8688	-	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Serial Interface Format

In parallel control mode, the DIF0 and TDM0B pins as shown in Table 7 can select four serial data modes. The register value of DIF0 and TDM0B bits are ignored. In serial control mode, the DIF2-0 and TDM1-0 bits shown in Table 8 can select 11 serial data modes. Initial value of DIF2-0 bits is "010". In all modes the serial data is MSB-first, 2's complement format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

In parallel control mode, when the TDM0B pin = "L", the audio interface format is TDM256 mode (Table 7). The audio data of all DACs (eight channels) are input to the SDTI1 pin. The input data to SDTI2-4 pins are ignored. BICK should be fixed to 256fs.

In serial control mode, when the TDM0 bit = "1" and the TDM1 bit = "0", the audio interface format is TDM256 mode (Table 8), and the audio data of all DACs (eight channels) are input to the SDTI1 pin. The input data to the SDTI2-4 pins are ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be at least 1/256fs. The audio data is MSB-first, 2's complement format. The input data to the SDTI1 pin is latched on the rising edge of BICK. In TDM128 mode (TDM1-0 bits = "11", Table 8), the audio data of DACs (four channels; L1, R1, L2, R2) are input to the SDTI1 pin. The other four data (L3, R3, L4, R4) are input to the SDTI2 pin. The input data to SDTI3-4 pins are ignored. BICK should be fixed to 128fs. The audio data is MSB-first, 2's complement format. The input data to SDTI1-2 pins are latched on the rising edge of BICK.

Mode		TDM0B pin	DIF0 pin	SDTI Format	LRCK	BICK	Figure
Normal	2	H	L	24-bit MSB Justified	H/L	≥48fs	Figure 8
	3	H	H	24-bit I^2S Compatible	L/H	≥48fs	Figure 9
TDM256	5	L	L	24-bit MSB Justified	↑	256fs	Figure 10
	6	L	H	24-bit I^2S Compatible	↓	256fs	Figure 11

Table 7. Audio Data Formats (Parallel control mode)

Mode		TDM1 bit	TDM0 bit	DIF2 bit	DIF1 bit	DIF0 bit	SDTI Format	LRCK	BICK	Figure
Normal	0	0	0	0	0	0	16-bit LSB Justified	H/L	≥32fs	Figure 6
	1	0	0	0	0	1	20-bit LSB Justified	H/L	≥40fs	Figure 7
	2	0	0	0	1	0	24-bit MSB Justified	H/L	≥48fs	Figure 8
	3	0	0	0	1	1	24-bit I^2S Compatible	L/H	≥48fs	Figure 9
	4	0	0	1	0	0	24-bit LSB Justified	H/L	≥48fs	Figure 7
TDM256		0	1	0	0	0	N/A			
		0	1	0	0	1	N/A			
	5	0	1	0	1	0	24-bit MSB Justified	↑	256fs	Figure 10
	6	0	1	0	1	1	24-bit I^2S Compatible	↓	256fs	Figure 11
	7	0	1	1	0	0	24-bit LSB Justified	↑	256fs	Figure 12
TDM128		1	1	0	0	0	N/A			
		1	1	0	0	1	N/A			
	8	1	1	0	1	0	24-bit MSB Justified	↑	128fs	Figure 13
	9	1	1	0	1	1	24-bit I^2S Compatible	↓	128fs	Figure 14
	10	1	1	1	0	0	24-bit LSB Justified	↑	128fs	Figure 15

Table 8. Audio Data Formats (Serial control mode) (N/A: Not available)

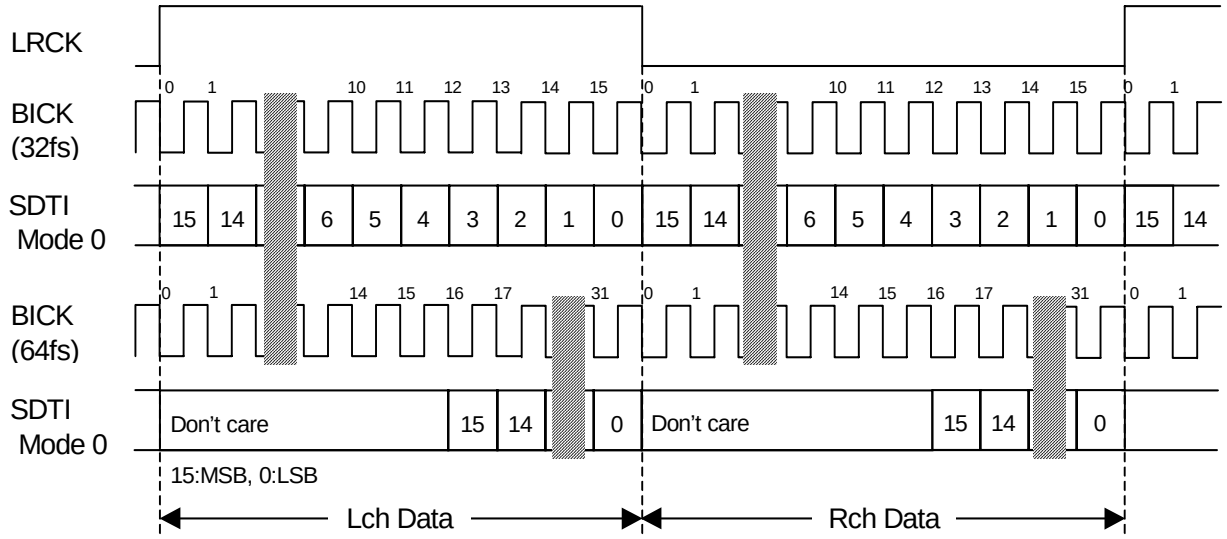


Figure 6. Mode 0 Timing

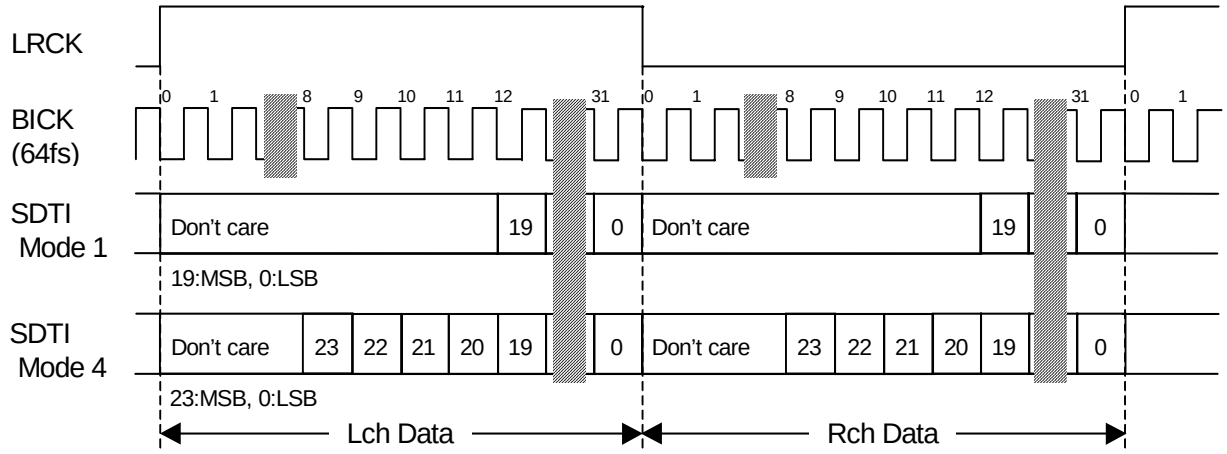


Figure 7. Mode 1/4 Timing

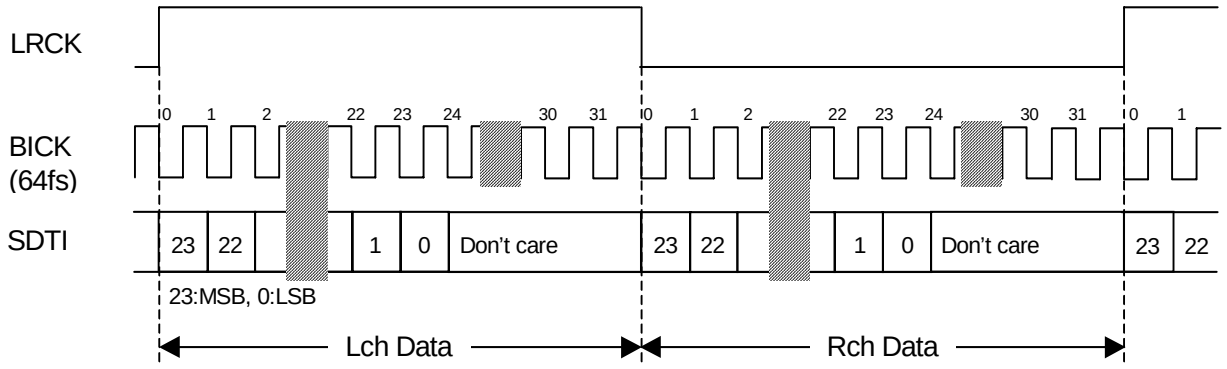


Figure 8. Mode 2 Timing

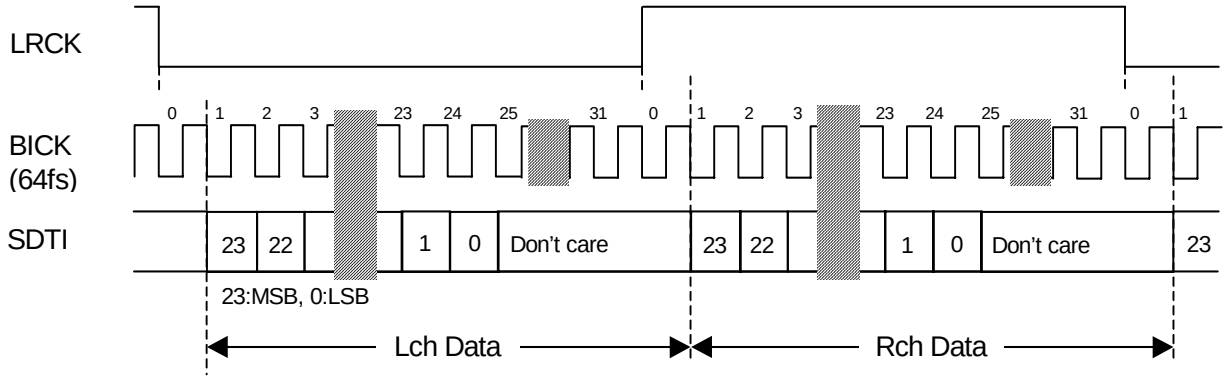


Figure 9. Mode 3 Timing

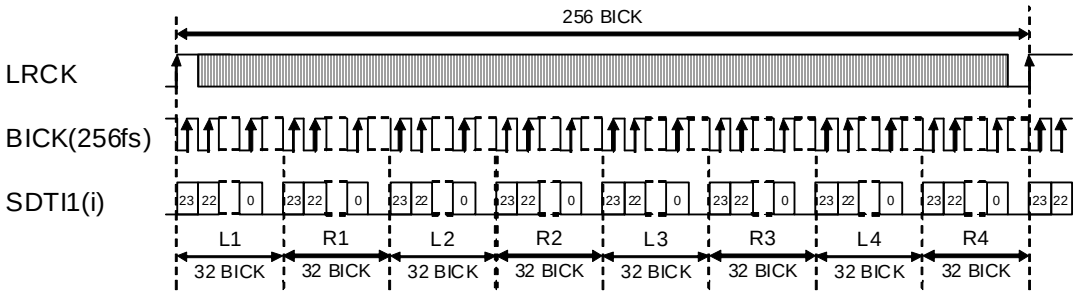


Figure 10. Mode 5 Timing

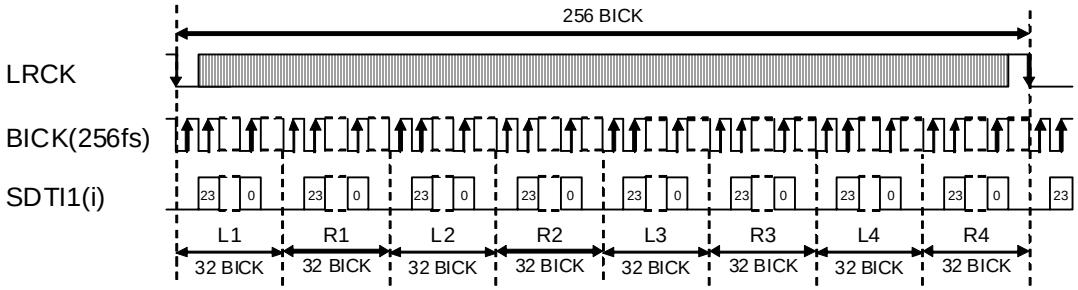


Figure 11. Mode 6 Timing

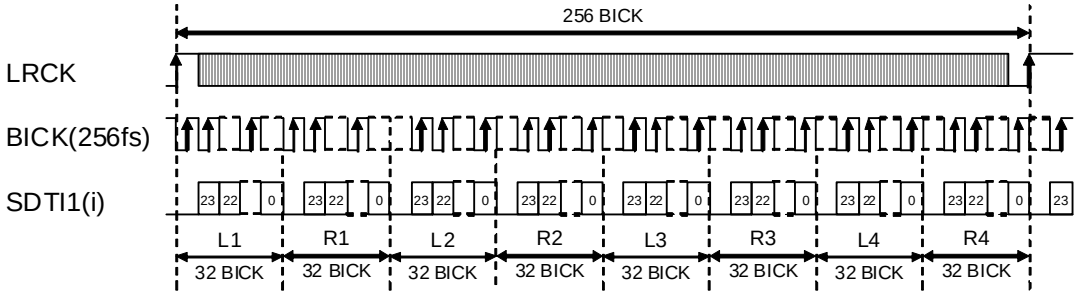


Figure 12. Mode 7 Timing

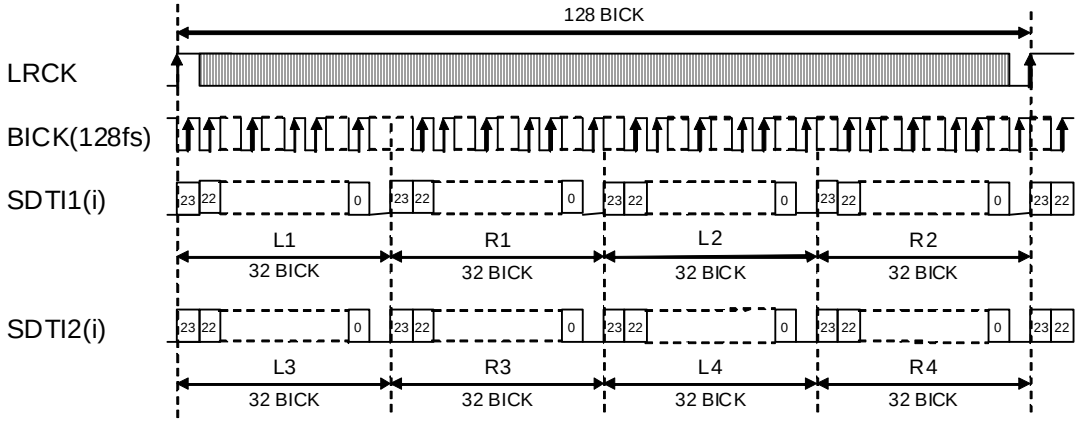


Figure 13. Mode 8 Timing

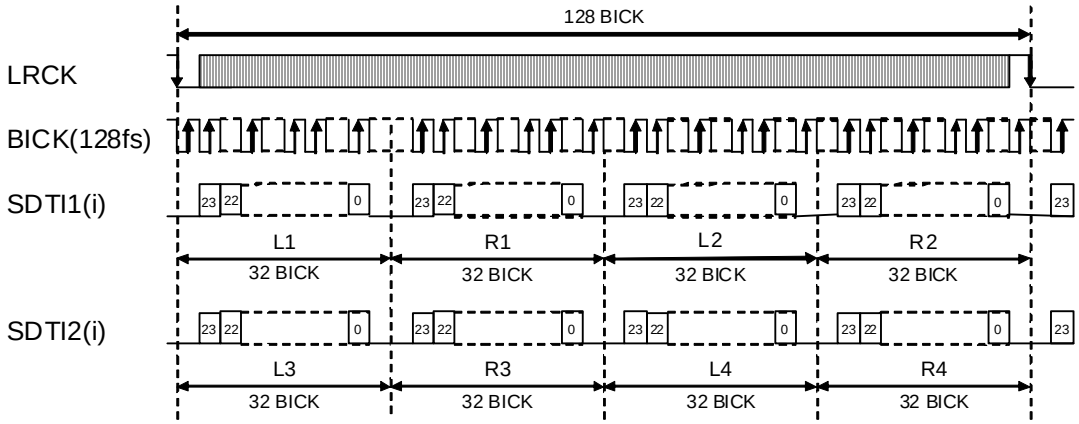


Figure 14. Mode 9 Timing

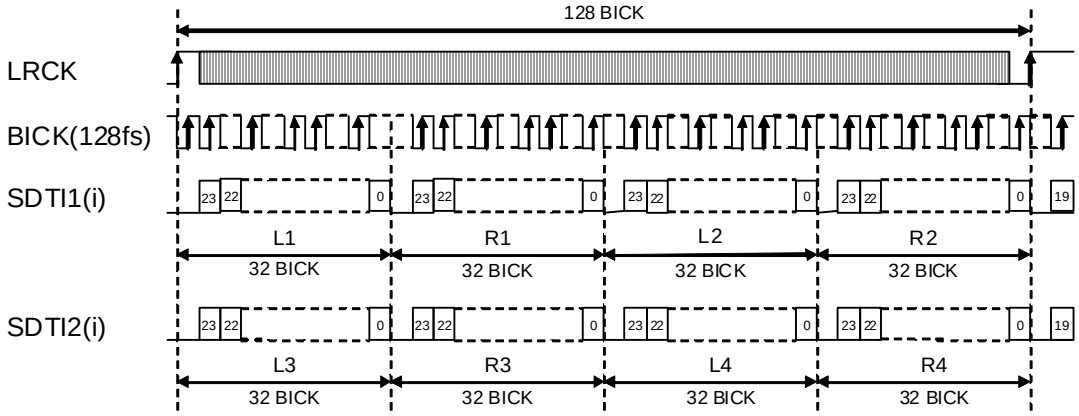


Figure 15. Mode 10 Timing

■ Analog Output Block

The internal negative power supply generation circuit (Figure 16) provides a negative power supply for the internal 2Vrms amplifier. It allows the AK4440 to output an audio signal centered at VSS (0V, typ) as shown in Figure 17. The negative power generation circuit (Figure 16) needs 1.0μF low ESR (Equivalent Series Resistance) capacitors (Ca, Cb). If this capacitor is polarized, the positive polarity pin should be connected to the CP and VSS2 pins. This circuit operates by clocks generated from MCLK. When MCLK stops, the AK4440 is placed in the reset mode automatically and the analog outputs settle to VSS (0V, typ).

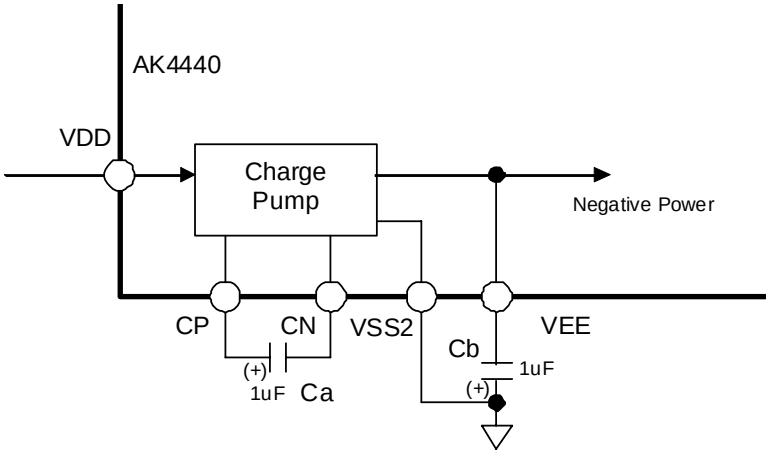


Figure 16. Negative Power Generation Circuit

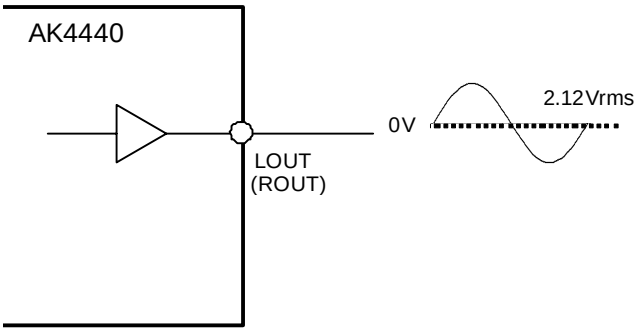


Figure 17. Audio Signal Output

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15μs). For double speed and quad speed modes, the digital de-emphasis filter is always off. In serial control mode, the DEM1-0 bits are valid for the DAC enabled by the DEMA-D bits (Table 9). In parallel control mode, DEM1-0 pins are valid (Table 10).

DEM1 bit	DEM0 bit	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

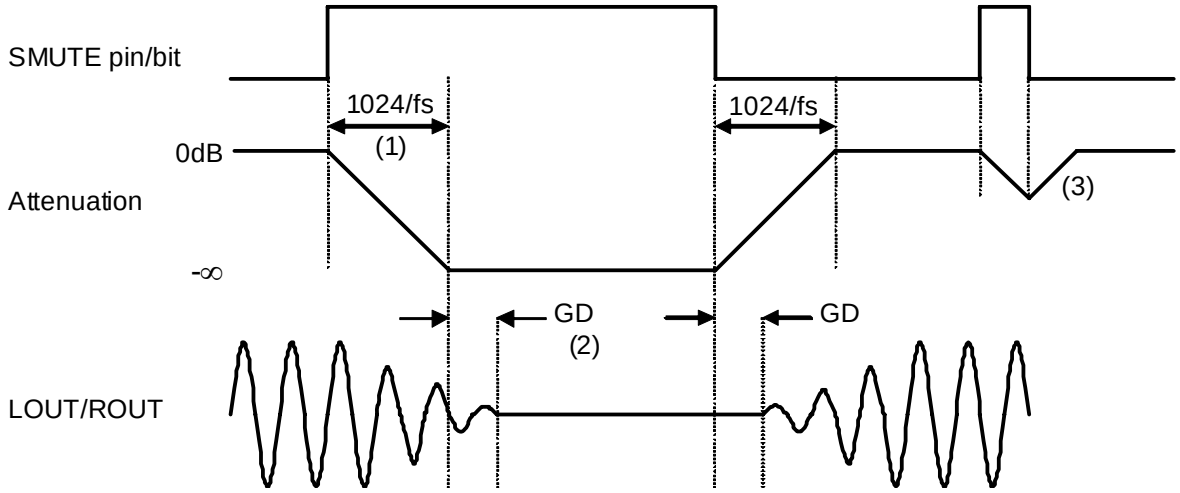
Table 9 De-emphasis Filter Control in Serial Control Mode (Normal Speed Mode)

DEM1 pin	DEM0 pin	Mode	
L	L	44.1kHz	
L	H	OFF	(default)
H	L	48kHz	
H	H	32kHz	

Table 10 De-emphasis Filter Control in Parallel Control Mode (Normal Speed Mode)

■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When the SMUTE pin/bit is set "1", the output signal is attenuated to -∞ in 1024 LRCK cycles. When the SMUTE pin/bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to 0dB in 1024 LRCK cycles. If the soft mute is cancelled within the 1024 LRCK cycles after starting this operation, the attenuation is discontinued and it is returned to 0dB by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The time for input data to be attenuated to -∞, is
Normal Speed Mode: 1024 LRCK cycles (1024/fs).
Double Speed Mode: 2048 LRCK cycles (2048/fs).
Quad Speed Mode: 4096 LRCK cycles (4096/fs).

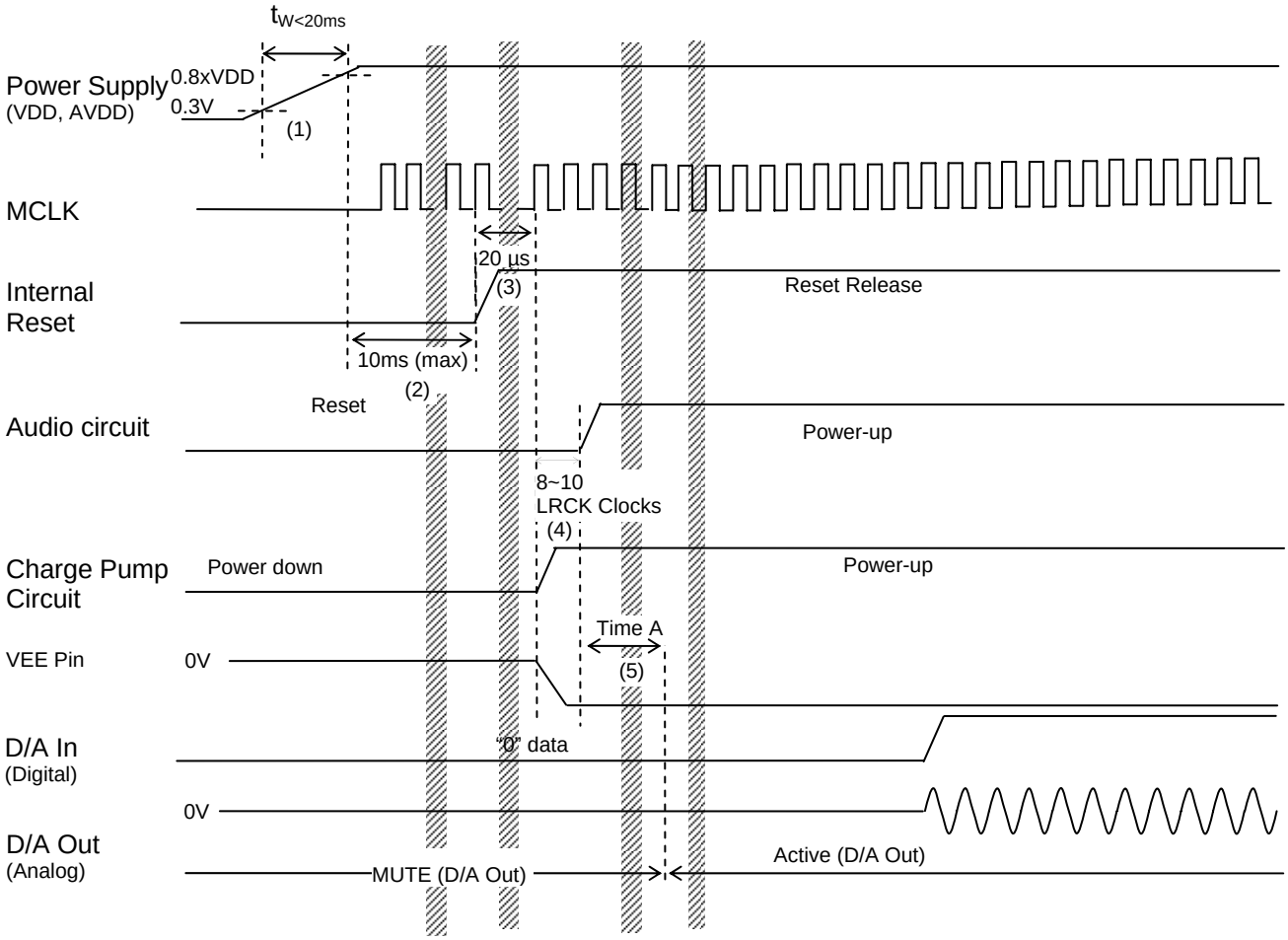
(2) The analog output corresponding to a specific digital input has group delay, GD.

(3) If soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level in the same cycle.

Figure 18. Soft Mute Function

■ System Reset

The AK4440 is in power down mode upon power-up. The MLCK should be input after the power supplies are ramped up. The AK4440 is in power-down mode until LRCK are input.



Notes:

(1) The AK4440 includes an internal Power on Reset Circuit which is used reset the digital logic into a default state after power up. Therefore, the power supply voltage must reach 80% VDD from 0.3V in less than 20msec.

(2) Register writings are valid after 10ms (max).

(3) When internal reset is released, approximately 20us after a MCLK input, the internal analog circuit is powered-up.

(4) The digital circuit and charge pump circuit are powered-up in 8~10 LRCK cycles when the analog circuit is powered-up.

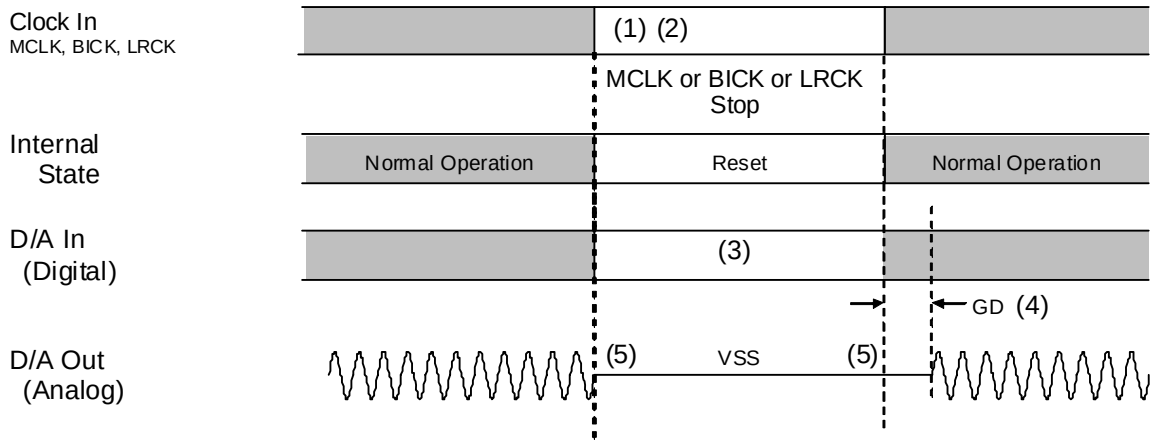
(5) The charge pump counter starts after the charge pump circuit is powered-up. The DAC outputs a valid analog signal after Time A.

Time A = 1024/(fs x 16): Normal speed mode
Time A = 1024/(fs x 8): Double speed mode
Time A = 1024/(fs x 4): Quad speed mode

Figure 19. System Reset Diagram

■ Reset Function

When the MCLK, LRCK or BICK stops, the AK4440 is placed in reset mode and its analog outputs are set to VSS (0V, typ). When the MCLK, LRCK and BICK are restarted, the AK4440 returns to normal operation mode.



Notes:

(1) Clocks (MCLK, BICK, LRCK) can be stopped in the reset mode (MCLK or LRCK or BICK is stopped).
(2) The AK4440 detects the stop of LRCK or BICK if LRCK or BICK stops for more than 2048/fs. When LRCK is stopped, the AK4440 exits reset mode after LRCK is inputted. When BICK is stopped, the AK4440 exits reset mode after BICK is input.
(3) Digital data can be stopped. The click noise after MCLK, LRCK and BICK are input again can be reduced by inputting the "0" data during this period.
(4) The analog output corresponding to a specific digital input has group delay (GD).
(5) No audible click noise occurs under normal conditions.

Figure 20. Reset Timing Example

■ Register Control Interface

The AK4440's functions are controlled by registers. Two types of control mode write internal registers. In the I^2C-bus mode, the chip address is determined by the state of the CAD0 pin. In 3-wire mode, the chip address is fixed to "11". Writing "0" to the RSTN bit resets the internal timing circuit, but the registers are not initialized.

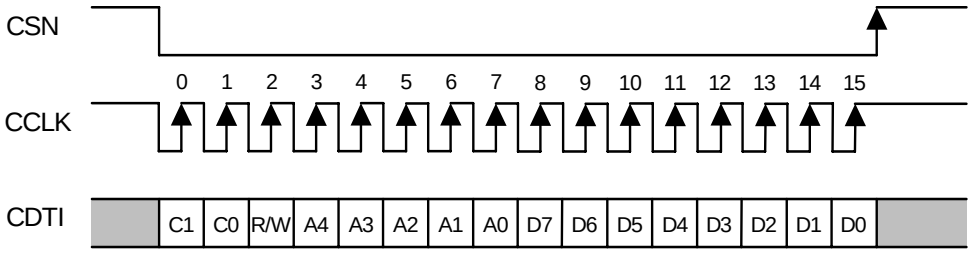
* The AK4440 does not support read commands.
* When the state of the P/S pin is changed, the AK4440 should be reset by the RSTB bit = "0".
* In serial control mode, the setting of parallel pins is invalid.

Function	Parallel Control Mode	Serial Control Mode
Double sampling mode at 128/192fs	-	X
De-emphasis	X	X
SMUTE	X	X
16/20/24bit LSB justified format	-	X
TDM256 mode	X	X
TDM128 mode	-	X

Table 11 Function Table (X: Available, -: Not available)

(1) 3-wire Serial Control Mode (I2C pin = "L")

The 3-wire μP interface pins, CSN, CCLK and CDTI, write internal registers. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "11"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). The AK4440 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by the rising edge of CSN. The clock speed of CCLK is 5MHz (max).



C1-C0: Chip Address (Fixed to "11")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 21. Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4440 supports the fast-mode I²C-bus system (max: 400kHz).

Figure 22 shows the data transfer sequence at the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 26). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit which is a data direction bit (R/W) (Figure 23). The most significant six bits of the slave address are fixed as "001001". The next one bit is CAD0 (device address bit). The bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) set them. If the slave address match that of the AK4440 and R/W bit is "0", the AK4440 generates an acknowledge and the write operation is executed. If R/W bit is "1", the AK4440 does not answer any acknowledge (Figure 27).

The second byte consists of the address for control registers of the AK4440. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 24). Those data after the second byte contain control data. The format is MSB first, 8bits (Figure 25). The AK4440 generates an acknowledge after each byte is received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 26).

The AK4440 is capable of more than one byte write operation by one sequence. After receipt of the third byte, the AK4440 generates an acknowledge, and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the addresses exceed 03H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 28) except for the START and the STOP condition.

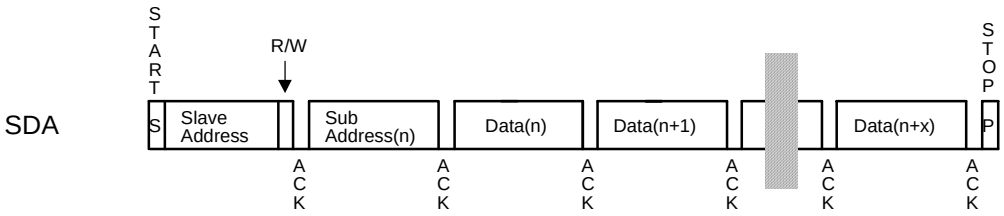


Figure 22. Data transfer sequence at the I²C-bus mode

0	0	1	0	0	1	CAD0	R/W

(This CAD0 should match with CAD0 pin)

Figure 23. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 24. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 25. Byte structure after the second byte

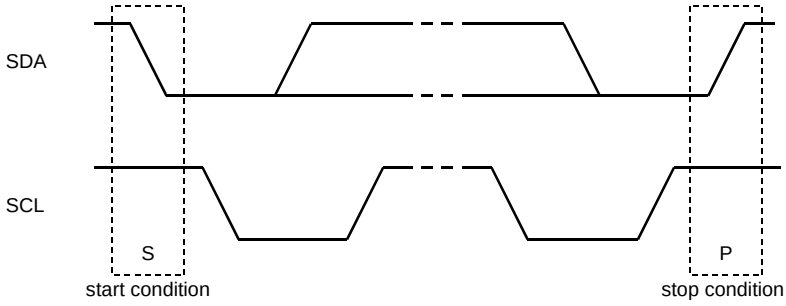


Figure 26. START and STOP conditions

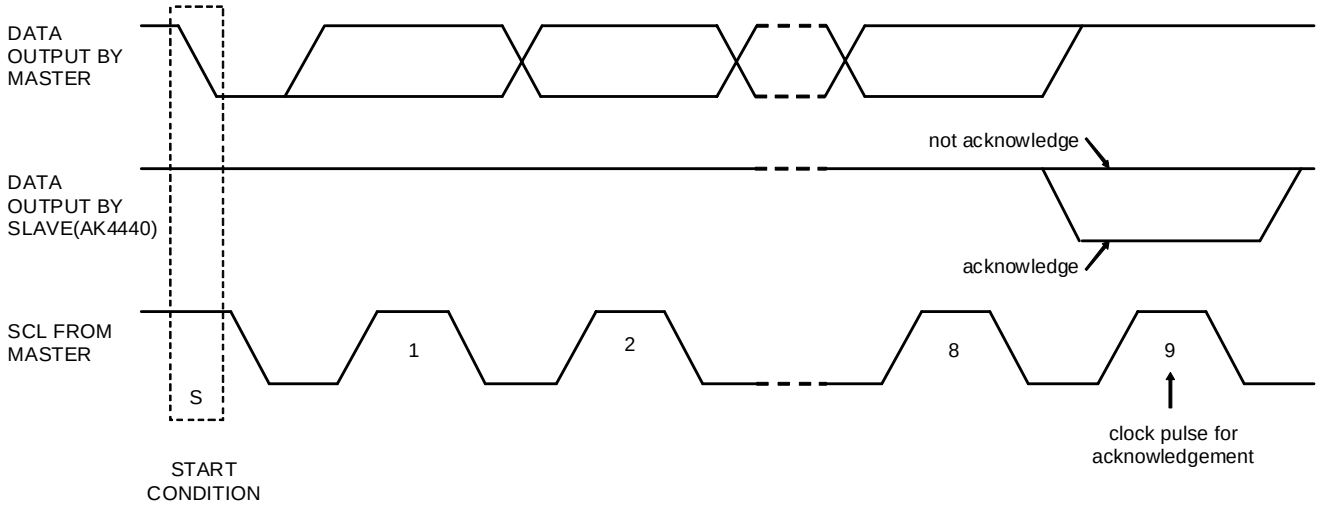


Figure 27. Acknowledge on the I^2C-bus

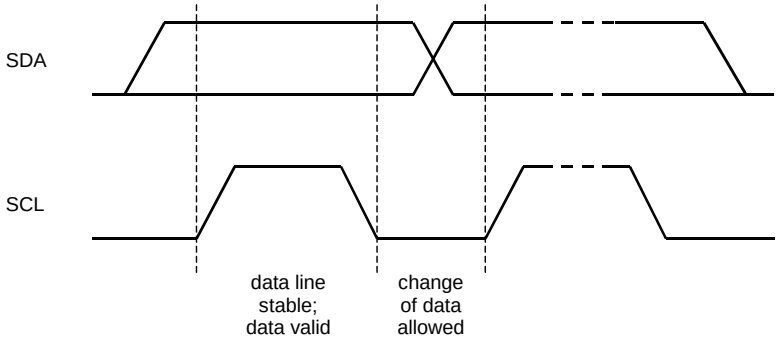


Figure 28. Bit transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	TDM1	TDM0	DIF2	DIF1	DIF0	0	RSTN
01H	Control 2	RRST	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Power Down Control	0	0	0	0	PW4	PW3	PW2	PW1
03H	DEM Control	0	0	0	0	DEMA	DEMB	DEMC	DEMD

Note: For addresses from 04H to 1FH, data must not be written.
Do not write the registers within 10msec after the power supplies are fed.
All data can be written to the registers even if PW1-4 and RSTN bits are "0".
When RSTN bit goes to "0", only internal timing is reset, and the registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	TDM1	TDM0	DIF2	DIF1	DIF0	0	RSTN
Default		1	0	0	0	1	0	0	1

RSTN: Internal timing reset
0: Reset. Any registers are not initialized.
1: Normal operation

DIF2-0: Audio data interface modes (Table 8)
Default: "010"

TDM0-1: TDM Mode Select

Mode	TDM1	TDM0	BICK	SDTI	Sampling Speed
Normal	0	0	32fs~	1-4	Normal, Double, Quad Speed
TDM256	0	1	256fs fixed	1	Normal Speed
TDM128	1	1	128fs fixed	1-2	Normal, Double Speed

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS1-0 bits is ignored. When this bit is "0", DFS1-0 bits set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	RRST	0	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
Default		0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal operation
1: DAC outputs soft-muted

DEM1-0: De-emphasis Response (Table 9, Table 10)
Default: "01", OFF

DFS1-0: Sampling speed control (Table 1)
00: Normal speed
01: Double speed

10: Quad speed
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

SLOW: Slow Roll-off Filter Enable
0: Sharp Roll-off Filter
1: Slow Roll-off Filter

RRST: All registers are initialized.
0: Normal Operation
1: Reset. All registers are initialized.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Down Control	0	0	0	0	PW4	PW3	PW2	PW1
Default		0	0	0	0	1	1	1	1

PW4-1: Power-down control (0: Power-down, 1: Power-up)
PW1: Power down control of DAC1
PW2: Power down control of DAC2
PW3: Power down control of DAC3
PW4: Power down control of DAC4

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	DEM Control	0	0	0	0	DEMA	DEMB	DEMC	DEMD
Default		0	0	0	0	0	0	0	0

DEMA-D: De-emphasis Enable bit of DAC1/2/3/4
0: Disable
1: Enable

SYSTEM DESIGN

Figure 29 and Figure 30 show the system connection diagram. The evaluation board (AKD4440) demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

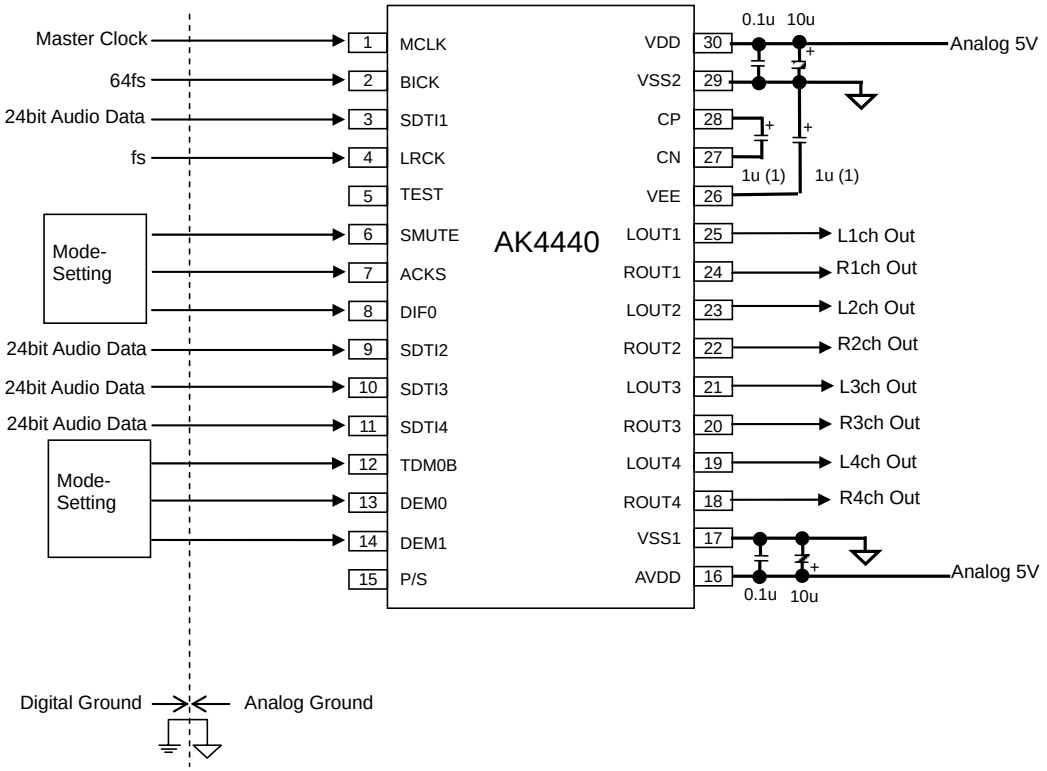


Figure 29. Typical Connection Diagram (Parallel Control Mode)

Notes:
- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- The capacitor of low ESR should be used to the capacitor (1). When it uses the capacitor with the polarity, the positive pole of the capacitor should be connected to CP pin and VSS2 pin.
- All input pins except for the P/S pin should not be left floating.

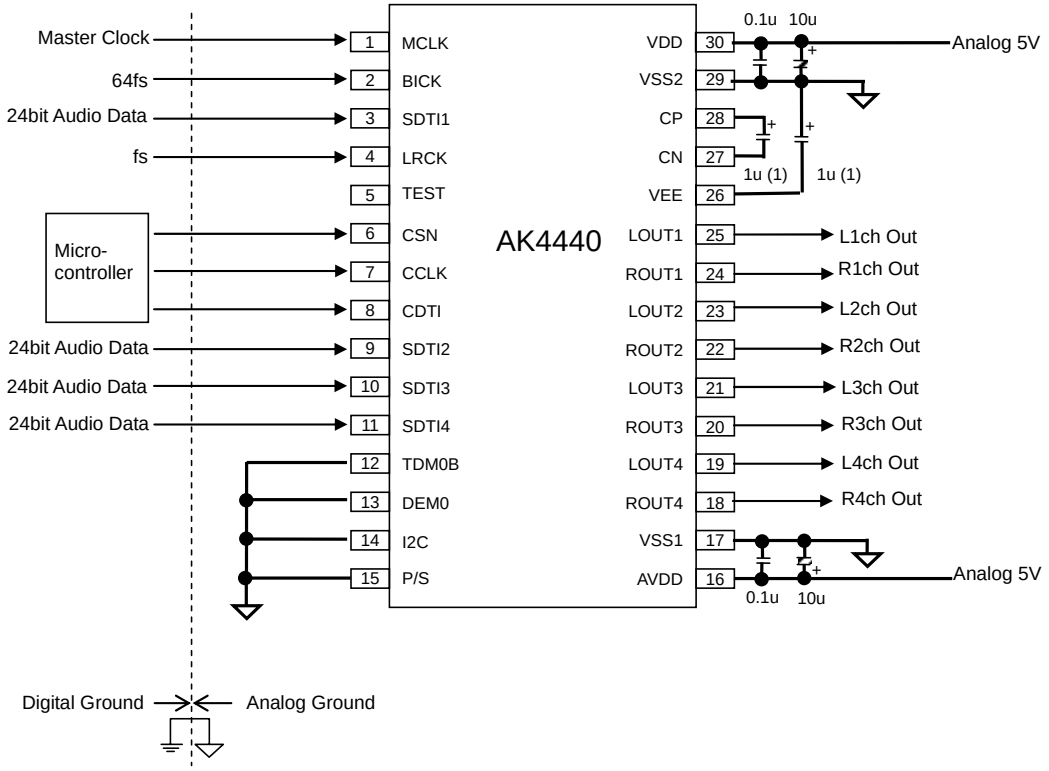


Figure 30. Typical Connection Diagram (3-wire Serial Control Mode)

Notes:
- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- The capacitor of low ESR should be used to the capacitor (1). When it uses the capacitor with the polarity, the positive pole of the capacitor should be connected to CP pin and VSS2 pin.
- All input pins except for the P/S pin should not be left floating.

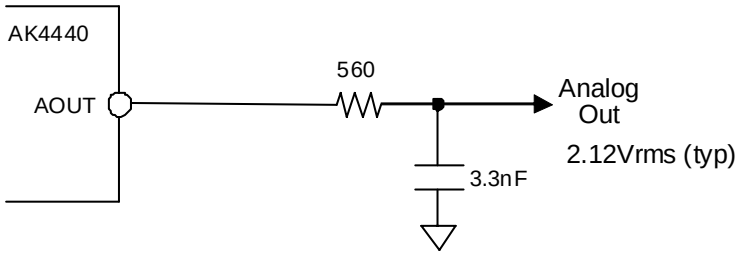
1. Grounding and Power Supply Decoupling

VDD and AVDD are supplied from the analog supply and should be separated from the system digital supply. Decoupling capacitors, especially 0.1μF ceramic capacitors for high frequency bypass, should be placed as near to VDD and AVDD as possible. The VSS1 and VSS2 must be connected to the same analog ground plane. **Power-up sequence between VDD and AVDD is not critical.**

2. Analog Outputs

The analog outputs are single-ended and centered around the VSS (ground) voltage. The output signal range is typically 2.12Vrms (typ @AVDD=5V). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Using single a 1st-order LPF (Figure 31) can reduce noise beyond the audio passband.

The output voltage is a positive full scale for 7FFFFFH (@24bit data) and a negative full scale for 800000H (@24bit data). The ideal output is 0V (VSS) voltage for 000000H (@24bit data). The DC offset is ±60mV or less.

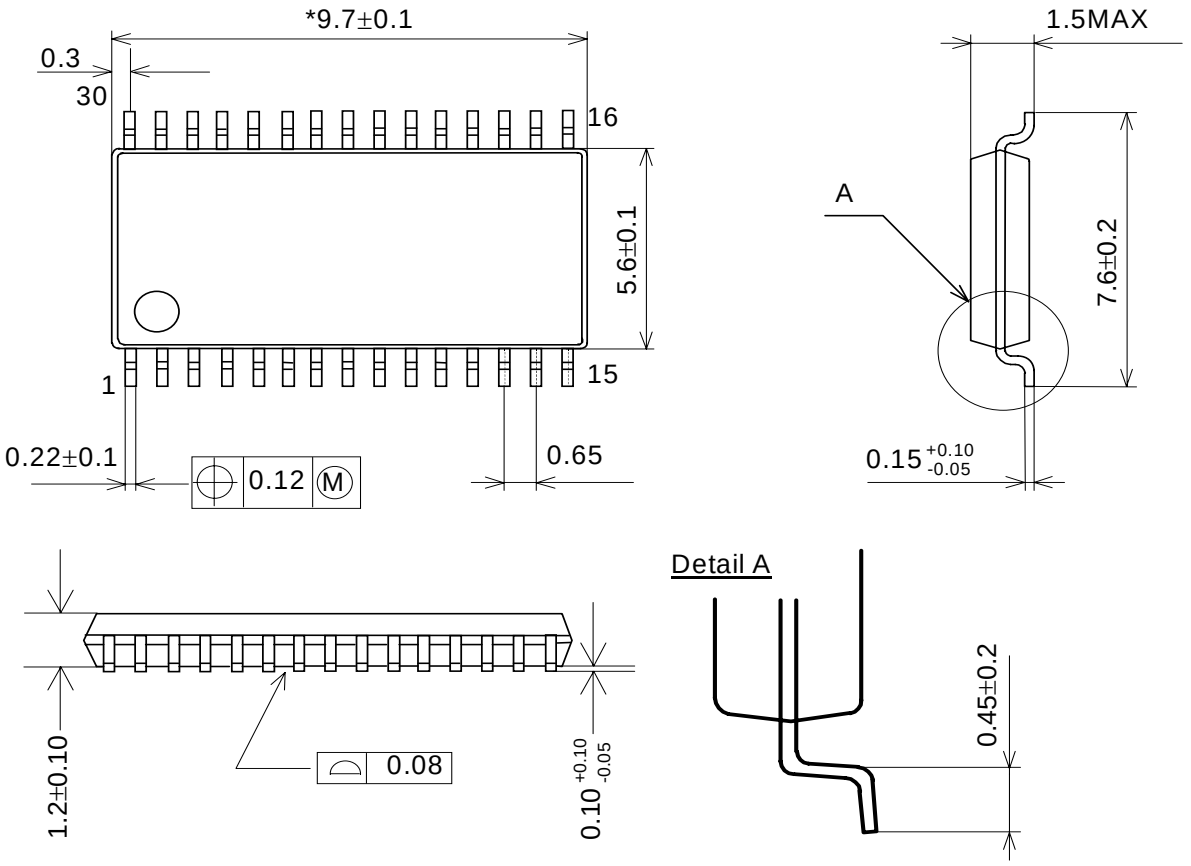


(fc = 86.1kHz, gain = -0.85dB @ 40kHz, gain = -2.70dB @ 80kHz)

Figure 31. External 1st order LPF Circuit Example1

PACKAGE

30pin VSOP (Unit: mm)



NOTE: Dimension "*" does not include mold flash.

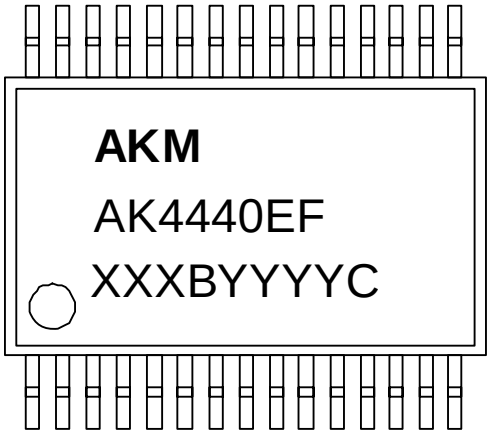
■ Package & Lead frame material

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

RoHS Compliance

*All integrated circuits form Asahi Kasei Microdevices Corporation (AKM) assembled in "lead-free" packages are fully compliant with RoHS.

MARKING



XXXBYYYYC Date code identifier

XXXB: Lot number (X: Digit number, B: Alpha character)
YYYYC: Assembly date (Y: Digit number, C: Alpha character)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
09/10/15	00	First Edition		
11/03/01	01	Error Correction	28	1. Grounding and Power Supply Decoupling The description was changed.

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  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKM products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.