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19-1081; Rev 1; 8/96

MAXIM

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

General Description

The MAX113/MAX117 are microprocessor-compatible, 8-bit, 4-channel and 8-channel analog-to-digital converters (ADCs). They operate from a single +3V supply and use a half-flash technique to achieve a 1.8µs conversion time (400ksps). A power-down pin (PWRDN) reduces current consumption to 1µA typical. The devices return from power-down mode to normal operating mode in less than 900ns, allowing large supply-current reductions in burst-mode applications. (In burst mode, the ADC wakes up from a low-power state at specified intervals to sample the analog input signals.) Both converters include a track/hold, enabling the ADC to digitize fast analog signals.

Microprocessor (µP) interfaces are simplified because the ADC can appear as a memory location or I/O port without external interface logic. The data outputs use latched, three-state buffer circuitry for direct connection to an 8-bit parallel µP data bus or system input port. The MAX113/MAX117 input/reference configuration enables ratiometric operation.

The 4-channel MAX113 is available in a 24-pin DIP or SSOP. The 8-channel MAX117 is available in a 28-pin DIP or SSOP. For +5V applications, refer to the MAX114/MAX118 data sheet.

Applications

Battery-Powered Systems
System-Health Monitoring
Communications Systems
Portable Equipment
Remote Data Acquisition

Features

- **+3.0V to +3.6V Single-Supply Operation**
- **4 (MAX113) or 8 (MAX117) Analog Input Channels**
- **Low Power: 1.5mA (operating mode)**
  1µA (power-down mode)
- **Total Unadjusted Error ≤ 1LSB**
- **Fast Conversion Time: 1.8µs per Channel**
- **No External Clock Required**
- **Internal Track/Hold**
- **Ratiometric Reference Inputs**
- **Internally Connected 8th Channel Monitors Reference Voltage (MAX117)**

Ordering Information

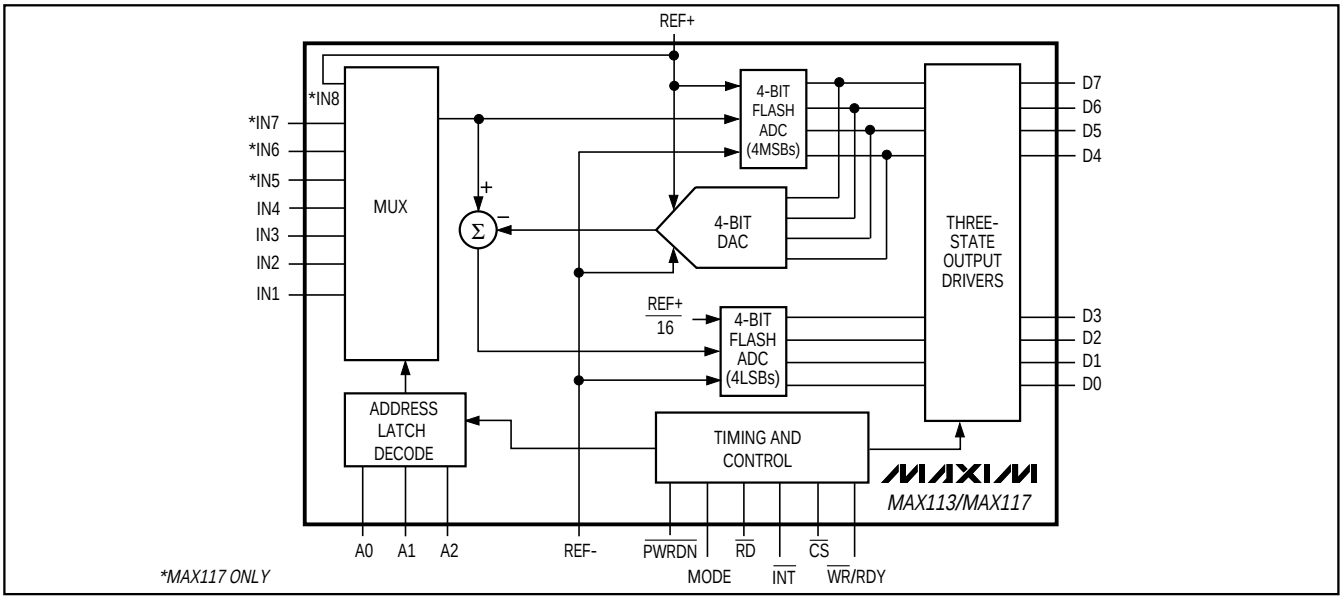
PART	TEMP. RANGE	PIN-PACKAGE
MAX113CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX113CAG	0°C to +70°C	24 SSOP
MAX113C/D	0°C to +70°C	Dice*
MAX113ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX113EAG	-40°C to +85°C	24 SSOP
MAX113MRG	-55°C to +125°C	24 Narrow CERDIP**

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability.*

Pin Configuration appears at end of data sheet.

Functional Diagram



+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +7V
Digital Input Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Output Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
REF+ to GND .....-0.3V to (V_{DD} + 0.3V)
REF- to GND .....-0.3V to (V_{DD} + 0.3V)
IN_ to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
24 Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.08W
24 SSOP (derate 8.00mW/°C above +70°C).....640mW
24 Narrow CERDIP (derate 12.50mW/°C above +70°C) 1W
28 Wide Plastic DIP
(derate 14.29mW/°C above +70°C) 1.14W
28 SSOP (derate 9.52mW/°C above +70°C).....762mW
28 Wide CERDIP (derate 16.67mW/°C above +70°C)....1.33W
Operating Temperature Ranges
MAX113C_G/MAX117C_I .....0°C to +70°C
MAX113E_G/MAX117E_I .....-40°C to +85°C
MAX113MRG/MAX117MJI .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V to +3.6V, REF+ = 3V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	N		8			Bits
Total Unadjusted Error	TUE				±1	LSB
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±1	LSB
Zero-Code Error					±1	LSB
Full-Scale Error					±1	LSB
Channel-to-Channel Mismatch					±1/4	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Plus Distortion Ratio	SINAD	MAX11_C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz	45			dB
		MAX11_M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	45			
Total Harmonic Distortion	THD	MAX11_C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz			-50	dB
		MAX11_M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz			-50	
Spurious-Free Dynamic Range	SFDR	MAX11_C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz	50			dB
		MAX11_M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	50			
Input Full-Power Bandwidth		$V_{IN\_}$ = 3Vp-p		0.3		MHz
Input Slew Rate, Tracking			0.28	0.5		V/µs
ANALOG INPUT						
Input Voltage Range	$V_{IN\_}$		V_{REF-}		V_{REF+}	V
Input Leakage Current	$I_{IN\_}$	GND < $V_{IN\_}$ < V_{DD}			±3	µA
Input Capacitance	$C_{IN\_}$			32		pF
REFERENCE INPUT						
Reference Resistance	R_{REF}		1	2	4	kΩ
REF+ Input Voltage Range			V_{REF-}		V_{DD}	V
REF- Input Voltage Range			GND		V_{REF+}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V to +3.6V, REF+ = 3V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2		2			V
		MODE		2.4			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				0.66	V
		MODE				0.8	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$, A0, A1, A2				±1	µA
		$\overline{WR}$				±3	
		MODE			15	100	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE, A0, A1, A2				±1	µA
Input Capacitance (Note 2)	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE, A0, A1, A2			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{SINK} = 20µA, $\overline{INT}$, D0–D7				0.1	V
		I_{SINK} = 400µA, $\overline{INT}$, D0–D7				0.4	
		RDY, I_{SINK} = 1mA				0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 20µA, $\overline{INT}$, D0–D7		V_{DD} - 0.1			V
		I_{SOURCE} = 400µA, $\overline{INT}$, D0–D7		V_{DD} - 0.4			
Three-State Current	I_{LKG}	D0–D7, RDY, digital outputs = 0V to V_{DD}				±3	µA
Three-State Capacitance (Note 2)	C_{OUT}	D0–D7, RDY			5	8	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			3.0		3.6	V
V_{DD} Supply Current	I_{DD}	V_{DD} = 3.6V, $\overline{CS}$ = $\overline{RD}$ = 0V, $\overline{PWRDN}$ = V_{DD}	MAX11_C		2.5	5	mA
			MAX11_E/M		2.5	6	
		V_{DD} = 3.0V, $\overline{CS}$ = $\overline{RD}$ = 0V, $\overline{PWRDN}$ = V_{DD}	MAX11_C		1.5	3	
			MAX11_E/M		1.5	3.5	
Power-Down V_{DD} Current		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, $\overline{PWRDN}$ = 0V (Note 3)			1	10	µA
Power-Supply Rejection	PSR	V_{DD} = 3.0V to 3.6V, V_{REF} = 3.0V			±1/16	±1/4	LSB

Note 1: Accuracy measurements performed at V_{DD} = +3.0V. Operation over supply range is guaranteed by power-supply rejection test.
Note 2: Guaranteed by design.
Note 3: Power-down current increases if logic inputs are not driven to GND or V_{DD}.

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

TIMING CHARACTERISTICS

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C ALL GRADES			T_A = T_{MIN} to T_{MAX}				UNITS
						MAX117C/E		MAX117M		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Conversion Time (WR-RD Mode)	t_{CWR}	t_{RD} < t_{INTL}, C_L = 100pF (Note 5)			1.8		2.06		2.4	µs
Conversion Time (RD Mode)	t_{CRD}				2.0		2.4		2.6	µs
Power-Up Time	t_{UP}				0.9		1.2		1.4	µs
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R_L = 5.1kΩ to V_{DD}			100		120		140	ns
Data Access Time (RD Mode)	t_{ACC0}	C_L = 100pF (Note 5)			t_{CRD} + 100		t_{CRD} + 130		t_{CRD} + 150	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		100	160		170		180	ns
Data Hold Time	t_{DH}	(Note 6)			100		130		150	ns
Minimum Acquisition Time	t_{ACQ}	(Note 7)	450			600		700		ns
$\overline{WR}$ Pulse Width	t_{WR}		0.6		10	0.66	10	0.8	10	µs
Delay Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		0.8			0.9		1.0		µs
$\overline{RD}$ Pulse Width (WR-RD Mode)	t_{READ1}	t_{RD} < t_{INTL}, determined by t_{ACC1}	400			500		600		ns
Data Access Time (WR-RD Mode)	t_{ACC1}	t_{RD} < t_{INTL}, C_L = 100pF (Note 5)			400		500		600	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}				300		340		400	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF		0.7	1.45		1.6		1.8	µs
$\overline{RD}$ Pulse Width (WR-RD Mode)	t_{READ2}	t_{RD} > t_{INTL}, determined by t_{ACC2}	180			220		250		ns
Data Access Time (WR-RD Mode)	t_{ACC2}	t_{RD} > t_{INTL}, C_L = 100pF (Note 5)			180		220		250	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{IHWR}	Pipelined mode, C_L = 50pF			180		200		240	ns
Data Access Time After $\overline{INT}$	t_{ID}	Pipelined mode, C_L = 100pF			100		130		150	ns
Multiplexer Address Hold Time	t_{AH}		50			60		70		ns

Note 4: Input control signals are specified with t_r = t_f = 5ns, 10% to 90% of 3V, and timed from a voltage level of 1.3V. Timing delays get shorter at higher supply voltages. See the Conversion Time vs. Supply Voltage graph in the *Typical Operating Characteristics* to extrapolate timing delays at other power-supply voltages.

Note 5: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.66V or 2.0V.

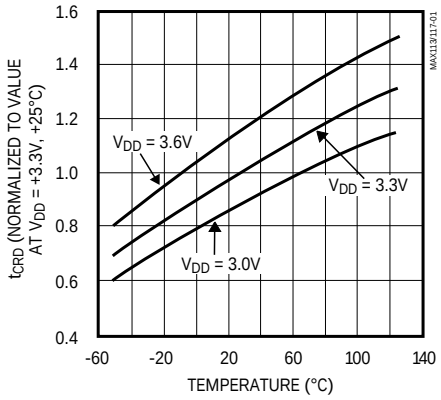
Note 6: See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.

Note 7: Also defined as the Minimum Address-Valid to Convert-Start Time.

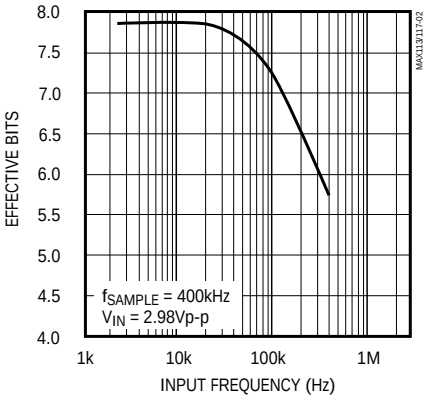
Typical Operating Characteristics

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

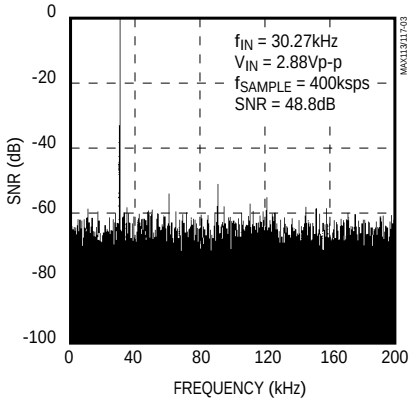
CONVERSION TIME vs. AMBIENT TEMPERATURE



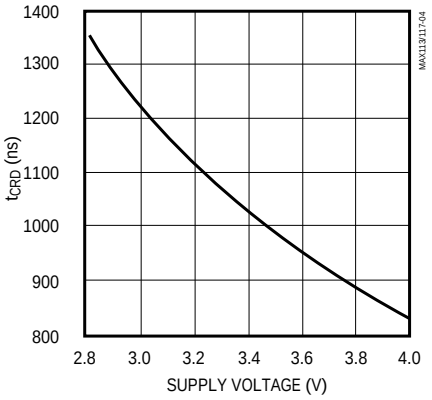
EFFECTIVE BITS vs. INPUT FREQUENCY (WR-RD MODE)



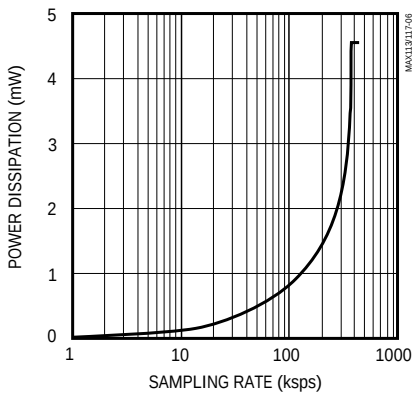
SIGNAL-TO-NOISE RATIO



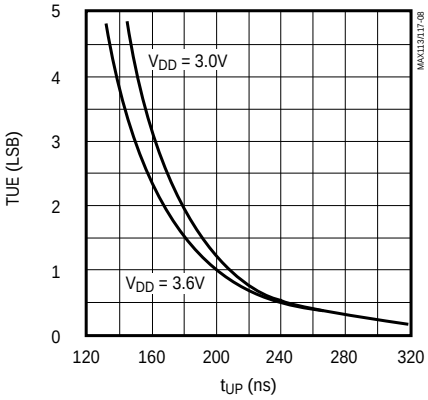
CONVERSION TIME vs. SUPPLY VOLTAGE



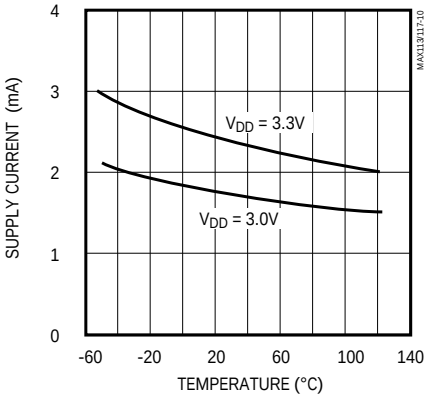
AVERAGE POWER CONSUMPTION vs. SAMPLING RATE USING PWRDN



TOTAL UNADJUSTED ERROR vs. POWER-UP TIME



SUPPLY CURRENT vs. TEMPERATURE (EXCLUDING REFERENCE CURRENT)



+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

Pin Description

PIN		NAME	FUNCTION
MAX113	MAX117		
—	1	IN6	Analog Input Channel 6
—	2	IN5	Analog Input Channel 5
1	3	IN4	Analog Input Channel 4
2	4	IN3	Analog Input Channel 3
3	5	IN2	Analog Input Channel 2
4	6	IN1	Analog Input Channel 1
5	7	MODE	Mode Selection Input. Internally pulled low with a 15µA current source. MODE = 0 activates read mode; MODE = 1 activates write-read mode (see *Digital Interface* section).
6	8	D0	Three-State Data Output (LSB)
7, 8, 9	9, 10, 11	D1, D2, D3	Three-State Data Outputs
10	12	$\overline{RD}$	Read Input. $\overline{RD}$ must be low to access data (see *Digital Interface* section).
11	13	$\overline{INT}$	Interrupt Output. $\overline{INT}$ goes low to indicate end of conversion (see *Digital Interface* section).
12	14	GND	Ground
13	15	REF-	Lower limit of reference span. REF- sets the zero-code voltage. Range is GND ≤ V_{REF-} < V_{REF+}.
14	16	REF+	Upper limit of reference span. REF+ sets the full-scale input voltage. Range is V_{REF-} < V_{REF+} ≤ V_{DD}. Internally hardwired to IN8 (Table 1).
15	17	$\overline{WR}$/RDY	Write-Control Input/Ready-Status Output (see *Digital Interface* section)
16	18	$\overline{CS}$	Chip-Select Input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs.
17, 18, 19	19, 20, 21	D4, D5, D6	Three-State Data Outputs
20	22	D7	Three-State Data Output (MSB)
—	23	A2	Multiplexer Channel Address Input (MSB)
21	24	A1	Multiplexer Channel Address Input
22	25	A0	Multiplexer Channel Address Input (LSB)
23	26	$\overline{PWRDN}$	Power-Down Input. $\overline{PWRDN}$ reduces supply current when low.
24	27	V_{DD}	Positive Supply, +3.0V to +3.6V
—	28	IN7	Analog Input Channel 7

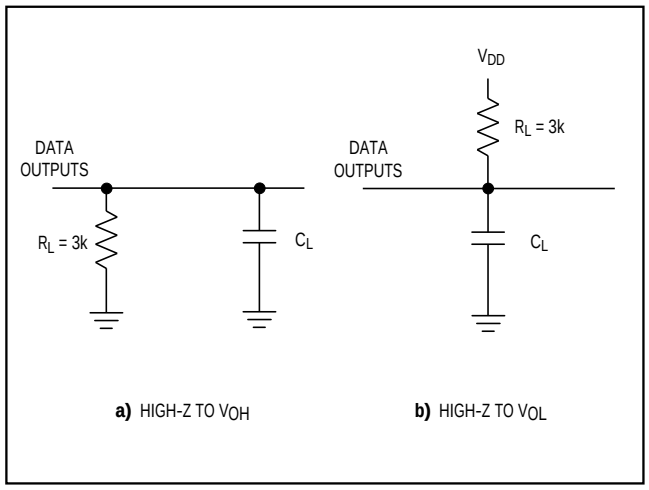


Figure 1. Load Circuits for Data-Access Time Test

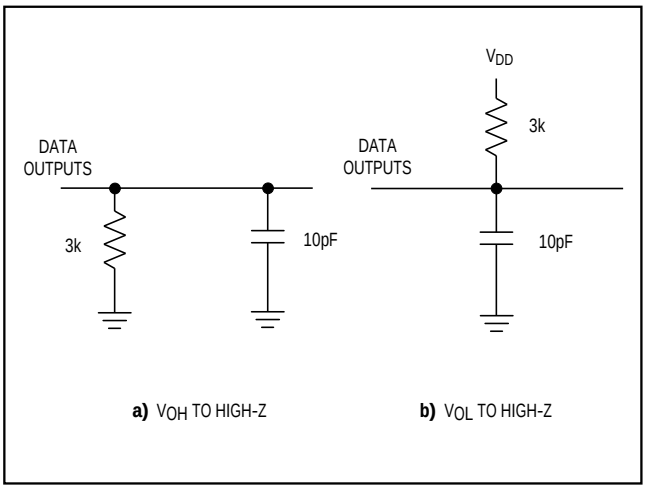


Figure 2. Load Circuits for Data-Hold Time Test

Detailed Description

Converter Operation

The MAX113/MAX117 use a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper four data bits. An internal digital-to-analog converter (DAC) uses the four most significant bits (MSBs) to generate both the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower four data bits (LSBs).

An internal analog multiplexer enables the devices to read four (MAX113) or eight (MAX117) different analog voltages under microprocessor (µP) control. One of the MAX117's analog channels, IN8, is internally hardwired and always reads V_{REF+} when selected.

Power-Down Mode

In burst-mode or low-sample-rate applications, the MAX113/MAX117 can be shut down between conversions, reducing supply current to microamp levels (see *Typical Operating Characteristics*). A logic low on the $\overline{PWRDN}$ pin shuts the devices down, reducing supply current typically to 1µA when powered from a single +3V supply. A logic high on $\overline{PWRDN}$ wakes up the MAX113/MAX117, and the selected analog input enters the track mode. The signal is fully acquired after 900ns (this includes both the power-up delay and the track/hold acquisition time), and a new conversion can be started. If the power-down feature is not required, connect $\overline{PWRDN}$ to V_{DD}. For minimum current consumption, keep digital inputs at the supply rails in power-down mode. Refer to the *Reference* section for information on reducing the reference current during power-down.

Digital Interface

The MAX113/MAX117 have two basic interface modes, which are set by the MODE pin. When MODE is low, the converters are in read mode; when MODE is high, the converters are set up for write-read mode. The A0, A1, and A2 inputs control channel selection, as shown in Table 1. The address must be valid for a minimum time, t_{ACQ}, before the next conversion starts.

Table 1. Truth Table for Input Channel Selection

MAX113		MAX117			SELECTED CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	IN1
0	1	0	0	1	IN2
1	0	0	1	0	IN3
1	1	0	1	1	IN4
—	—	1	0	0	IN5
—	—	1	0	1	IN6
—	—	1	1	0	IN7
—	—	1	1	1	IN8 (reads V_{REF+} if selected)

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

Read Mode (MODE = 0)

In read mode, conversions and data access are controlled by the $\overline{RD}$ input (Figure 3). The comparator inputs track the analog input voltage for the duration of t_{ACQ}. A conversion is initiated by driving $\overline{CS}$ and $\overline{RD}$ low. With µPs that can be forced into a wait state, hold $\overline{RD}$ low until output data appears. The µP starts the conversion, waits, and then reads data with a single read instruction.

In read mode, $\overline{WR}$/RDY is configured as a status output (RDY), so it can drive the ready or wait input of a µP. RDY is an open-collector output (no internal pull-up) that goes low after the falling edge of $\overline{CS}$ and goes high at the end of the conversion. If not used, the $\overline{WR}$/RDY pin can be left unconnected. The $\overline{INT}$ output goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Write-Read Mode (MODE = 1)

Figures 4 and 5 show the operating sequence for write-read mode. The comparator inputs track the analog input voltage for the duration of t_{ACQ}. The conversion is initiated by a falling edge of $\overline{WR}$. When $\overline{WR}$ returns high, the result of the four-MSBs flash is latched into the output buffers and the conversion of the four-LSBs flash starts. $\overline{INT}$ goes low, indicating conversion end, and the lower four data bits are latched into the output buffers. The data is then accessible after $\overline{RD}$ goes low (see *Timing Characteristics*).

A minimum acquisition time (t_{ACQ}) is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Options for reading data from the converter include using internal delay, reading before delay, and pipelined operation (discussed in the following sections).

Using Internal Delay

The µP waits for the $\overline{INT}$ output to go low before reading the data (Figure 4). $\overline{INT}$ goes low after the rising edge of $\overline{WR}$, indicating that the conversion is complete and the result is available in the output latch. With $\overline{CS}$ low, data outputs D0–D7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

Fastest Conversion: Reading Before Delay

An external method of controlling the conversion time is shown in Figure 5. The internally generated delay (t_{INTL}) varies slightly with temperature and supply voltage, and can be overridden with $\overline{RD}$ to achieve the fastest conversion time. $\overline{RD}$ is brought low after the rising edge of $\overline{WR}$, but before $\overline{INT}$ goes low. This completes the conversion and enables the output buffers

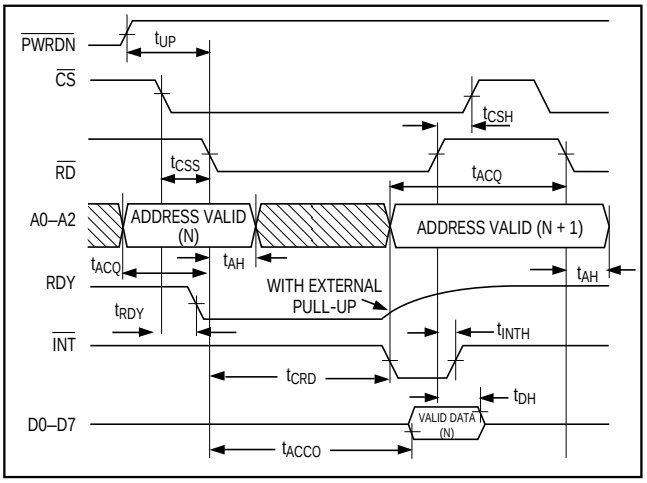


Figure 3. Read Mode Timing (Mode = 0)

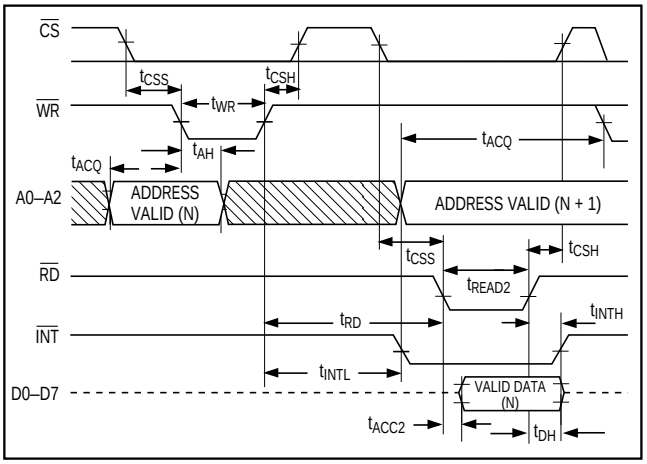


Figure 4. Write-Read Mode Timing ($t_{RD} > t_{INTL}$) (Mode = 1)

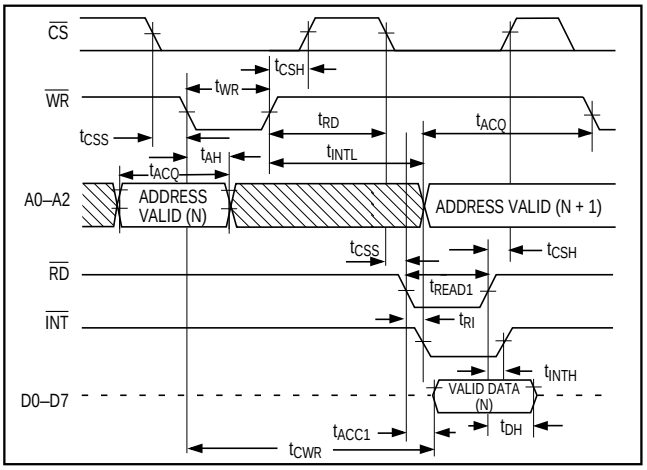


Figure 5. Write-Read Mode Timing ($t_{RD} < t_{INTL}$) (Mode = 1)

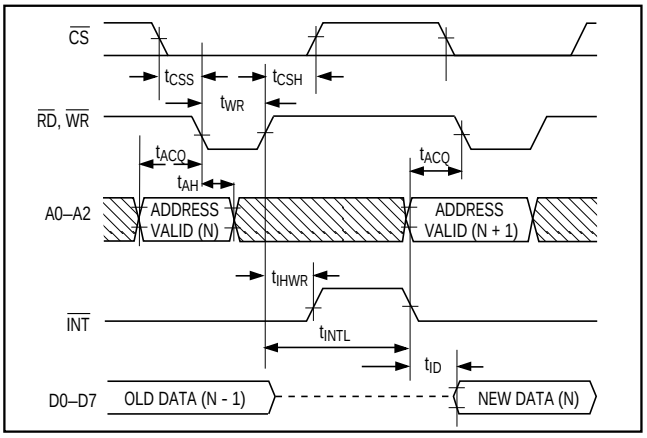


Figure 6. Pipelined Mode Timing ($\overline{WR}$ = $\overline{RD}$) (Mode = 1)

that contain the conversion result (D0–D7). $\overline{INT}$ also goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The total conversion time is therefore: $t_{WR} + t_{RD} + t_{ACC1}$ = 1800ns.

Pipelined Operation

Besides the two standard write-read-mode options, "pipelined" operation can be achieved by connecting $\overline{WR}$ and $\overline{RD}$ together (Figure 6). With $\overline{CS}$ low, driving $\overline{WR}$ and $\overline{RD}$ low initiates a conversion and concurrently reads the result of the previous conversion.

Analog Considerations

Reference

Figures 7a, 7b, and 7c show typical reference connections. The voltages at REF+ and REF- set the ADC's analog input range (Figure 10). The voltage at REF- defines the input that produces an output code of all zeros, and the voltage at REF+ defines the input that produces an output code of all ones.

The internal resistance from REF+ to REF- can be as low as 1kΩ, and current will flow through it even when the MAX113/MAX117 are shut down. Figure 7d shows how an N-channel MOSFET can be connected to REF- to break this current path during power-down. The FET should have an on-resistance of less than 2Ω with a 3V gate drive. When REF- is switched, as in Figure 7d, a new conversion can be initiated after waiting a time equal to the power-up delay (t_{UP}) plus the N-channel FET's turn-on time.

Although REF+ is frequently connected to V_{DD}, the circuit of Figure 7d uses a low-current, low-dropout, 2.5V voltage reference: the MAX872. Since the MAX872 cannot continuously furnish enough current for the reference resistance, this circuit is intended for applications where the MAX113/MAX117 are normally in standby and are turned on in order to make measurements at intervals greater than 100µs. C1 (the capacitor connected to REF+) is slowly charged by the MAX872 during the standby period, and furnishes the reference current during the short measurement period.

The 4.7µF value of C1 ensures a voltage drop of less than 1/2LSB when performing four to eight successive conversions. Larger capacitors reduce the error still further. Use ceramic or tantalum capacitors for C1.

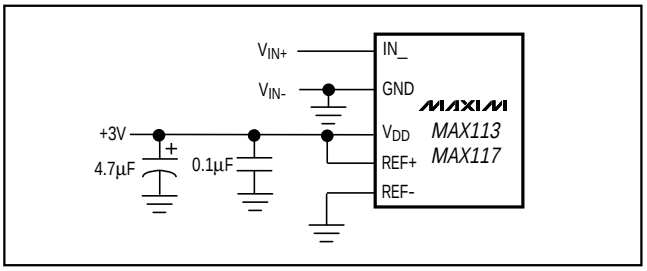


Figure 7a. Power Supply as Reference

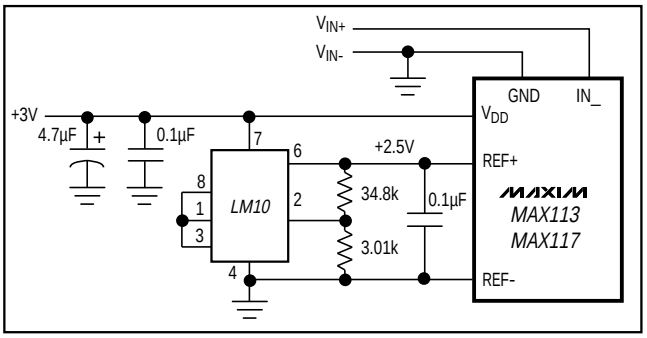


Figure 7b. External Reference, 2.5V Full Scale

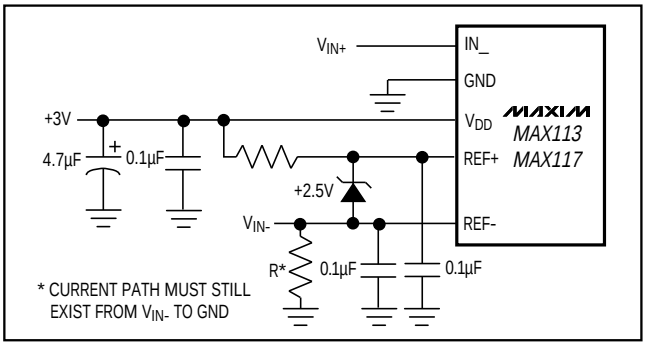


Figure 7c. Input Not Referenced to GND

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

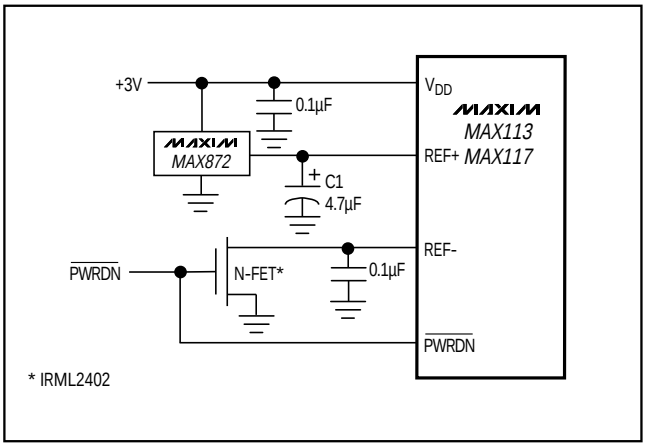


Figure 7d. An N-channel MOSFET switches off the reference load during power-down

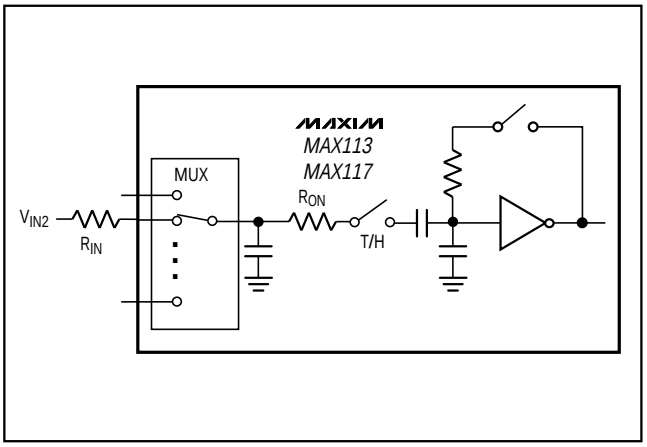


Figure 8. Equivalent Input Circuit

Initial Power-Up

When power is first applied, perform a conversion to initialize the MAX113/MAX117. Disregard the output data.

Bypassing

Use a 4.7µF electrolytic in parallel with a 0.1µF ceramic capacitor to bypass V_{DD} to GND. Minimize capacitor lead lengths.

Bypass the reference inputs with 0.1µF capacitors, as shown in Figures 7a, 7b, and 7c.

Analog Inputs

Figure 8 shows the equivalent circuit of the MAX113/MAX117 input. When a conversion starts and $\overline{WR}$ is low, $V_{IN\_}$ is connected to sixteen 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches. In addition, about 22pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 32pF input capacitance allows source resistance as high as 1.5kΩ without setup problems. For larger resistances, the acquisition time (t_{ACQ}) must be increased.

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the channel input pins to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale and zero scale the inputs must not exceed V_{DD} by more than 50mV or be lower than GND by 50mV.

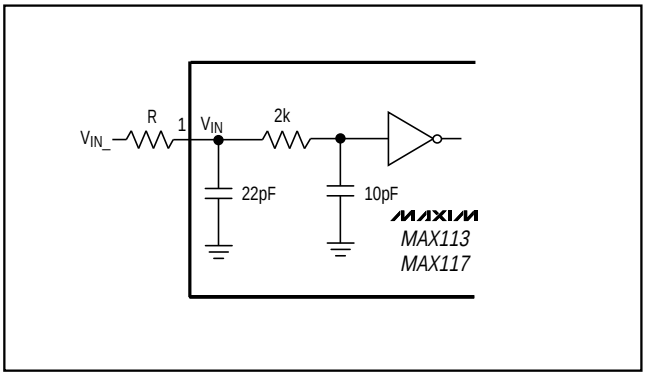


Figure 9. RC Network Equivalent Input Model

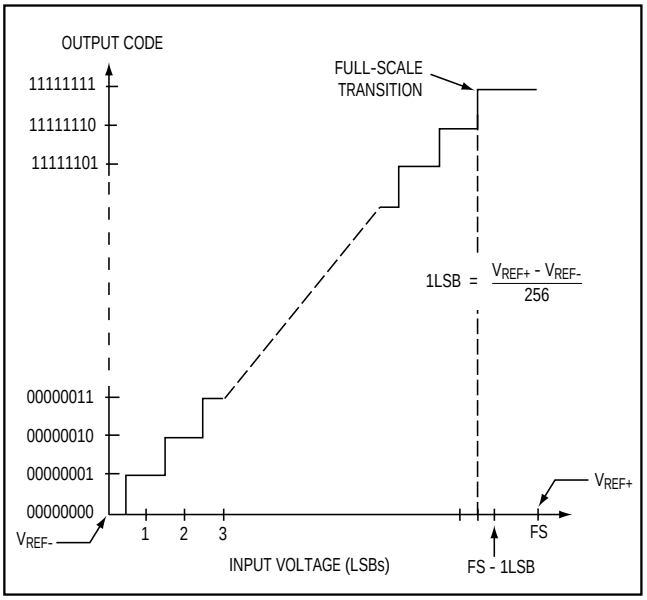


Figure 10. Transfer Function

If the analog input exceeds 50mV beyond the supplies, limit the input current to no more than two milliamperes, as excessive current will degrade the conversion accuracy of the on channel.

Track/Hold

The track/hold enters hold mode when a conversion starts ($\overline{RD}$ low or $\overline{WR}$ low). INT goes low at the end of the conversion, at which point the track/hold enters track mode. The next conversion can start after the minimum acquisition time, t_{ACQ}.

Transfer Function

Figure 10 shows the MAX113/MAX117's nominal transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary with 1LSB = (V_{REF+} - V_{REF-}) / 256.

Conversion Rate

The maximum sampling rate (f_{MAX}) for the MAX113/MAX117 is achieved in write-read mode ($t_{RD} < t_{INTL}$) and is calculated as follows:

$$f_{MAX} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_{ACQ}}$$

$$f_{MAX} = \frac{1}{600ns + 800ns + 300ns + 450ns}$$

$$f_{MAX} = 465kHz$$

where t_{WR} = the write pulse width, t_{RD} = the delay between write and read pulses, t_{RI} = $\overline{RD}$ to $\overline{INT}$ delay, and t_{ACQ} = minimum acquisition time.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT Plot (see *Typical Operating Characteristics*) shows the result of sampling a pure 30.27kHz sinusoid at a 400kHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution (or "effective number of bits") the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SINAD - 1.76) / 6.02 (see *Typical Operating Characteristics*).

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20\log\left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ...V_N^2}}{V_1}\right]$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor. See the Signal-to-Noise Ratio graph in *Typical Operating Characteristics*.

+3V, 400ksps, 4/8-Channel, 8-Bit ADCs with 1µA Power-Down

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX117CPI	0°C to +70°C	28 Wide Plastic DIP
MAX117CAI	0°C to +70°C	28 SSOP
MAX117C/D	0°C to +70°C	Dice*
MAX117EPI	-40°C to +85°C	28 Wide Plastic DIP
MAX117EAI	-40°C to +85°C	28 SSOP
MAX117MJI	-55°C to +125°C	28 Wide CERDIP**

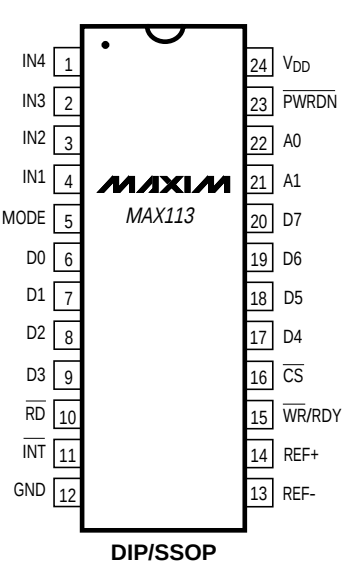
*Dice are specified at T_A = +25°C, DC parameters only.
**Contact factory for availability.

Chip Information

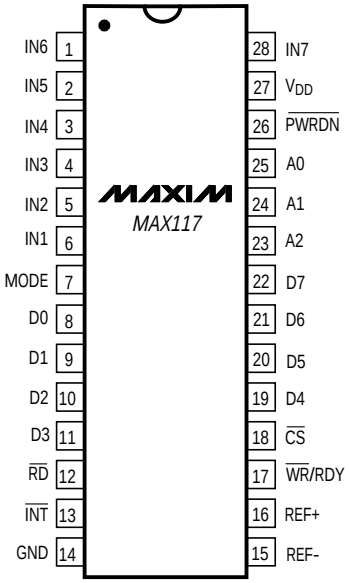
TRANSISTOR COUNT: 2011

Pin Configurations

TOP VIEW



DIP/SSOP



DIP/SSOP