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Data Sheet | March 31, 2005 | FN3214.6

CMOS 20 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold

The HI5812 is a fast, low power, 12-bit, successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 1.9mA when operating at 5V. The HI5812 features a built-in track and hold. The conversion time is as low as 20µs with a 5V supply.

The twelve data outputs feature full high speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable, i.e., 12-bit, 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag, and conversion-start input complete the digital interface.

An internal clock is provided and is available as an output. The clock may also be over-driven by an external source.

Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
HI5812JIP	±1.5	-40 to 85	24 Ld PDIP	E24.3
HI5812JIPZ (See Note)	±1.5	-40 to 85	24 Ld PDIP* (Pb-free)	E24.3
HI5812JIB	±1.5	-40 to 85	24 Ld SOIC	M24.3
HI5812JIBZ (See Note)	±1.5	-40 to 85	24 Ld SOIC (Pb-free)	M24.3
HI5812KIB	±1.0	-40 to 85	24 Ld SOIC	M24.3
HI5812KIBZ (See Note)	±1.0	-40 to 85	24 Ld SOIC (Pb-free)	M24.3

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

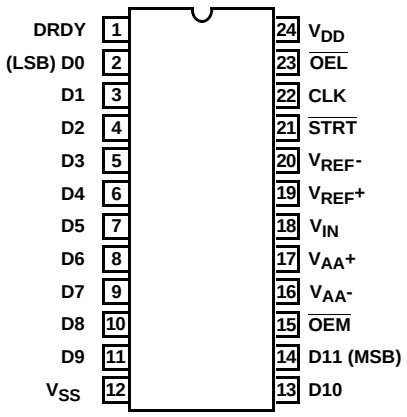
- Conversion Time 20µs
- Throughput Rate . . . . . 50 kSPS
- Built-In Track and Hold
- Guaranteed No Missing Codes Over Temperature
- Single Supply Voltage . . . . . +5V
- Maximum Power Consumption 25mW
- Internal or External Clock
- Pb-Free Available (RoHS Compliant)

Applications

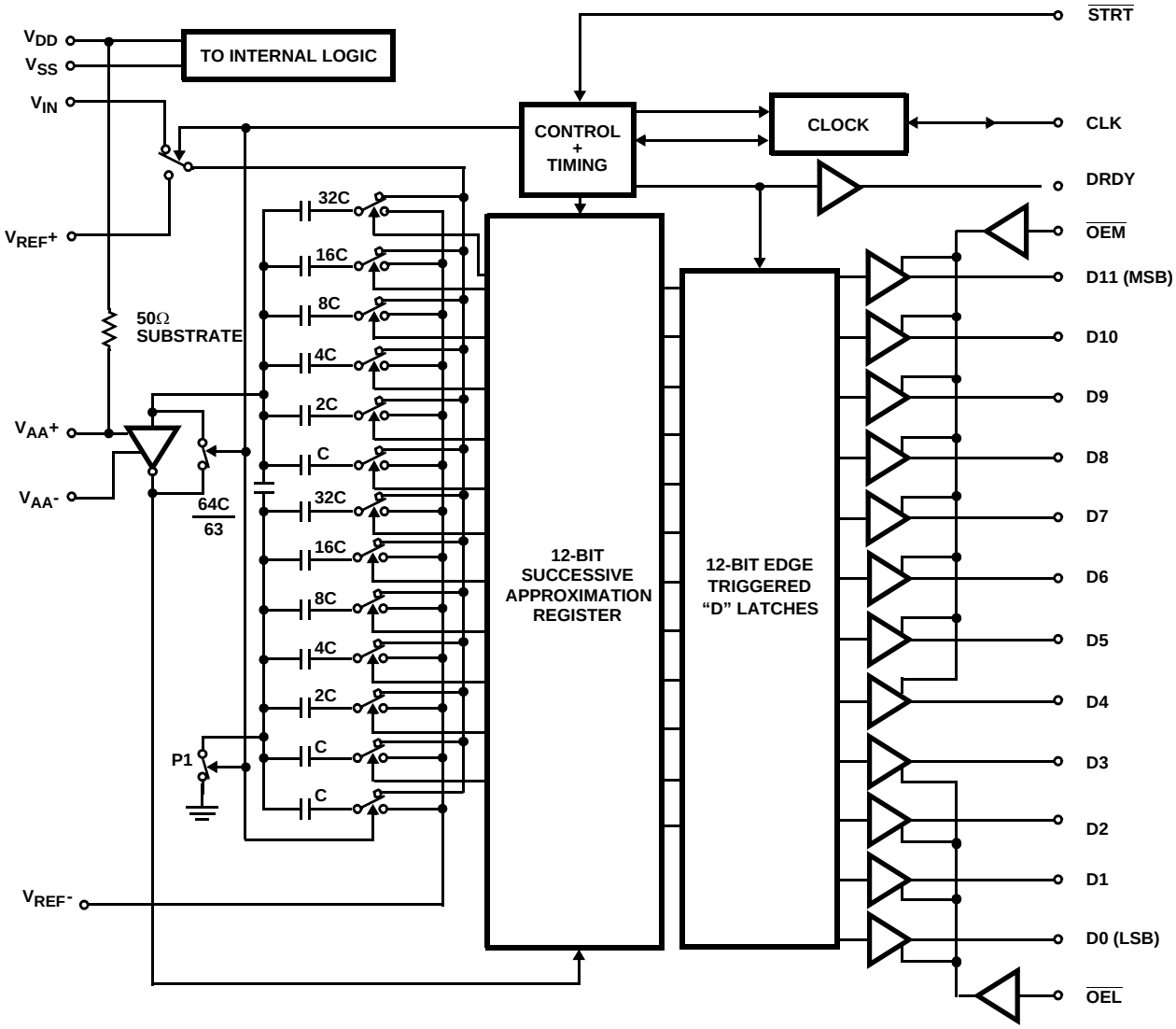
- Remote Low Power Data Acquisition Systems
- Digital Audio
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement System
- Professional Audio Positioner/Fader

Pinout

HI5812
(PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} . . . . . (V_{SS} -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- . . . . . (V_{SS} -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} . . . . . ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF}+, V_{REF}- . . . . . (V_{SS} -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins . . . . . (V_{SS} -0.3V) < $V_{I/O}$ < (V_{DD} +0.3V)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PDIP Package*	70
SOIC Package	75

Maximum Junction Temperature
- Plastic Packages . . . . . 150°C

Maximum Storage Temperature Range . . . . . -65°C to 150°C

Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_{DD} = V_{AA}+ = 5V, V_{REF}+ = +4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 750kHz, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	25°C			-40°C TO 85°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±1.5	-	±1.5	LSB
	K		-	-	±1.0	-	±1.0	LSB
Differential Linearity Error, DNL	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±1.0	-	±1.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±3.0	-	±3.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
Offset Error, V_{OS} (Adjustable to Zero)	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±1.0	-	±1.0	LSB
Power Supply Rejection, PSRR		V_{REF} = 4V	-			-		
Offset Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		±0.1	±0.5		±0.5	LSB
Gain Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		±0.1	±0.5		±0.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD = RMS Signal / RMS Noise + Distortion	J	f_S = Internal Clock, f_{IN} = 1kHz	-	68.8	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		69.2				dB
	K	f_S = Internal Clock, f_{IN} = 1kHz	-	71.0	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		71.5				dB
Signal to Noise Ratio, SNR = RMS Signal / RMS Noise	J	f_S = Internal Clock, f_{IN} = 1kHz	-	70.5	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		71.1				dB
	K	f_S = Internal Clock, f_{IN} = 1kHz	-	71.5	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		72.1				dB
Total Harmonic Distortion, THD	J	f_S = Internal Clock, f_{IN} = 1kHz	-	-73.9	-	-	-	dBc
		f_S = 750kHz, f_{IN} = 1kHz		-73.8				dBc
	K	f_S = Internal Clock, f_{IN} = 1kHz	-	-80.3	-	-	-	dBc
		f_S = 750kHz, f_{IN} = 1kHz		-79.0				dBc

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 750kHz, Unless Otherwise Specified **(Continued)**

PARAMETER		TEST CONDITIONS	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	UNITS
Spurious Free Dynamic Range, SFDR	J	f_S =Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-75.4 -75.1	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-80.9 -79.6	-	-	-	dB dB
ANALOG INPUT								
Input Current, Dynamic		At $V_{IN} = V_{REF}+$, 0V	-	±50	±100	-	±100	µA
Input Current, Static		Conversion Stopped	-	±0.4	±10	-	±10	µA
Input Bandwidth -3dB			-	1	-	-	-	MHz
Reference Input Current			-	160	-	-	-	µA
Input Series Resistance, R_S		In Series with Input C_{SAMPLE}	-	420	-	-	-	W
Input Capacitance, C_{SAMPLE}		During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}		During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$								
High-Level Input Voltage, V_{IH}			2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}			-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}		Except CLK, V_{IN} = 0V, 5V	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}			-	10	-	-	-	pF
DIGITAL OUTPUTS								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -400µA	4.6	-	-	4.6	-	V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Three-State Leakage, I_{OZ}		Except DRDY, V_{OUT} = 0V, 5V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}		Except DRDY	-	20	-	-	-	pF
CLOCK								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -100µA (Note 2)	4	-	-	4	-	V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 100µA (Note 2)	-	-	1	-	1	V
Input Current		CLK Only, V_{IN} = 0V, 5V	-	-	±5	-	±5	mA
TIMING								
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time)			20	-	-	20	-	µs
Clock Frequency		Internal Clock, (CLK = Open)	200	300	400	150	500	kHz
		External CLK (Note 2)	0.05	2	1.5	0.05	1.5	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}		External CLK (Note 2)	100	-	-	100	-	ns
Aperture Delay, t_DAPR		(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, t_{D1}DRDY		(Note 2)	-	105	150	-	180	ns
Clock to Data Ready Delay, t_{D2}DRDY		(Note 2)	-	100	160	-	195	ns
Start Removal Time, $t_R\overline{STRT}$		(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$		(Note 2)	85	60	-	100	-	ns
Start Pulse Width, $t_W\overline{STRT}$		(Note 2)	10	4	-	15	-	ns
Start to Data Ready Delay, t_{D3} DRDY		(Note 2)	-	65	105	-	120	ns

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 750kHz, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	25°C			-40°C TO 85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Clock Delay from Start, $t_D\overline{STRT}$	(Note 2)	-	60	-	-	-	ns
Output Enable Delay, t_{EN}	(Note 2)	-	20	30	-	50	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	80	95	-	120	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$		-	1.9	5	-	8	mA

NOTE:

2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams

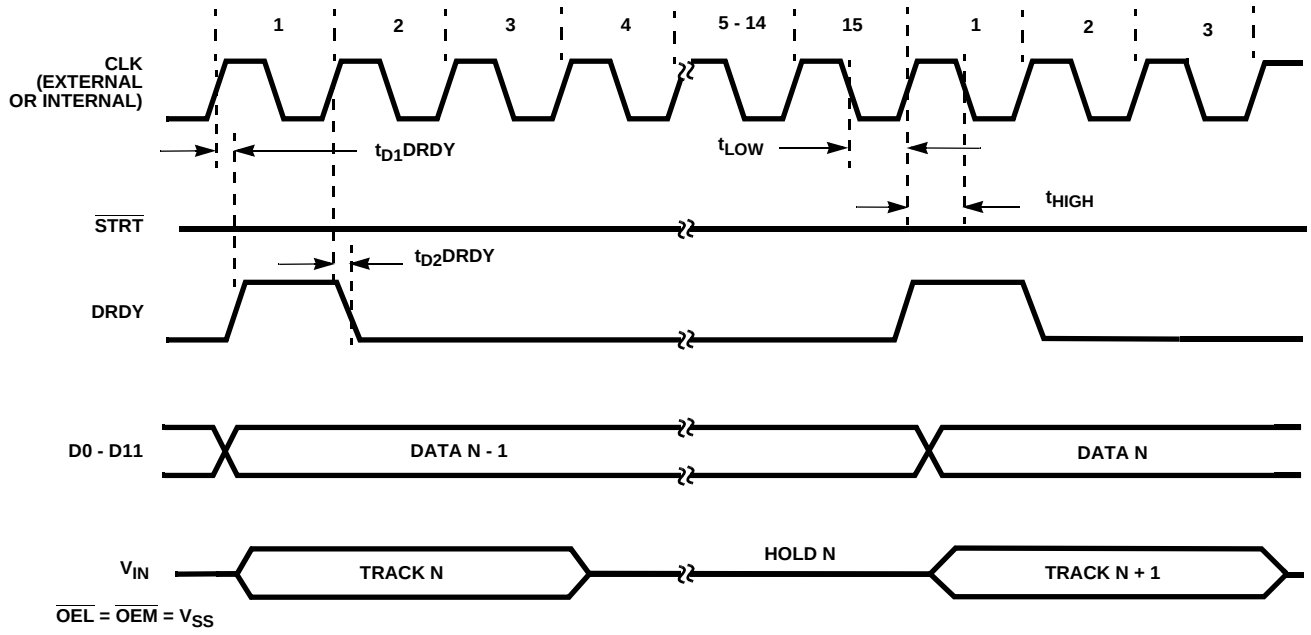


FIGURE 1. CONTINUOUS CONVERSION MODE

Timing Diagrams (Continued)

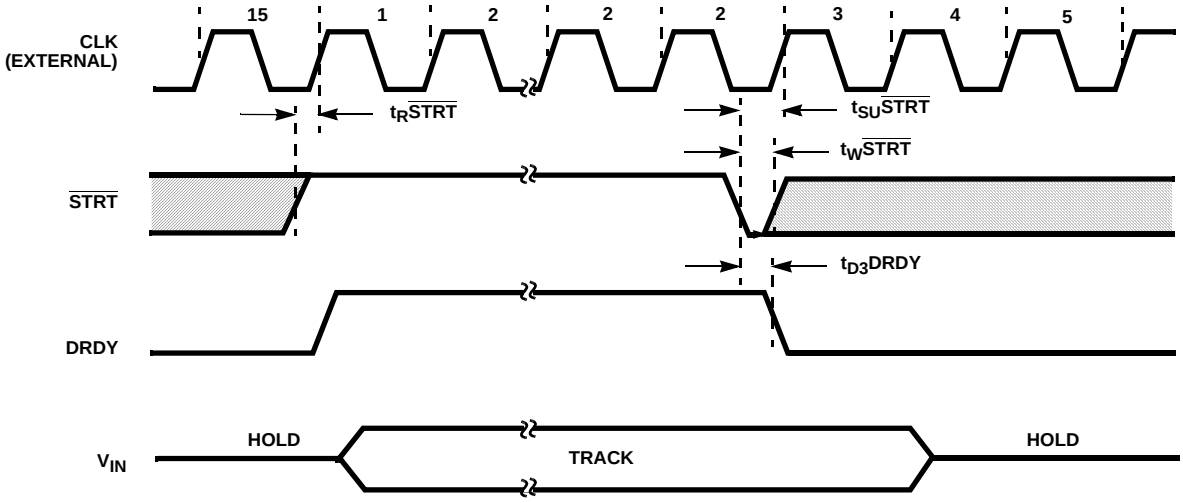


FIGURE 2. SINGLE SHOT MODE EXTERNAL CLOCK

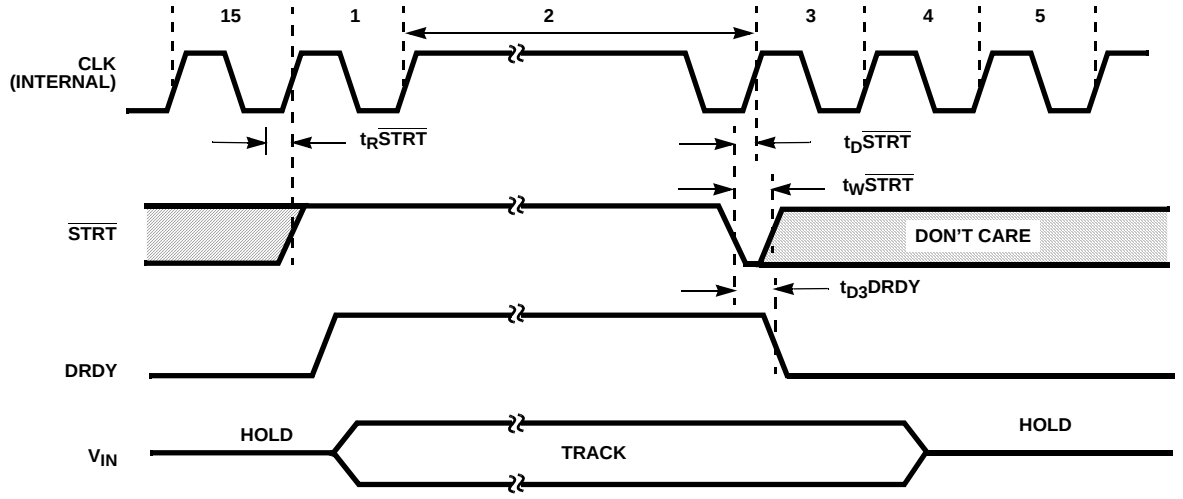


FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK

Timing Diagrams (Continued)

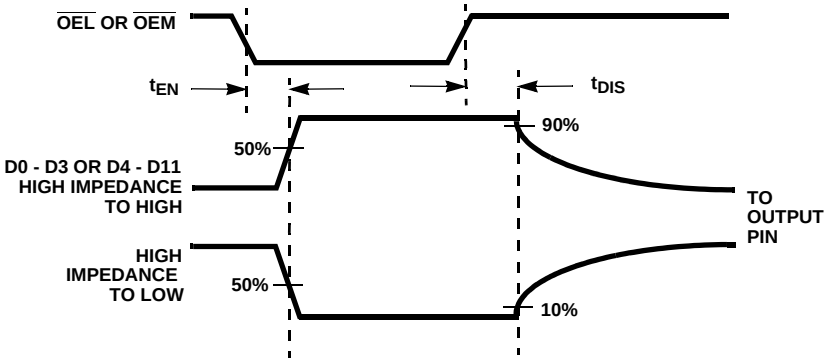


FIGURE 4A.

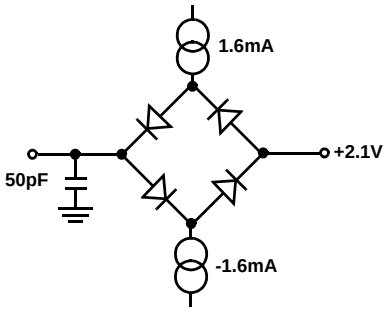


FIGURE 4B.

FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

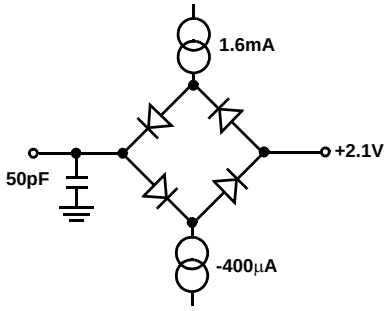


FIGURE 5. GENERAL TIMING LOAD CIRCUIT

Typical Performance Curves

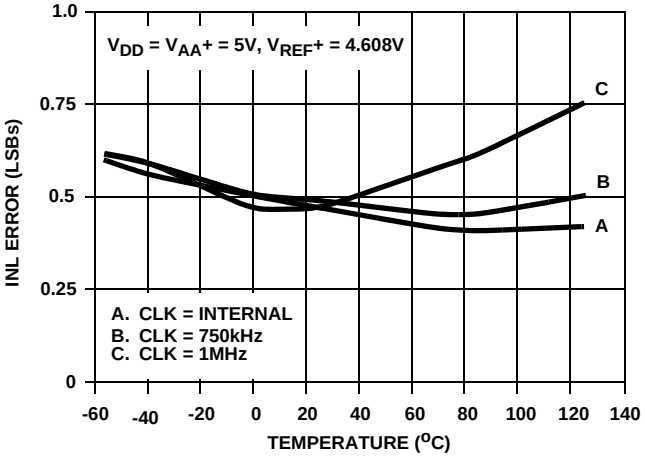


FIGURE 6. INL vs TEMPERATURE

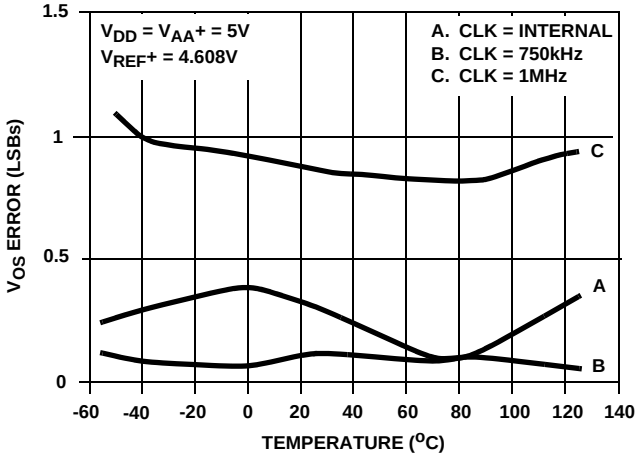


FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE

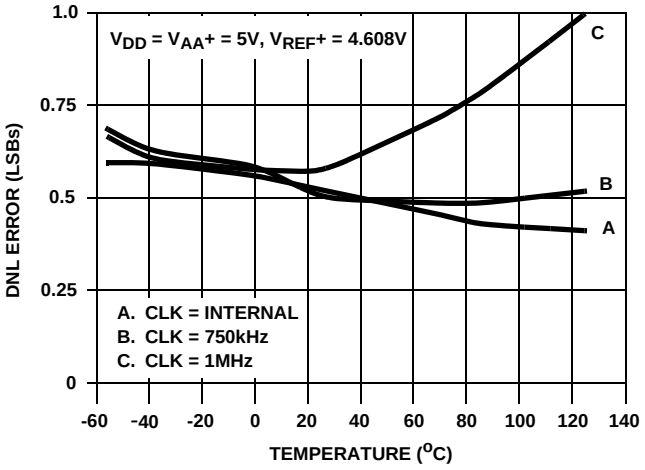


FIGURE 8. DNL vs TEMPERATURE

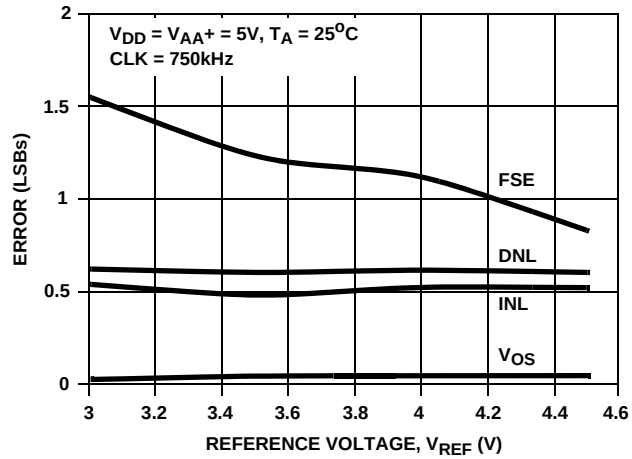


FIGURE 9. ACCURACY vs REFERENCE VOLTAGE

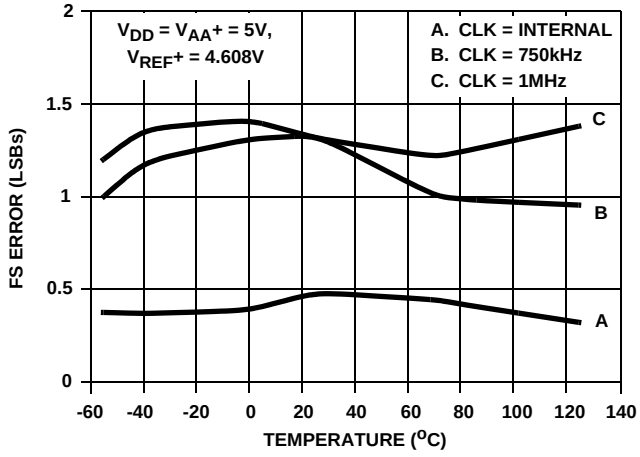


FIGURE 10. FULL SCALE ERROR vs TEMPERATURE

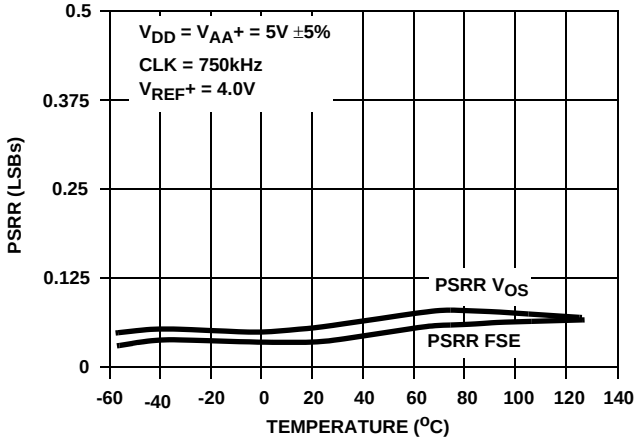


FIGURE 11. POWER SUPPLY REJECTION vs TEMPERATURE

Typical Performance Curves (Continued)

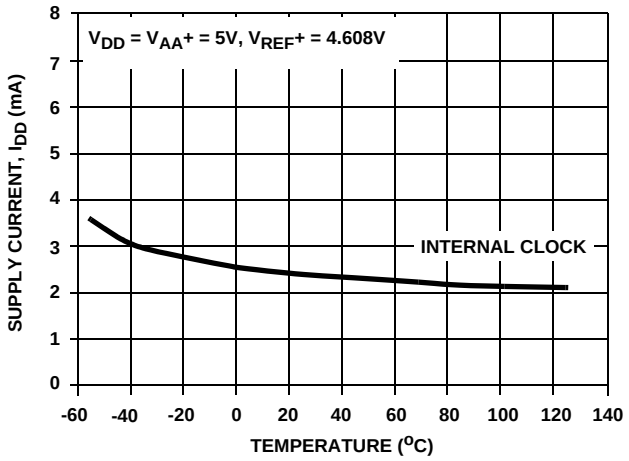


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

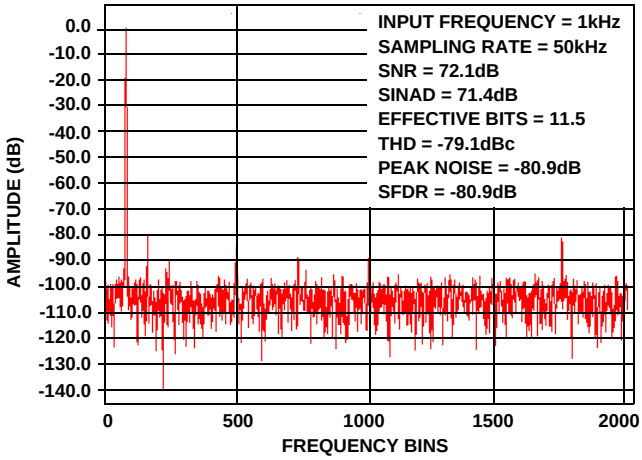


FIGURE 13. FFT SPECTRUM

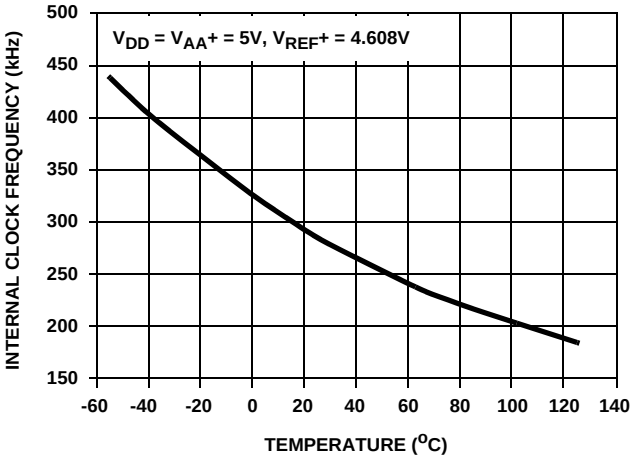


FIGURE 14. INTERNAL CLOCK FREQUENCY vs TEMPERATURE

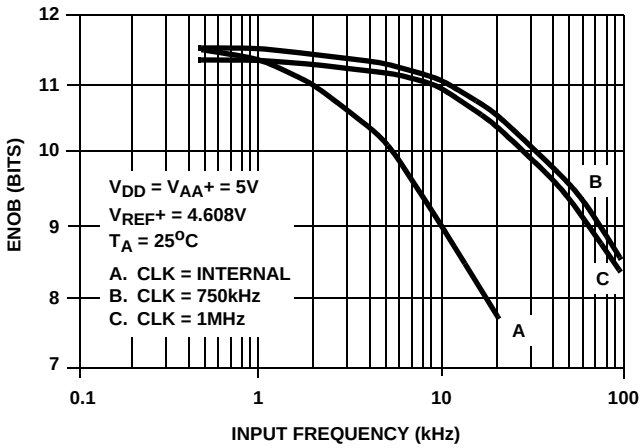


FIGURE 15. EFFECTIVE BITS vs INPUT FREQUENCY

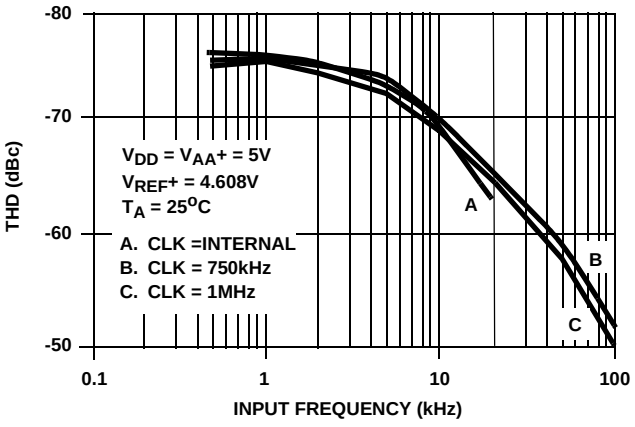


FIGURE 16. TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

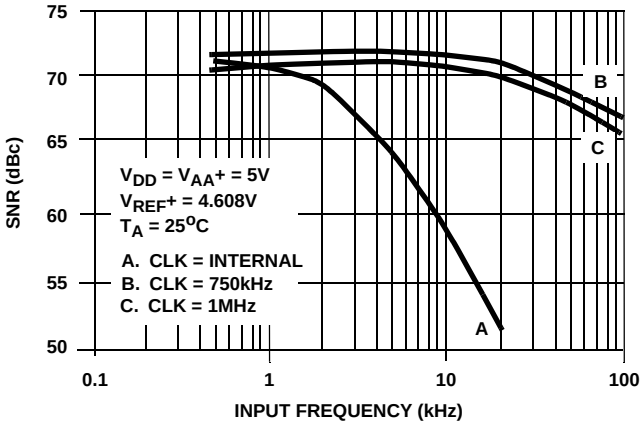


FIGURE 17. SIGNAL NOISE RATIO vs INPUT FREQUENCY

TABLE 1. PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit 0 (Least Significant Bit, LSB).
3	D1	Bit 1.
4	D2	Bit 2.
5	D3	Bit 3.
6	D4	Bit 4.
7	D5	Bit 5.
8	D6	Bit 6.
9	D7	Bit 7.
10	D8	Bit 8.
11	D9	Bit 9.
12	V_{SS}	Digital Ground (0V).
13	D10	Bit 10.
14	D11	Bit 11 (Most Significant Bit, MSB).
15	$\overline{OEM}$	Three-State Enable for D4-D11. Active low input.
16	V_{AA}-	Analog Ground, (0V).
17	V_{AA}+	Analog Positive Supply. (+5V) (See text.)
18	V_{IN}	Analog Input.
19	V_{REF}+	Reference Voltage Positive Input, sets 4095 code end of input range.
20	V_{REF}-	Reference Voltage Negative Input, sets 0 code end of input range.
21	$\overline{STRT}$	Start Conversion Input Active Low, recognized after end of clock period 15.
22	CLK	CLK Input or Output. Conversion functions are synchronized to positive going edge. (See text.)
23	$\overline{OEL}$	Three-State Enable for D0 D3. Active Low Input.
24	V_{DD}	Digital Positive Supply (+5V).

Theory of Operation

HI5812 is a CMOS 12-Bit Analog-to-Digital Converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5812.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}+ or V_{REF}-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto-balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the V_{REF}+ terminal; and the remaining capacitors to V_{REF}-. The capacitor-common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of (V_{REF}+ - V_{REF}-). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}+ (if the comparator was high) or returned to V_{REF}-. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of (V_{REF}+ - V_{REF}-).

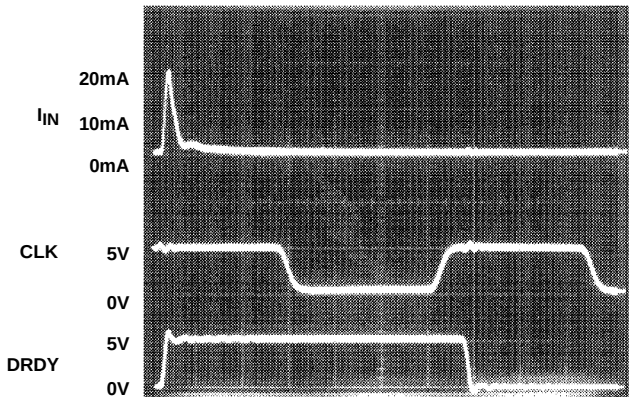
At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at V_{REF}+ or at V_{REF}-.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5μA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 18. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.



CONDITIONS: V_{DD} = V_{AA}+ = 5.0V, V_{REF}+ = 4.608V, V_{IN} = 4.608V, CLK = 750kHz, T_A = 25°C

FIGURE 18. TYPICAL ANALOG INPUT CURRENT

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With an external clock of 750kHz the track period is 4μs.

A simplified analog input model is presented in Figure 19. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4μs. The maximum source impedance (R_{SOURCE} Max) for a 4μs acquisition time settling to within 0.5LSB is 750Ω.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.

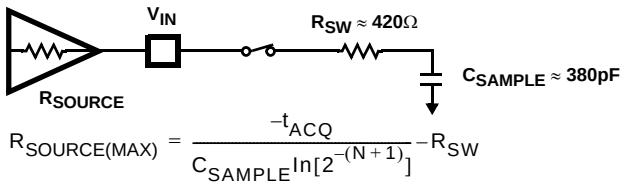
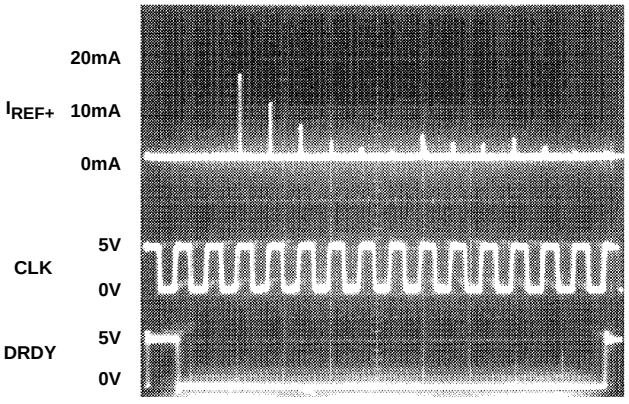


FIGURE 19. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

As shown in Figure 20, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge-balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.



CONDITIONS: $V_{DD} = V_{AA}+ = 5.0V$, $V_{REF}+ = 4.608V$, $V_{IN} = 2.3V$, CLK = 750kHz, $T_A = 25^oC$

FIGURE 20. TYPICAL REFERENCE INPUT CURRENT

The HI5812 is specified with a 4.608V reference, however, it will operate with a reference down to 3V having a slight degradation in performance. A typical graph of accuracy vs reference voltage is presented.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5812 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5812 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by t_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by t_{D1}DRDY) after the start of clock period 1, and returns low (specified by t_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on three-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). t_{EN} and t_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

When $\overline{STRT}$ input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the $\overline{STRT}$ signal is removed (at least $t_R\overline{STRT}$) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

A low signal applied to $\overline{STRT}$ (at least $t_W\overline{STRT}$ wide) can now initiate a new conversion. The $\overline{STRT}$ signal (after a delay of ($t_D\overline{STRT}$)) causes the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external clock. If $\overline{STRT}$ is removed (at least $t_R\overline{STRT}$) before clock period 2, a low signal applied to $\overline{STRT}$ will drop the DRDY flag as before, and with the first positive-going clock edge that meets the ($t_{SU}\overline{STRT}$) setup time, the converter will continue with clock period 3.

Clock

The HI5812 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronized with the rising edge of the clock signal.

Figure 21 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.

The internal clock will shut down if the A/D is not restarted after a conversion. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minimum frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge-pump voltage to decay.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum t_{LOW} and t_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

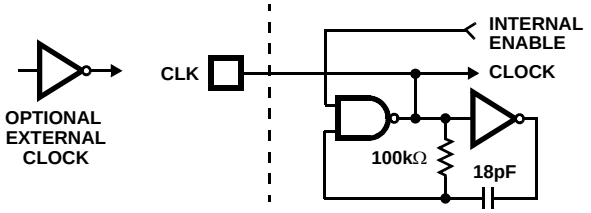


FIGURE 21. INTERNAL CLOCK CIRCUITRY

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{AA}+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The V_{AA}+ and V_{AA}- terminals supply the charge-balancing comparator only. Because the comparator is autobalanced between conversions, it has good low-frequency supply rejection. It does not reject well at high frequencies however; V_{AA}- should be returned to a clean analog ground and V_{AA}+ should be RC decoupled from the digital supply as shown in Figure 22.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}+. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A 10μF capacitor from V_{AA}+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to V_{AA}+ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76) dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10 \text{ Log } \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following:

$$SINAD = 10 \text{ Log } \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10 \text{ Log} \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \text{ Log} \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† V_{REF+} = 4.608V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE											
			MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	4.6069	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	4.6058	4094	1	1	1	1	1	1	1	1	1	1	1	0
$^3/_4$ FS	3.4560	3072	1	1	0	0	0	0	0	0	0	0	0	0
$^1/_2$ FS	2.3040	2048	1	0	0	0	0	0	0	0	0	0	0	0
$^1/_4$ FS	1.1520	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.001125	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

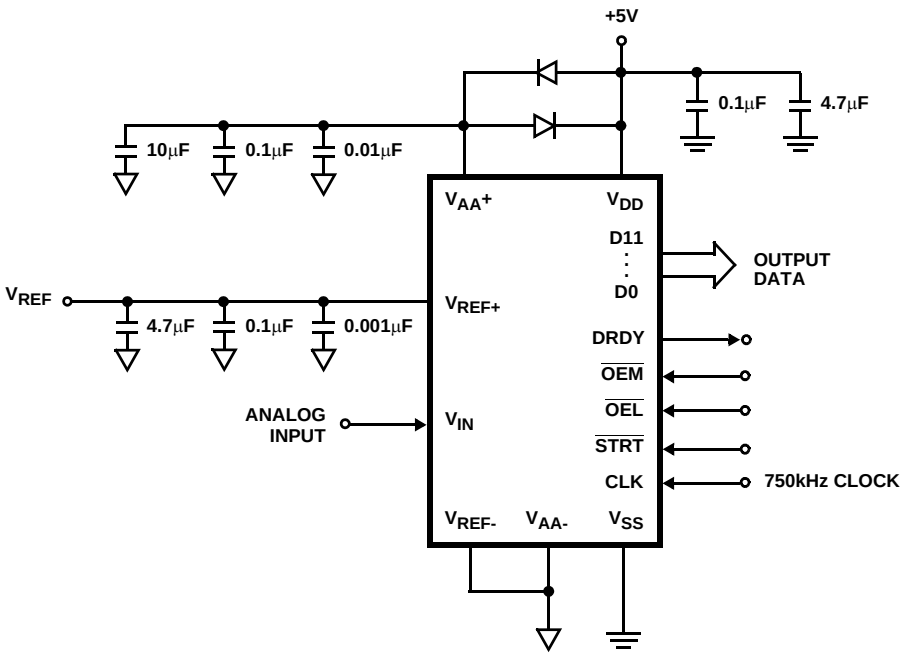


FIGURE 22. GROUND AND SUPPLY DECOUPLING

Die Characteristics

DIE DIMENSIONS:

3200µm x 3940µm

METALLIZATION:

Type: AlSi
Thickness: 11kÅ ±1kÅ

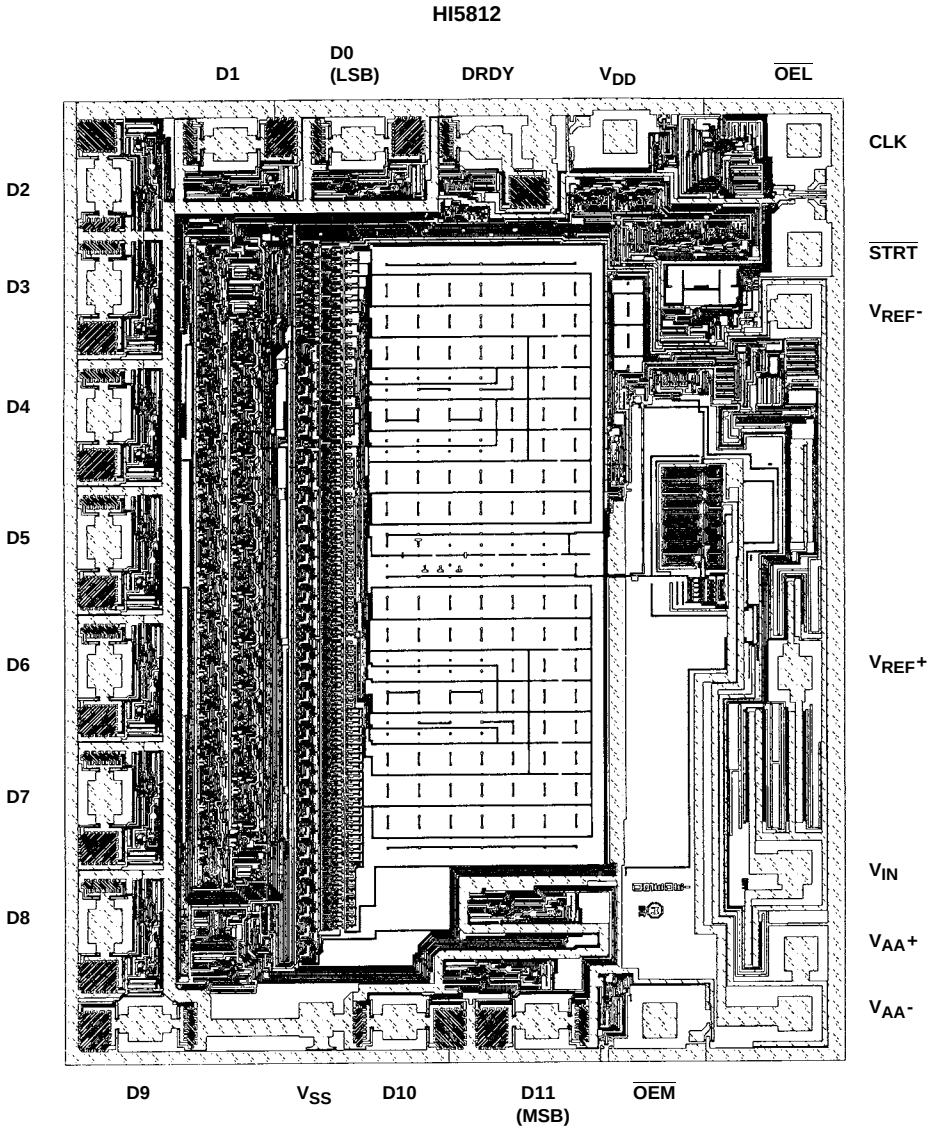
PASSIVATION:

Type: PSG
Thickness: 13kÅ ±2.5kÅ

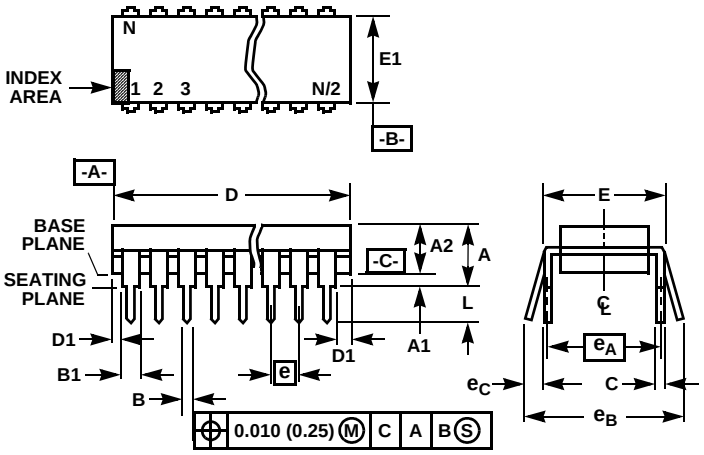
WORST CASE CURRENT DENSITY:

1.84×10^5 A/cm^2

Metallization Mask Layout



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

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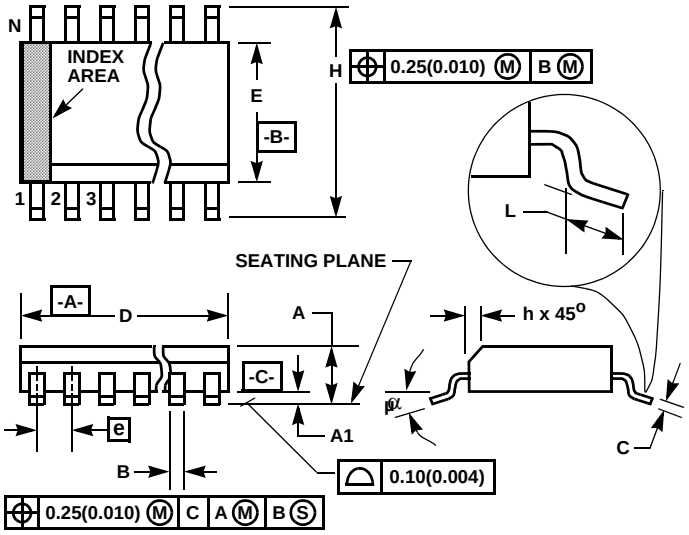
Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.