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MAX174/MX574A/MX674A

Industry-Standard, Complete 12-Bit ADCs

General Description

The MAX174/MX574A/MX674A are complete 12-bit analog-to-digital converters (ADCs) that combine high speed, low-power consumption, and on-chip clock and voltage reference. The maximum conversion times are 8µs (MAX174), 15µs (MX674A), and 25µs (MX574A). Maxim's BiCMOS construction reduces power dissipation 3 times (150mW) over comparable devices. The internal buried zener reference provides low-drift and low-noise performance. External component requirements are limited to only decoupling capacitors and fixed resistors. The versatile analog input structure allows for 0 to +10V or 0 to +20V unipolar or ±5V or ±10V bipolar input ranges with pin strapping.

The MAX174/MX574A/MX674A use standard microprocessor interface architectures and can be interfaced to 8-, 12-, and 16-bit wide buses. Three-state data outputs are controlled by $\overline{CS}$, CE, and R/$\overline{C}$ logic inputs.

***Ordering Information* appears at end of data sheet.**

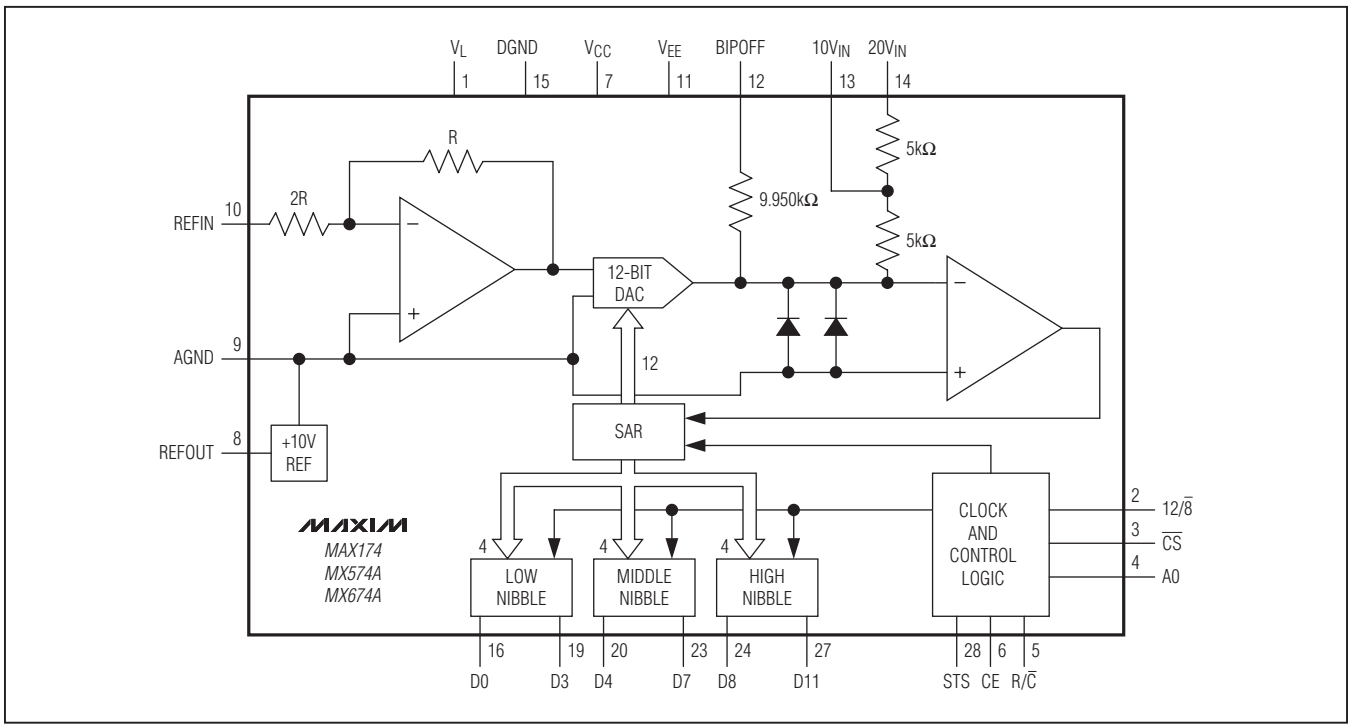
Features

- **Complete ADC with Reference and Clock**
- **12-Bit Resolution and Linearity**
- **No Missing Codes Over Temperature**
- **150mW Power Dissipation**
- **8µs (MAX174), 15µs (MX674A), and 25µs (MX574A) Max Conversion Times**
- **Precision Low TC Reference: 10ppm/°C**
- **Monolithic BiCMOS Construction**
- **150ns Maximum Data Access Time**

Applications

Digital Signal Processing
High-Accuracy Process Control
High-Speed Data Acquisition
Electro-Mechanical Systems

Functional Diagram



For related parts and recommended products to use with this part, refer to ***www.maxim-ic.com/MAX174.related***.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to DGND ..... 0 to 16.5V
V_{EE} to DGND ..... 0 to 16.5V
V_L to DGND ..... 0 to 7V
DGND to AGND ..... ±1V
Control Inputs to DGND
(CE, $\overline{CS}$, A0, 12/$\overline{8}$, R/$\overline{C}$) ..... -0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to DGND
(DB11–DB0, STS) ..... -0.3V to (V_L + 0.3V)
Analog Inputs to AGND (REFIN, BIPOFF, $10V_{IN}$) ..... ±16.5V
$20V_{IN}$ to AGND ..... ±24V
REFOUT ..... Indefinite short to V_{CC} or AGND

Power Dissipation (any package) to +75°C 1000mW
Derates above +75°C ..... 10mW/°C
Operating Temperature Ranges
MAX174_C, MX_74AJ/K/L ..... 0 to +70°C
MAX174_E, MX_74AJE/KE/LE ..... -40°C to +85°C
MAX174_M, MX_74AS/T/U ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
PDIP, Wide SO ..... +260°C
PLCC ..... +245°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX174

(V_L = +5V, V_{EE} = +15V or +12V, V_{EE} = -15V or -12V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Integral Nonlinearity	INL	T_A = +25°C	MAX174A/B			±1/2	LSB
			MAX174C			±1	
		T_A = T_{MIN} to T_{MAX}	MAX174AC/BC			±1/2	
			MAX174AE/BE/AM/BM			±3/4	
			MAX174C			±1	
Differential Nonlinearity	DNL	12 bits, no missing codes over temperature				±1	LSB
Unipolar Offset Error (Note 1)		MAX174A/B				±1	LSB
		MAX174C				±2	
Bipolar Offset Error (Notes 2, 3)		MAX174A				±3	LSB
		MAX174B/C				±4	
Full-Scale Calibration Error (Note 3)						±0.25	%
TEMPERATURE COEFFICIENTS (Using Internal Reference) (Notes 2, 3, 4)							
Unipolar Offset Change		MAX174A/B				±1	LSB
		MAX174C				±2	
Bipolar Offset Change		MAX174AC/BC				±1	LSB
		MAX174CC				±2	
		MAX174AE/AM				±1	
		MAX174BE/BM				±2	
		MAX174CE/CM				±4	

ELECTRICAL CHARACTERISTICS—MAX174 (continued)

(V_L = +5V, V_{EE} = +15V or +12V, V_{EE} = -15V or -12V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Scale Calibration Change		MAX174AC				±2 (10)	LSB (ppm/°C
		MAX174BC				±5 (27)	
		MAX174CC				±9 (50)	
		MAX174AE				±7 (19)	
		MAX174BE				±10 (38)	
		MAX174CE				±20 (75)	
		MAX174AM				±5 (12)	
		MAX174BM				±10 (25)	
		MAX174CM				±20 (50)	
INTERNAL REFERENCE							
Output Voltage		No load	MAX174A	9.98	10.00	10.02	V
			MAX174B/C	9.97	10.00	10.03	
Output Current (Note 5)		Available for external loads, in addition to REFIN and BIPOFF load				2	mA

ELECTRICAL CHARACTERISTICS—MX574A, MX674A

(V_L = + 5V, V_{EE} = +15V or +12V, V_{EE} = -15V or -12V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Integral Nonlinearity	INL	T_A = +25°C	MX574AK/L/T/U, MX674AK/L/T/U			±1/2	LSB
			MX574AJ/S, MX674AJ/S			±1	
		T_A = T_{MIN} to T_{MAX}	MX574AK/L/KE/LE			±1/2	
			MX674AK/L/KE/LE			±1/2	
			MX574AT/U, MX674AT/U			±3/4	
			MX574AJ/S, MX674AJ/S			±1	
Differential Nonlinearity	DNL	12 bits, no missing codes over temperature				±1	LSB
Unipolar Offset Error (Note 1)		MX574AK/L/T/U, MX674AK/L/T/U				±1	LSB
		MX574AJ/S, MX674AJ/S				±2	
Bipolar Offset Error (Notes 2, 3)		MX574AL/U, MX674AL/U				±3	LSB
		MX574AJ/K/S/T, MX674AJ/K/S/T				±4	
Full-Scale Calibration Error (Note 3)		MX574AL/U				±0.125	%
		MX574AJ/K/S/T, MX674A				±0.25	
TEMPERATURE COEFFICIENTS (Using Internal Reference) (Notes 2, 3, 4)							
Unipolar Offset Change		MX574AK/L/T/U, MX674AK/L/T/U				±1	LSB
		MX574AJ/S, MX674AJ/S				±2	

ELECTRICAL CHARACTERISTICS—MX574A, MX674A (continued)

(V_L = + 5V, V_{EE} = +15V or +12V, V_{EE} = -15V or -12V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bipolar Offset Change		MX574AK/L, MX674AK/L				±1	LSB
		MX574AJ, MX674AJ				±2	
		MX574AU/LE, MX674AU/LE				±1	
		MX574AT/KE, MX674AT/KE				±2	
		MX574AS/JE, MX674AS/JE				±4	
Full-Scale Calibration Change		MX574AL, MX674AL				±2 (10)	LSB (ppm/°C
		MX574AK, MX674AK				±5 (27)	
		MX574AJ, MX674AJ				±9 (50)	
		MX574ALE, MX674ALE				±7 (19)	
		MX574AKE, MX674AKE				±10 (38)	
		MX574AJE, MX674AJE				±20 (75)	
		MX574AU, MX674AU				±5 (12)	
		MX574AT, MX674AT				±10 (25)	
		MX574AS, MX674AS				±20 (50)	
INTERNAL REFERENCE							
Output Voltage		No load	MX574AL/U	9.99	10.00	10.01	V
			MX574AJ/K/S/T, MX674AL/U	9.98	10.00	10.02	
			MX674AJ/K/S/T	9.97	10.00	10.03	
Output Current (Note 5)		Available for external loads, in addition to REFIN and BIPOFF load				2	mA

ELECTRICAL CHARACTERISTICS—MAX174/MX574/MX674A

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Bipolar Input Range		Using 10V input				±5	V
		Using 20V input				±10	
Unipolar Input Range		Using 10V input		0		+10	V
		Using 20V input		0		+20	
Input Impedance		10V input		3	5	7	kΩ
		20V input		6	10	14	
POWER-SUPPLY REJECTION (Max Change in Full-Scale Calibration)							
V_{CC} Only		15V ±1.5V or 12V ±0.6V	MAX174A/B, MX_74AK/L/TU		±1/8	±1	LSB
			MAX174C, MX_74AJ/S		±1/8	±2	
V_{EE} Only		15V ±1.5V or 12V ±0.6V			±1/8	±1/2	LSB
V_L Only		5V ±0.5V			±1/8	±1/2	LSB
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$		2.0			V

ELECTRICAL CHARACTERISTICS—MAX174/MX574/MX674A (continued)

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current	I_{IN}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$, V_{IN} = 0 to V_L				±5	µA
Input Capacitance	C_{IN}	$\overline{CS}$, CE, R/$\overline{C}$, A0, 12/$\overline{8}$			7		pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	DB11–DB0, STS	I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	DB11–DB0, STS	I_{SOURCE} = 500µA	4			V
Floating State Leakage Current	I_{LKG}	DB11–DB0, STS	V_{OUT} = 0 to V_L			±10	µA
Floating State Output Capacitance	C_{OUT}	DB11–DB0			8		pF
CONVERSION TIME							
12-Bit Cycle	t_{CONV}	MX574A		15	20	25	µs
		MX674A		9	12	15	
		MAX174		6	7	8	
8-Bit Cycle	t_{CONV}	MX574A		10	14	18	µs
		MX674A		6	8	11	
		MAX174		4	5	6	
POWER REQUIREMENTS							
V_{CC} Operating Range				11.4		16.5	V
V_L Operating Range				4.5		5.5	V
V_{EE} Operating Range				-11.4		-16.5	V
V_{CC} Supply Current (Note 5)	I_{CC}				3	5	mA
V_L Supply Current (Note 5)	I_L				3	8	mA
V_{EE} Supply Current (Note 5)	I_{EE}				6	10	mA
Power Dissipation (Note 5)	P_D	V_{CC} = +15V and V_{EE} = -15V			150	265	mW

Note 1: Adjustable to zero.
Note 2: With 50Ω fixed resistor from REFOUT to BIPOFF. Adjustable to zero.
Note 3: With 50Ω fixed resistor from REFOUT to REFIN. Adjustable to zero.
Note 4: Maximum change in specification from T_A = +25°C to T_{MIN} or T_A = +25°C to T_{MAX}.
Note 5: External load current should not change during a conversion. For ±12V supply operation, REFOUT need not be buffered except when external load in addition to REFIN and BIPOFF inputs have to be driven.

TIMING CHARACTERISTICS—MAX174/MX574A/MX674A (Note 6)

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = -40°C TO +85°C T_A = 0°C TO +70° C			T_A = -55°C TO +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CONVERT START TIMING—FULL CONTROL MODE												
STS Delay from CE	t_{DSC}	C_L = 50pF		100	200			250			320	ns
CE Pulse Width	t_{HEC}		50	15		50			50			ns
$\overline{CS}$ to CE Setup	t_{SSC}		50			50			50			ns
$\overline{CS}$ Low During CE High	t_{HSC}		50			50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRC}		50			50			50			ns
R/$\overline{C}$ Low During CE High	t_{HRC}		50			50			50			ns
A0 to CE Setup	t_{SAC}		0			0			0			ns
A0 Valid During CE High	t_{HAC}		50			50			50			ns
READ TIMING—FULL CONTROL MODE												
Access Time (From CE)	t_{DD}	C_L = 100pF		60	120			150			200	ns
Data Valid After CE Low	t_{HD}		25	40		20			15			ns
Output Float Delay	t_{HL}				75			100			120	ns
$\overline{CS}$ to CE Setup	t_{SSR}		50			50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRR}		0			0			0			ns
A0 to CE Setup	t_{SAR}		50			50			50			ns
$\overline{CS}$ Valid After CE Low	t_{HSR}		0			0			0			ns
R/$\overline{C}$ High After CE Low	t_{HRR}		0			0			0			ns
A0 Valid After CE Low	t_{HAR}		0			0			0			ns
STAND-ALONE MODE												
Low R/$\overline{C}$ Pulse Width	t_{HRL}		50	15		50			50			ns
STS Delay from R/$\overline{C}$	t_{DS}			115	200			250			320	ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}		25	40		20			15			ns
STS Delay After Data Valid	t_{HS}	MX574A	300	600	1000	300		1000	300		1000	ns
		MX674A	30	320	600	30		600	30		600	
		MAX174	30	140	300	30		300	30		400	
High R/$\overline{C}$ Pulse Width	t_{HRH}		150			150			200			ns
Data Access Time	t_{DDR}	C_L = 100pF		60	120			150			200	ns

Note 6: Timing specifications guaranteed by design. All input control signals specified with $t_R = t_F$ = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. See loading circuits in Figures 1 and 2.

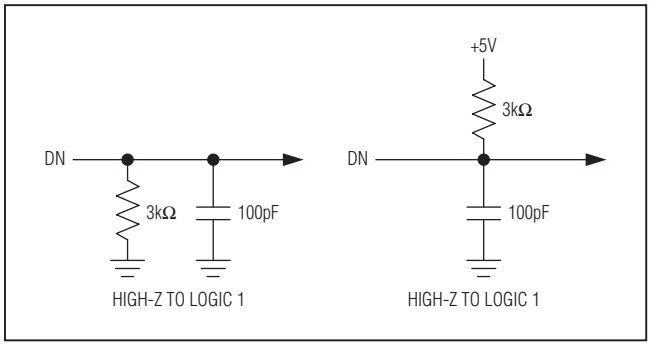


Figure 1. Load Circuit for Access Time Test

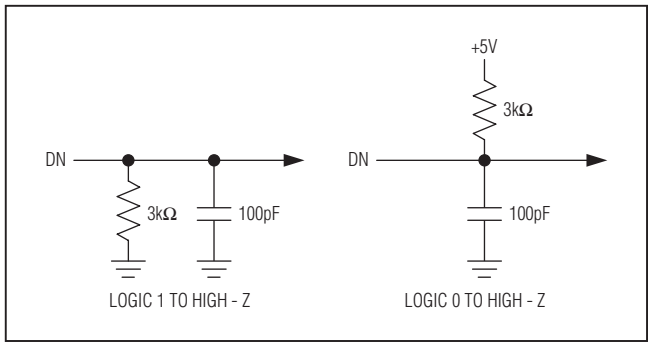
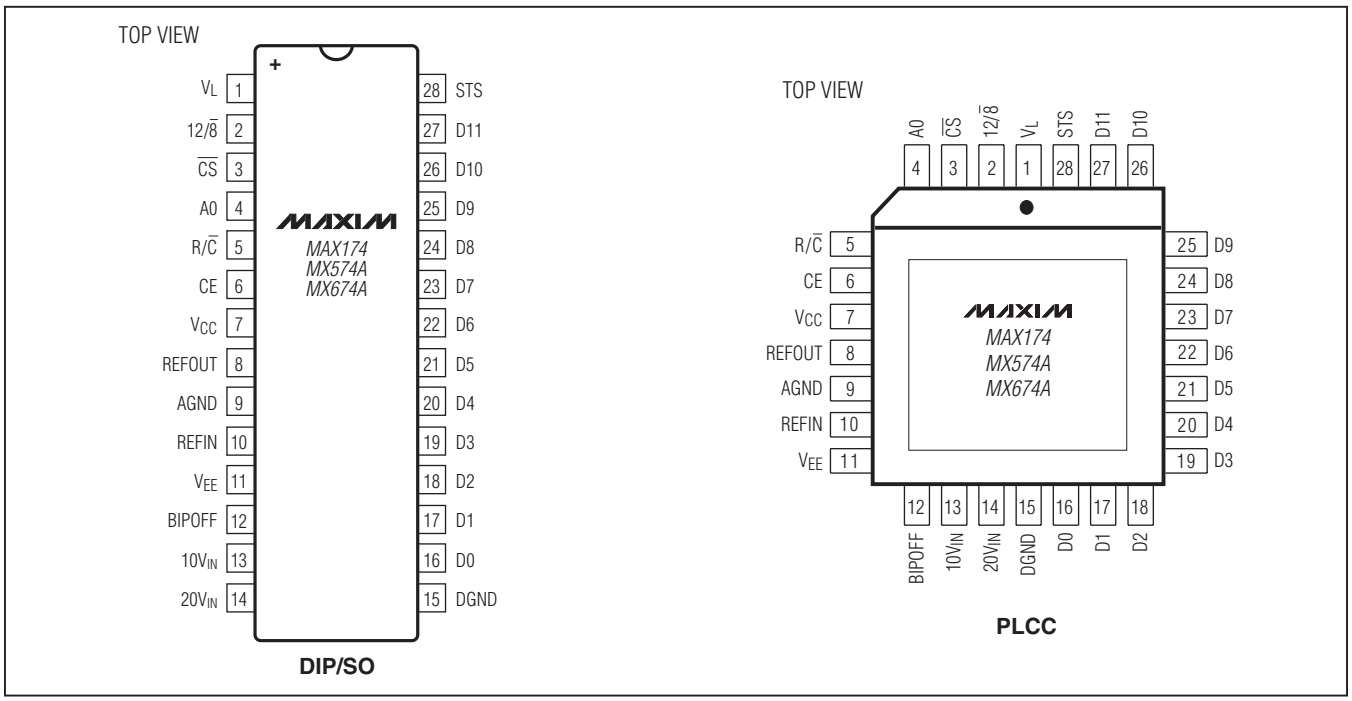


Figure 2. Load Circuit for Output Float Delay Test

Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	V_L	Logic Supply, +5V
2	$12/\overline{8}$	Data Mode Select Input
3	CS	Chip-Select Input. Must be low to select device.
4	A0	Byte Address/Short-Cycle Input. When starting a conversion, controls number of bits converted (low = 12 bits, high = 8 bits). When reading data, if $12/\overline{8}$ = low, enables low byte (A0 = high) or high byte (A0 = low).
5	$R/\overline{C}$	Read/Convert Input. When high, the device will be in the data-read mode. When low, the device will be in the conversion start mode.

Pin Description (continued)

PIN	NAME	FUNCTION
6	CE	Chip-Enable Input. Must be high to select device.
7	V_{CC}	+12V or +15V Supply
8	REFOUT	+10V Reference Output
9	AGND	Analog Ground
10	REFIN	Reference Input
11	V_{EE}	-12V or -15V Supply
12	BIPOFF	Bipolar Offset Input. Connect to REFOUT for bipolar input range.
13	$10V_{IN}$	10V Span Input
14	$20V_{IN}$	20V Span Input
15	DGND	Digital Ground
16–27	D0–D11	Three-State Data Outputs
28	STS	Status Output

Detailed Description

Converter Operation

The MAX174/MX574A/MX674A use a successive approximation technique to convert an unknown analog input to a 12-bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital (A/D) function.

The internal voltage output DAC is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 5kΩ resistor for the 10V input and 10kΩ resistor for the 20V input. The comparator is essentially a zero-crossing detector, and its output is fed back to the SAR input.

The SAR is set to half-scale as soon as a conversion starts. The analog input is compared to 1/2 of the full-scale voltage. The bit is kept if the analog input is greater than half-scale or dropped if smaller. The next bit, bit 10, is then set with the DAC output either at 1/4 scale, if the most significant bit (MSB) is dropped, or 3/4 scale if the MSB is kept. The conversion continues in this manner until the least significant bit (LSB) is tried. At the end of the conversion, the SAR output is latched into the output buffers.

Digital Interface

CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the MAX174/MX574A/MX674A. While both CE and $\overline{CS}$ are asserted, the state of R/$\overline{C}$ selects whether a conversion (R/$\overline{C}$ = 0) or a data read (R/$\overline{C}$ = 1) is in progress. The register control inputs, 12/$\overline{8}$ and A0, select the data format and conversion length. A0 is usually tied to the LSB of the address bus. To perform a full 12-bit conversion, set A0 low during a convert start. For a shorter 8-bit conversion, A0 must be high during a convert start.

Output Data Format

During a data read, A0 also selects whether the three-state buffers contain the 8 MSBs (A0 = 0) or the 4 LSBs (A0 = 1) of the digital result. The 4 LSBs are followed by 4 trailing 0s.

Output data is formatted according to the 12/$\overline{8}$ pin. If this input is low, the output will be a word broken into two 8-bit bytes. This allows direct interlace to 8-bit buses without the need for external three-state buffers. If 12/$\overline{8}$ is high, the output will be one 12-bit word. A0 can change state while a data-read operation is in effect.

To begin a conversion, the microprocessor must write to the ADC address. Then, since a conversion usually takes longer than a single clock cycle, the microprocessor must wait for the ADC to complete the conversion. Valid data will be made available only at the end of the conversion, which is indicated by STS. STS can be ether polled or used to generate an interrupt upon completion. Or, the microprocessor can be kept idle by inserting the appropriate number of No Operation (NOP) instructions between the conversion-start and data-read commands.

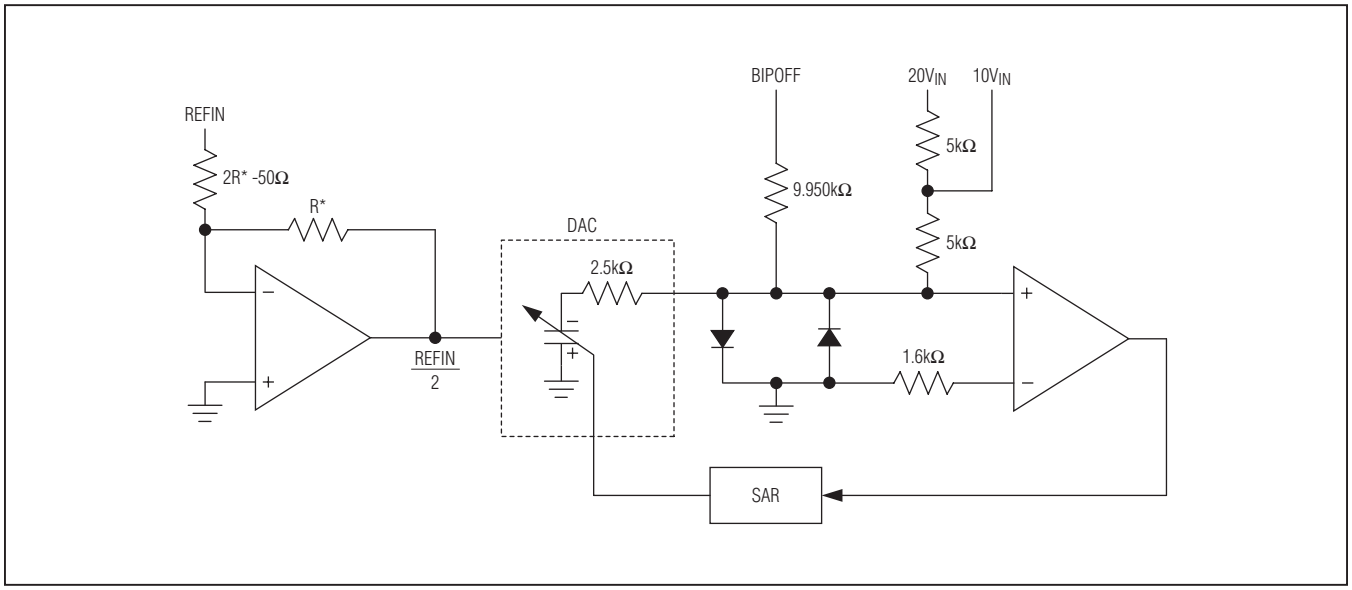


Figure 3. Analog Equivalent Circuit

Table 1. Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 12-bit conversion
1	0	1	1	X	Enable 12-bit conversion
1	0	1	0	0	Enable 8 MSBs
1	0	1	0	1	Enable 4 LSBs + 4 trailing 0s

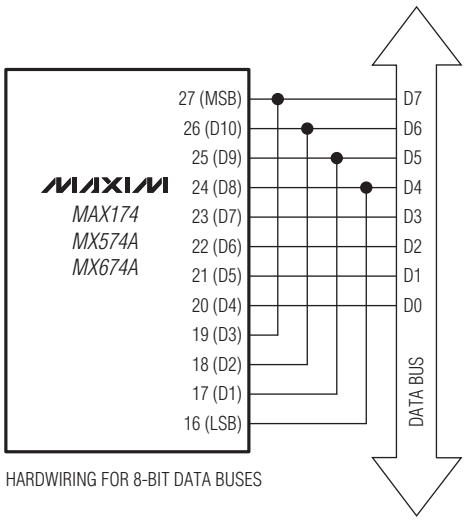
After the conversion is completed, data can be obtained by the microprocessor. The ADCs have the required logic for 8-, 12-, and 16-bit bus interfacing, which is determined by the 12/$\overline{8}$ input. If 12/$\overline{8}$ is high, the ADCs are configured for a 16-bit bus. Data lines D0–D11 may be connected to the bus as either the 12 MSBs or the 12 LSBs. The other 4 bits must be masked out in software.

For 8-bit bus operation, 12/$\overline{8}$ is set low. The format is left justified, and the even address, A0 low, contains the 8 MSBs. The odd address, A0 high, contains the 4 LSBs, which is followed by 4 trailing 0s. There is no need to use a software mask when the ADCs are connected to an 8-bit bus.

Note that the output cannot be forced to a right-justified format by rearranging the data lines on the 8-bit bus interface.

Table 2. MAX174/MX574A/MX674A Data Format for 8-Bit Bus

	D7	D6	D5	D4	D3	D2	D1	D0
High Byte (A0 = 0)	MSB	D10	D9	D8	D7	D6	D5	D4
Low Byte (A0 = 1)	D3	D2	D1	D0	0	0	0	0



HARDWIRING FOR 8-BIT DATA BUSES

Timing and Control

Convert Start Timing—Full Control Mode

R/$\overline{C}$ must be low before asserting both CE and $\overline{CS}$. If it is high, a brief read operation occurs possibly resulting in system bus contention. To initiate a conversion, use either CE or $\overline{CS}$. CE is recommended since it is shorter by one propagation delay than $\overline{CS}$ and is the faster input of the two. CE is used to begin the conversion in Figure 4.

The STS output is high during the conversion indicating the ADC is busy. During this period, additional convert start commands will be ignored, so that the conversion cannot be prematurely terminated or restarted. However, if the state of A0 is changed after the beginning of the conversion, any additional start conversion transitions will latch the new state of A0, possibly resulting in an incorrect conversion length (8 bits vs. 12 bits) for that conversion.

Read Timing—Full Control Mode

Figure 5 illustrates the read-cycle timing. While reading data, access time is measured from when CE and R/$\overline{C}$ are both high. Access time is extended 10ns if $\overline{CS}$ is used to initiate a read.

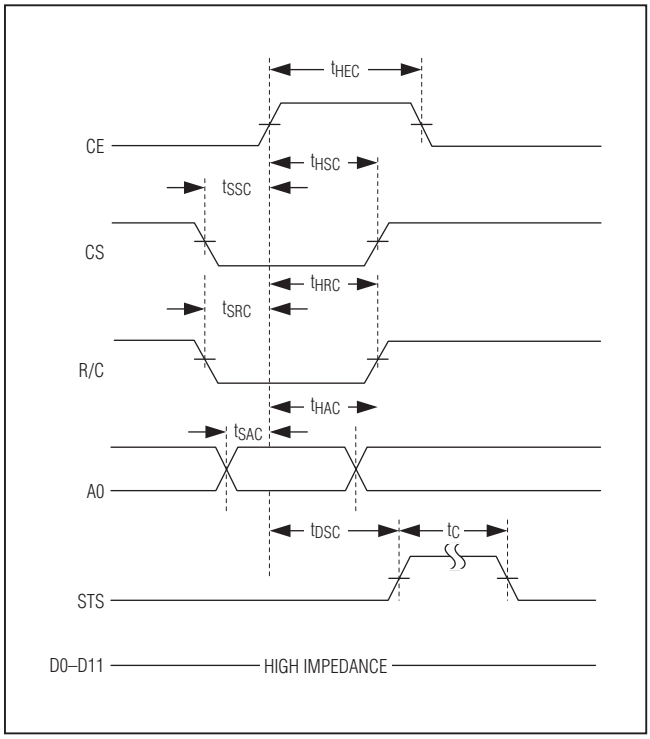


Figure 4. Convert Start Timing

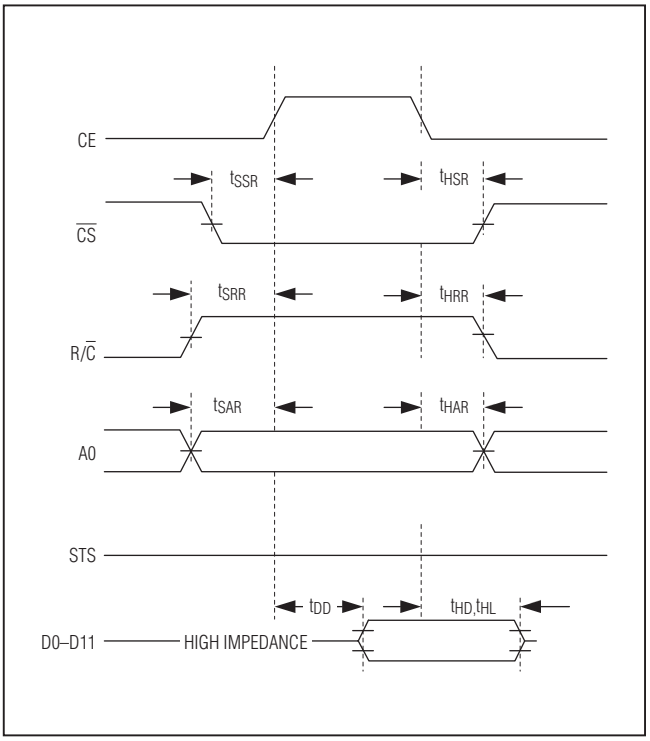


Figure 5. Read Timing

Stand-Alone Operation

For systems which do not use or require full bus interfacing, the MAX174/MX574A/MX674A can be operated in a stand-alone mode directly linked through dedicated input ports.

When configured in the stand-alone mode, conversion is controlled by R/$\overline{C}$. In addition, $\overline{CS}$ and A0 are wired low; CE and 12/$\overline{8}$ are wired high. To enable the three-state buffers, set R/$\overline{C}$ low. A conversion starts when R/$\overline{C}$ is set high. This allows either a high- or a low-pulse control signal. Shown in Figure 6 is the operation with a low pulse. In this mode, the outputs, in response to the falling edge of R/$\overline{C}$, are forced into the high-impedance state and return to valid logic-levels after the conversion is complete. The STS output goes high following the R/$\overline{C}$ falling edge and returns low when the conversion is complete.

A high-pulse conversion initiation is illustrated in Figure 7. When R/$\overline{C}$ is high, the data lines are enabled. The next conversion starts with the falling edge of R/$\overline{C}$. The data lines return and remain in high impedance state until another R/$\overline{C}$ high pulse.

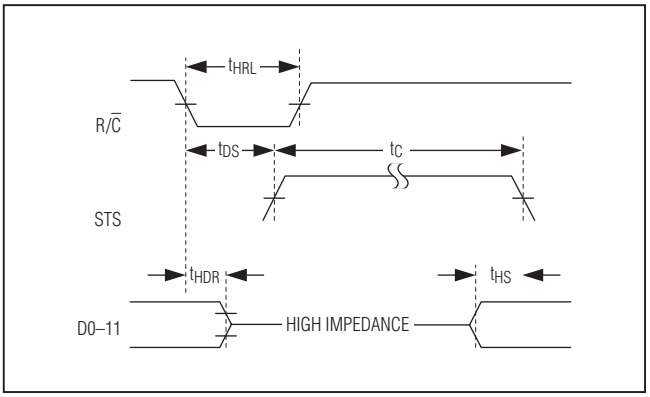


Figure 6. Low Pulse for R//C in Stand-Alone Mode

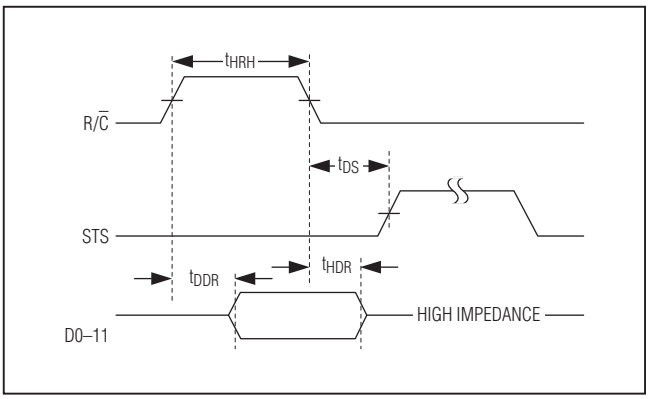


Figure 7. High Pulse for R//C in Stand-Alone Mode

Analog Considerations

Application Hints

Physical Layout

For best system performance, PCBs should be used for the MAX174/MX574A/MX674A. Wirewrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX174/MX574A/MX674A.

Grounding

The recommended power-supply grounding practice is shown in Figure 8. The ground reference point for the on-chip reference is AGND. It should be connected directly to the analog reference point of the system. The analog and digital grounds should be connected together at the package in order to gain all of the accuracy possible from the MAX174/MX574A/MX674A in high digital noise environments. In situations permitting, they can be connected to the most accessible ground-reference point. The preference is analog power return.

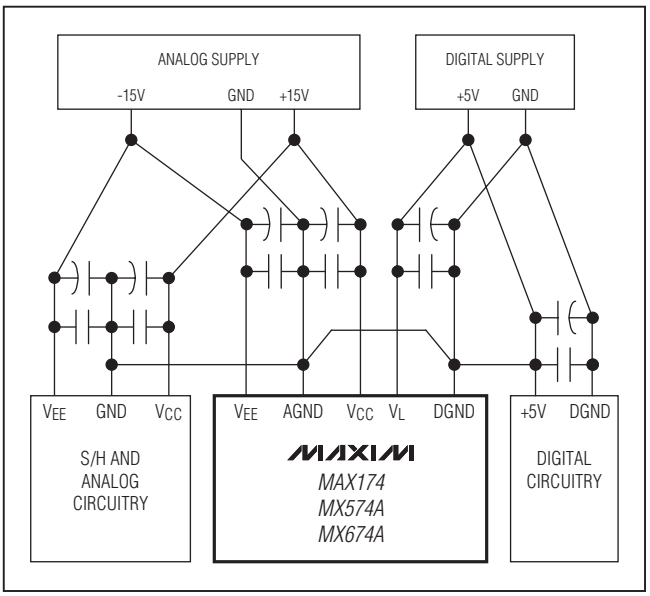


Figure 8. Power-Supply Grounding Practice

Power-Supply Bypassing

The MAX174/MX574A/MX674A power supplies must be filtered, well regulated, and free from high-frequency noise, or unstable output codes will result. Unless great care is taken in filtering any switching spikes present in the output, switching power supplies is not suggested for applications requiring 12-bit resolution. Take note that a few millivolts of noise converts to several error counts in a 12-bit ADC.

All power-supply pins should use supply decoupling capacitors connected with short lead length to the pins, as shown in Figure 9. The V_{CC} and V_{EE} pins should be decoupled directly to AGND. A 4.7µF tantalum type in parallel with a 0 1µF disc ceramic type is a suitable decoupling.

Internal Reference

The MAX174/MX574A/MX674A have an internal buried zener reference that provides a 10V, low-noise and low-temperature drift output. An external reference voltage can also be used for the ADC. When using ±15V supplies, the internal reference can source up to 2mA in addition to the BIPOFF and REFIN inputs over the entire operating temperature range. With ±12V supplies, the reference can drive the BIPOFF and REFIN inputs over temperature, but it CANNOT drive an additional load.

Driving the Analog Input

The input leads to AGND and $10V_{IN}$ or $20V_{IN}$ should be as short as possible to minimize noise pick up. If long leads are needed, use shielded cables.

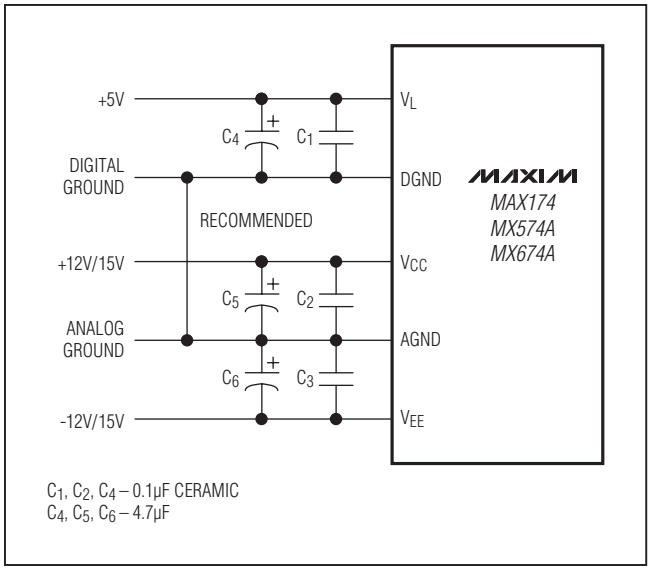


Figure 9. Power-Supply Bypassing

When using the $20V_{IN}$ as the analog input, load capacitance on the $10V_{IN}$ pin must be minimized. Especially on the faster MAX174, leave the $10V_{IN}$ pin open to minimize capacitance and to prevent linearity errors caused by inadequate settling time.

The amplifier driving the analog input must have low enough DC output impedance for low full-scale error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during the conversion. The output impedance of an amplifier is the open-loop output impedance divided by the loop gain at the frequency of interest.

MX574A and MX674A—The approximate internal clock rate is 600kHz and 1MHz, respectively, and amplifiers like the MAX400 can be used to drive the input.

MAX174—The internal clock rate is 2MHz and faster amplifiers like the OP-27, AD711, or OP-42 are required.

Track-and-Hold Interface

The analog input to the ADC must be stable to within 1/2 LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a couple of hertz for sinusoidal inputs even with the faster MAX174. For higher bandwidth signals, a track-and-hold amplifier should be used.

The STS output may be used to provide the Hold signal to the track-and-hold amplifier. However, since the A/D's DAC is switched at approximately the same time as the conversion is initiated, the switching transients at the output of the T/H caused by the DAC switching may result in code dependent errors. It is recommended that the Hold signal to the T/H amplifier precede a conversion or be coincident with the conversion start.

The first bit decision by the A/D is made approximately 1.5 clock cycles after the start of the conversion. This is 2.5µs, 1.5µs, and 0.8µs for the MX574A, MX674A, and MAX174, respectively. The T/H hold settling time must be less than this time. For the MX574A and MX674A, the AD585 sample-and-hold is recommended (Figure 10). For the MAX174, a faster T/H amplifier, like the HA5320 or HA5330, should be used (Figure 11).

Input Configurations

The MAX174/MX574A/MX674A input range can be set using pin strapping. Table 3 shows the possible input ranges and ideal transition voltages. End-point errors can be adjusted in all ranges.

Table 3. Input Ranges and Ideal Digital Output Codes

ANALOG INPUT VOLTAGE (V)				DIGITAL OUTPUT
0 to +10V	**0 to +20V**	**±5V**	**±10V**	**MSB LSB**
+10.0000	+20.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+19.9927	+4.9963	+9.9927	1111 1111 1110*
+5.0012	+10.0024	+0.0012	+0.0024	1000 0000 0000*
+4.9988	+9.9976	-0.0012	-0.0024	0111 1111 1111*
+4.9963	+9.9927	-0.0037	-0.0073	0111 1111 1110*
+0.0012	+0.0024	-4.9988	-9.9976	0000 0000 0000*
0.0000	0.0000	-5.0000	-10.0000	0000 0000 0000

Note 7: For unipolar input ranges, output coding is straight binary.
Note 8: For bipolar input ranges, output coding is offset binary.
Note 9: For 0 to + 10V or ±5V ranges, 1 LSB = 2.44mV.
Note 10: For 0 to +20V or ±10V ranges, 1 LSB = 4.88mV.

**The digital outputs will be flickering between the Indicated code and the indicated code plus one.*

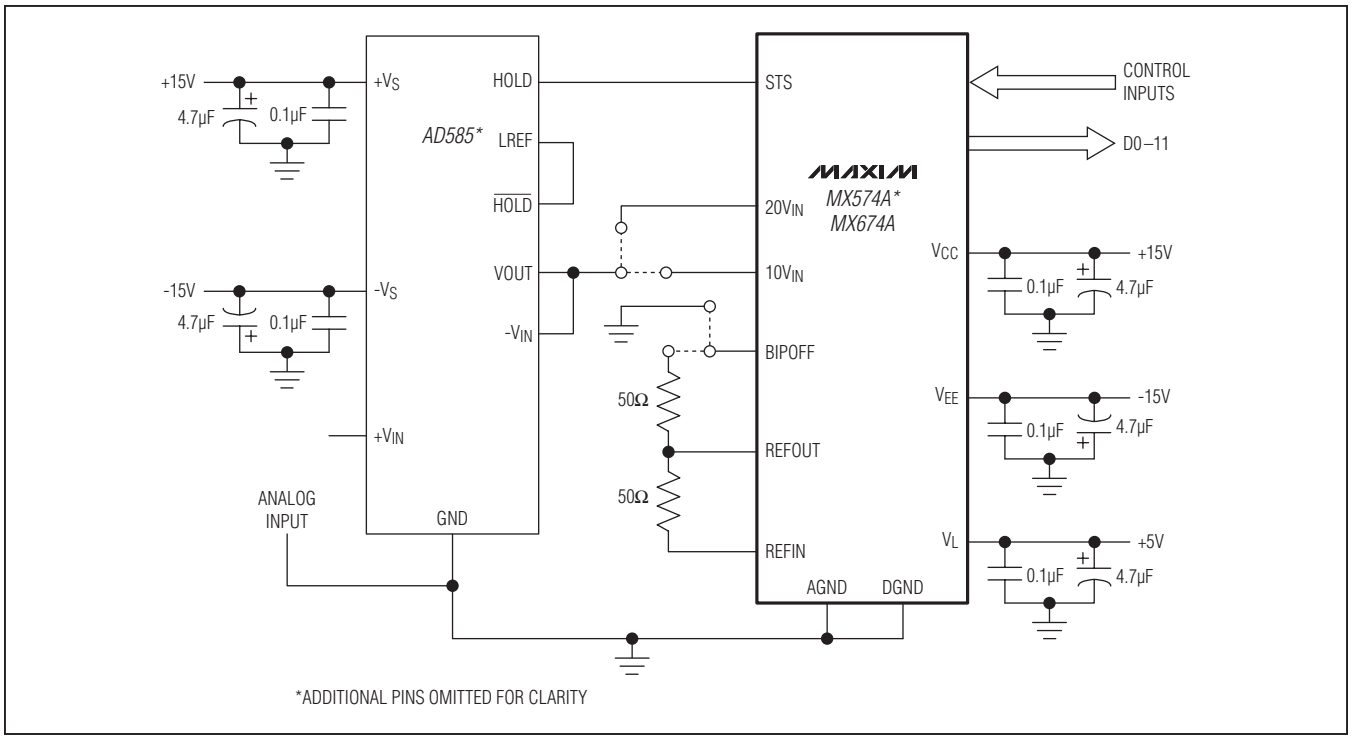


Figure 10. MX574/MX674A to AD585 Sample-and-Hold Interface

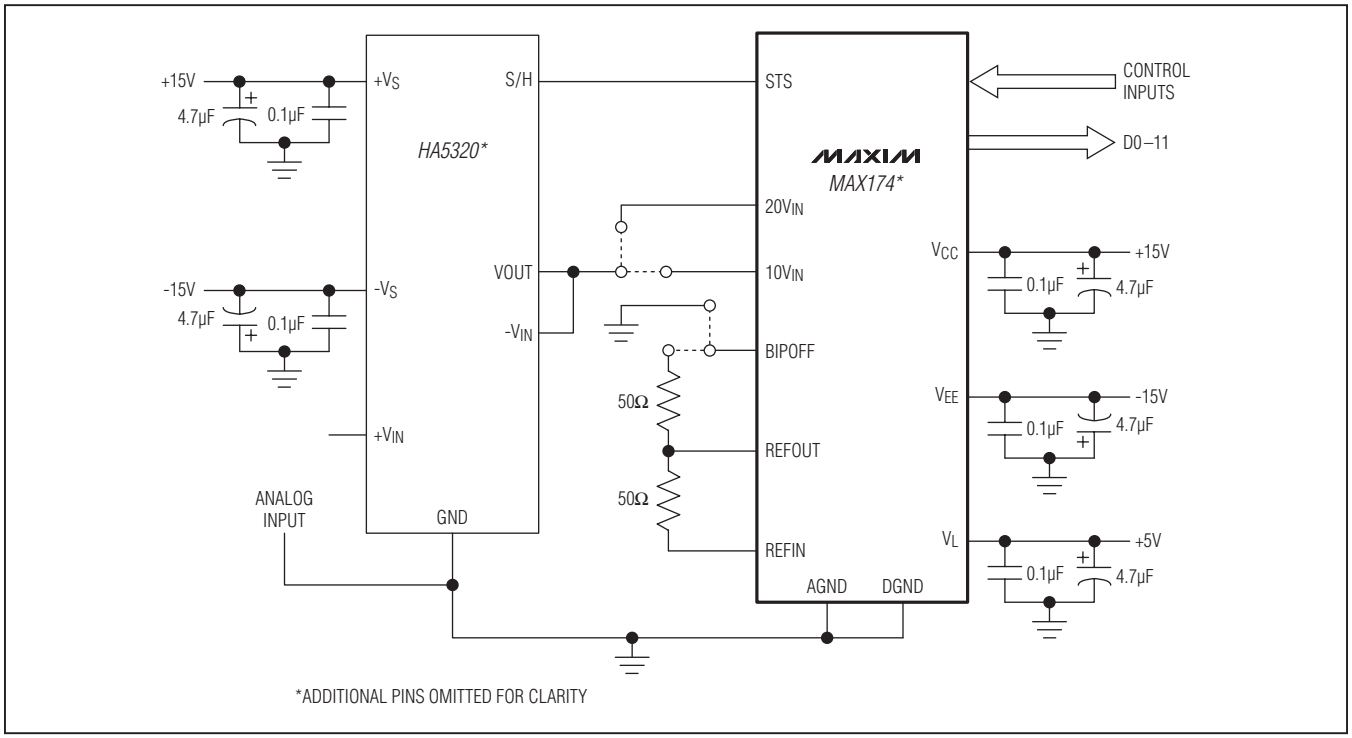


Figure 11. MAX174 to HA5320 Sample-and-Hold Interface

Unipolar Input Operation

The unipolar transfer function and input connections are shown in Figures 12 and 13.

Because all internal resistors of the MAX174/MX574A/MX674A are trimmed for absolute calibration, additional trimming is not necessary for most applications. The absolute accuracy for each grade is given in the specification tables.

If the offset trim is not needed, BIPOFF can be tied directly to AGND. The two resistors and trimmer for BIPOFF can then be discarded. A 50Ω ±1% metal film resistor should be attached between REFOUT and REFIN.

For a 0 to +10V input range, the analog input is connected between AGND and $10V_{IN}$. For a 0 to +20V input range, the analog input is connected between AGND and $20V_{IN}$. These ADCs can easily handle an input signal beyond the supplies. If full-scale trim is not needed, the gain trimmer, R2, should be swapped with a 50Ω resistor. Should a 10.24V input range be selected, a 200Ω trimmer should be inserted in series with $10V_{IN}$. For a full-scale input range of 20.48V, use a 500Ω trimmer in series with $20V_{IN}$. The nominal input impedance into $10V_{IN}$ is 5kΩ and 10kΩ for $20V_{IN}$.

Offset and Full-Scale Adjustment

In applications where the offset and full-scale range have to be adjusted, use the circuit shown in Figure 12. The offset should be adjusted first. Apply 1/2 LSB at the analog input and adjust R1 until the digital output code flickers between 0000 0000 0000 and 0000 0000 0001. To adjust the full-scale range, apply FS - 3/2 LSB at the analog input and adjust R2 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

Bipolar Input Operation

The bipolar transfer function is shown in Figure 14, and input connections are shown in Figure 15. One or both of the trimmers can be exchanged with a 50Ω ±1% fixed resistor if the offset and gain specifications suffice.

Offset and Full-Scale Adjustment

To begin bipolar calibration, a signal 1/2 LSB above negative full-scale is applied. R1 is trimmed until the digital output flickers between 0000 0000 0000 and 0000 0000 0001. Next, a signal 3/2 LSB below positive full scale is applied. Then, R2 is trimmed until the output flickers between 1111 1111 1110 and 1111 1111 1111.

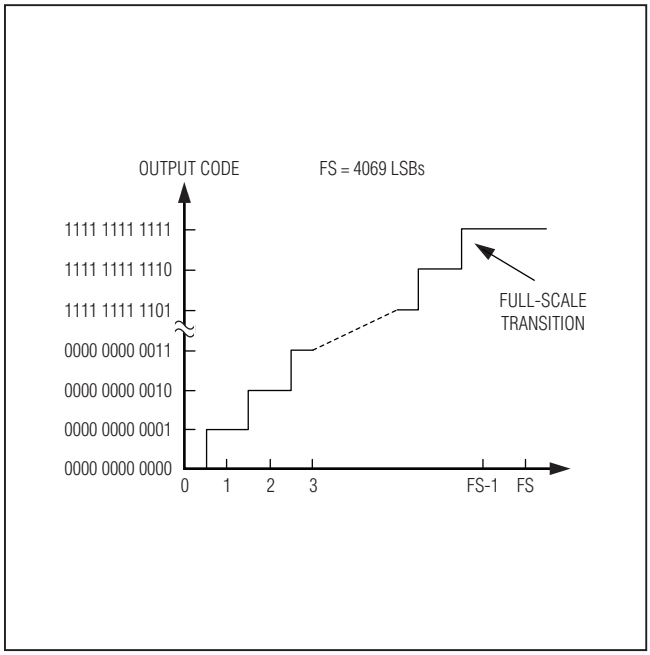


Figure 12. Ideal Unipolar Transfer Function

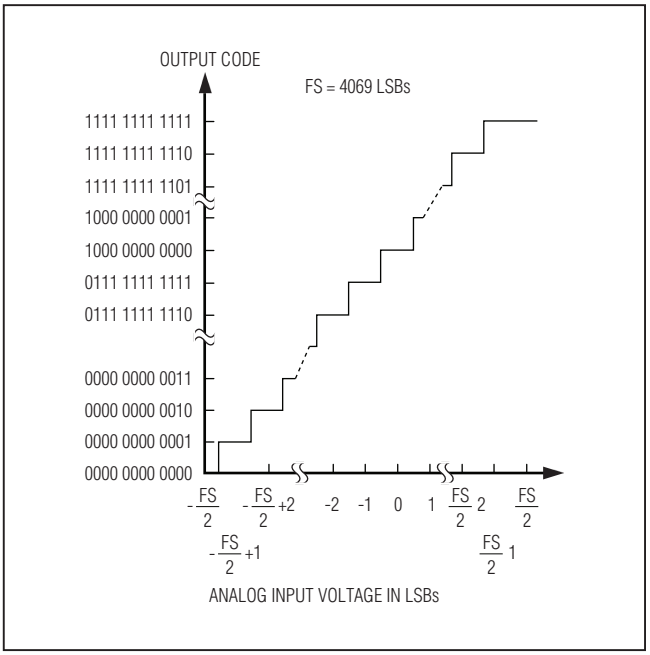


Figure 14. Ideal Bipolar Transfer Function

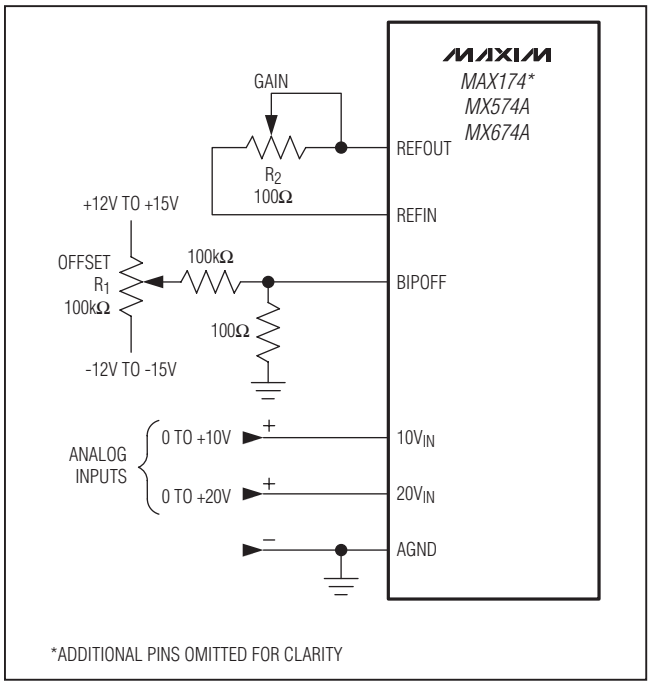


Figure 13. Unipolar Input Connections

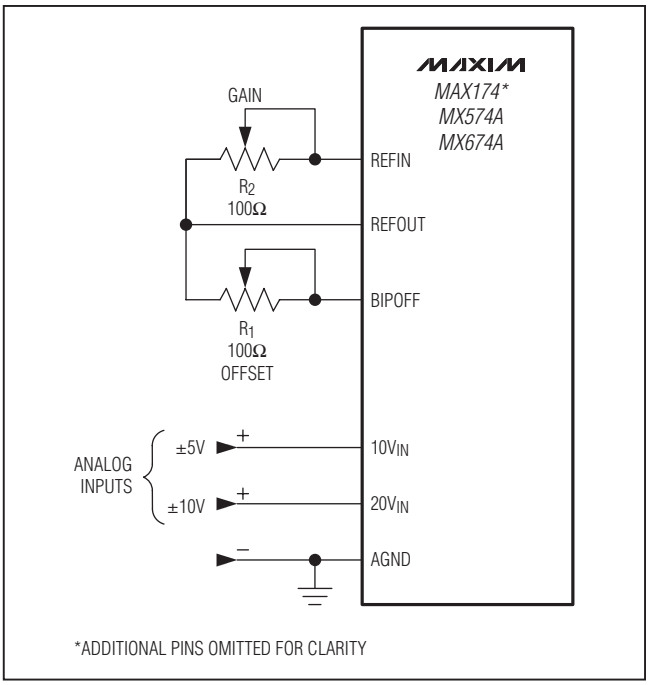


Figure 15. Bipolar Input Connections

Ordering Information

PART	PIN-PACKAGE	LINEARITY (LSB)	TEMPCO (ppm/°C)
8µs Maximum Conversion Time			
TEMP RANGE: 0°C to +70°C			
MAX174ACPI+	28 Plastic DIP	½	10
MAX174BCPI+	28 Plastic DIP	½	27
MAX174CCPI+	28 Plastic DIP	1	50
MAX174ACWI+	28 Wide SO	½	10
MAX174BCWI+	28 Wide SO	½	27
MAX174CCWI+	28 Wide SO	1	50
MAX174BC/D	Dice*	1/2	—
TEMP RANGE: -40°C to +85°C			
MAX174AEPI+	28 Plastic DIP	½	19
MAX174BEPI+	28 Plastic DIP	½	38
MAX174CEPI+	28 Plastic DIP	1	75
MAX174AEWI+	28 Wide SO	½	19
MAX174BEWI+	28 Wide SO	½	38
MAX174CEWI+	28 Wide SO	1	75
TEMP RANGE: -55°C to +125°C			
MAX174AMJI	28 CERDIP	¾	12
MAX174BMJI	28 CERDIP	¾	25
MAX174CMJ	28 CERDIP	1/21	50
15µs Maximum Conversion Time			
TEMP RANGE: 0°C to +70°C			
MX674AJN+	28 Plastic DIP	1	50
MX674AKN+	28 Plastic DIP	½	27
MX674ALN+	28 Plastic DIP	½	10
MX674AJCWI+	28 Wide SO	1	50
MX674AKCWI+	28 Wide SO	½	27
MX674ALCWI+	28 Wide SO	½	10
MX674AK/D	Dice*	½	—
TEMP RANGE: -40°C to +85°C			
MX674AJEPI+	28 Plastic DIP	1	75
MX674AKEPI+	28 Plastic DIP	½	38
MX674ALEPI+	28 Plastic DIP	½	19
MX674AJEWI+	28 Wide SO	1	75
MX674AKEWI+	28 Wide SO	½	38
MX674ALEWI+	28 Wide SO	½	19
TEMP RANGE: -55°C to +125°C			
MX674ASQ	28 CERDIP*	1	50
MX674ATQ	28 CERDIP*	¾	25
MX674AUQ	28 CERDIP*	¾	12
MX674ASD	28 Ceramic SB	1	50
MX674ATD	28 Ceramic SB	¾	25
MX674AUD	28 Ceramic SB	¾	12
25µs Maximum Conversion Time			
TEMP RANGE: 0°C to +70°C			
MX574AJN+	28 Plastic DIP	1	50
MX574AKN+	28 Plastic DIP	½	27
MX574ALN+	28 Plastic DIP	½	10
MX574AJCWI+	28 Wide SO	1	50
MX574AKCWI+	28 Wide SO	½	27
MX574ALCWI+	28 Wide SO	½	10
MX574AJP+	28 PLCC	1	50
MX574AKP+	28 PLCC	½	27
MX574ALP+	28 PLCC	½	10
MX574AK/D	Dice*	½	—
TEMP RANGE: -40°C to +85°C			
MX574AJEPI+	28 Plastic DIP	1	75
MX574AKEPI+	28 Plastic DIP	½	38
MX574ALEPI+	28 Plastic DIP	½	19
MX574AJEWI+	28 Wide SO	1	75
MX574AKEWI+	28 Wide SO	½	38
MX574ALEWI+	28 Wide SO	½	19
TEMP RANGE: -55°C to +125°C			
MX574ASQ	28 CERDIP*	1	50
MX574ATQ	28 CERDIP*	¾	25
MX574AUQ	28 CERDIP*	¾	12
MX574ASD	28 Ceramic SB	1	50
MX574ATD	28 Ceramic SB	¾	25
MX574AUD	28 Ceramic SB	¾	12

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Maxim reserves the right to ship Ceramic SB in lieu of CERDIP packages.*
***Consult factory for dice specifications.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 PDIP	P28+2	21-0044	—
28 PLCC	Q28+3	21-0049	90-0235
28 Wide SO	W28+2	21-0042	90-0109

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/90	Initial release	—
1	8/11	Updated the *Electrical Characteristics* and *Ordering Information*. Added *Revision History*.	2–4

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