阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

8-Bit, CMOS R2R D/A Converter

The HI3338 family are CMOS high speed R2R voltage output digital-to-analog converters. They can operate from a single +5V supply, at video speeds, and can produce “rail-to-rail” output swings. Internal level shifters and a pin for an optional second supply provide for an output range below digital ground.

The data complement control allows the inversion of input data while the latch enable control provides either feedthrough or latched operation. Both ends of the R2R ladder network are available externally and may be modulated for gain or offset adjustments. In addition, “glitch” energy has been kept very low by segmenting and thermometer encoding of the upper 3 bits.

The HI3338 is manufactured to give low dynamic power dissipation, low output capacitance, and inherent latch-up resistance.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI3338KIB	-40 to 85	16 Ld SOIC	M16.3
HI3338KIBZ (Note)	-40 to 85	16 Ld SOIC (Pb-free)	M16.3

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

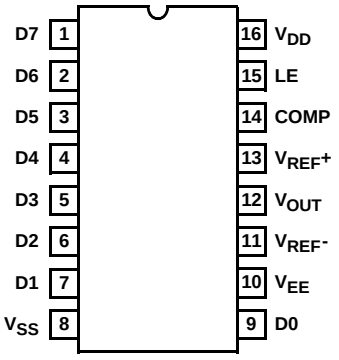
- CMOS Low Power (Typ) 100mW
- R2R Output, Segmented for Low “Glitch”
- CMOS/TTL Compatible Inputs
- Fast Settling (Typ) . . . . . 20ns to $^1/_2$ LSB
- Feedthrough Latch for Clocked or Unclocked Use
- Accuracy (Typ) . . . . . ±0.5 LSB
- Data Complement Control
- High Update Rate (Typ) 50MHz
- Unipolar or Bipolar Operation
- Linearity (INL)
  - HI3338KIB . . . . . ±0.75 LSB
- Pb-free Available

Applications

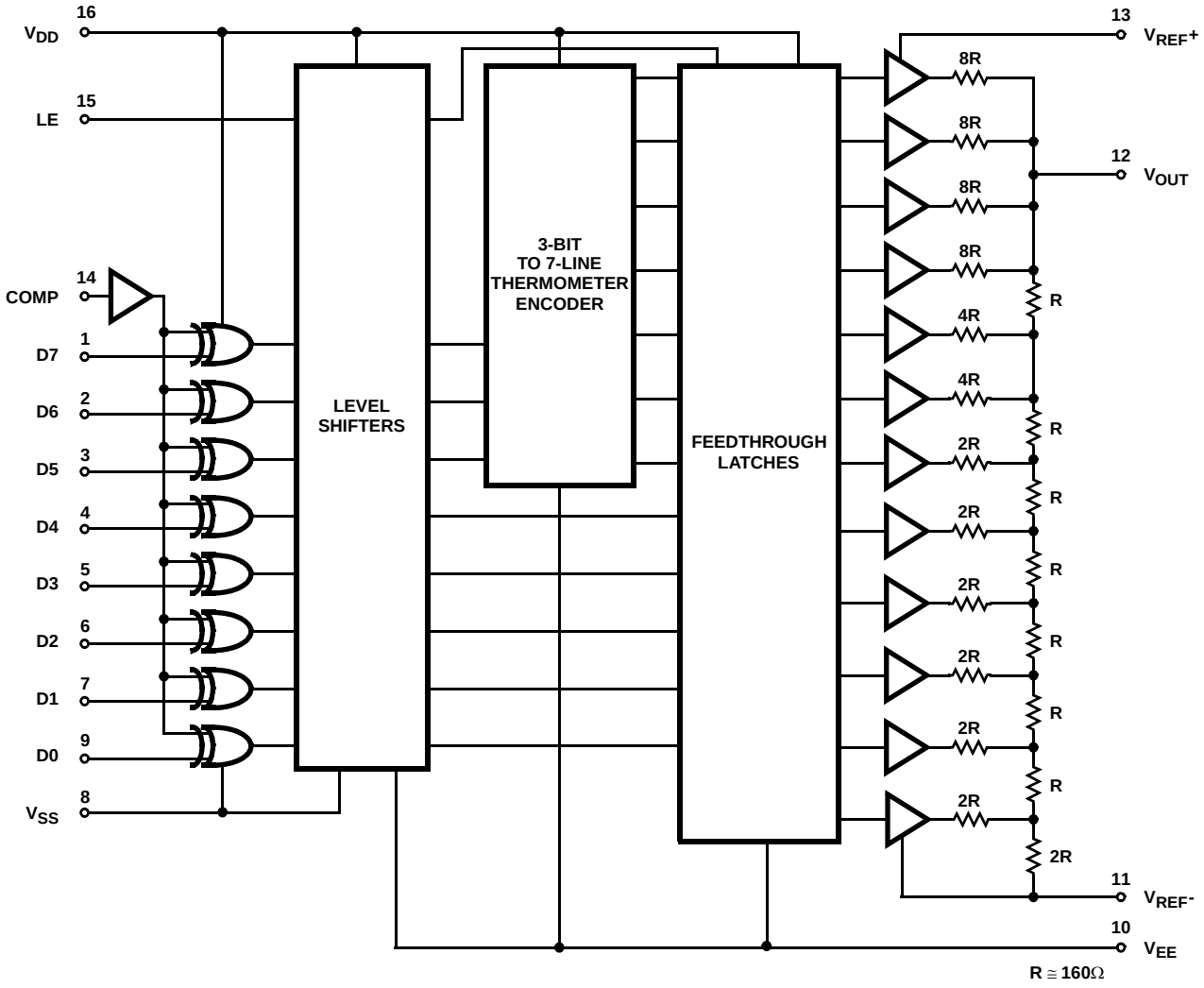
- TV/Video Display
- High Speed Oscilloscope Display
- Digital Waveform Generator
- Direct Digital Frequency Synthesis
- Wireless Communication

Pinout

HI3338 (SOIC)
TOP VIEW



Functional Diagram



Die Characteristics

DIE DIMENSIONS:

2,740µm x 3,310µm x 530 ±50µm

METALLIZATION:

Type: Al with 0.8% Si
Thickness: 11kÅ ±1kÅ

GLASSIVATION:

Type: 3% PSG
Thickness: 13kÅ ±2.6kÅ

Absolute Maximum Ratings

DC Supply-Voltage Range . . . . . -0.5V to +8V
(V_{DD} - V_{SS} or V_{DD} - V_{EE}, Whichever Is Greater)
Input Voltage Range
Digital Inputs (LE, COMP D0 - D7). . . . V_{SS} - 0.5V to V_{DD} + 0.5V
Analog Pins (V_{REF}+, V_{REF}-, V_{OUT}) . . . . V_{DD} - 8V to V_{DD} + 0.5V
DC Input Current
Digital Inputs (LE, COMP, D0 - D7) . . . . . ±20mA
Recommended Supply Voltage Range . . . . . 4.5V to 7.5V

Thermal Information

Thermal Resistance (Typical) θ_{JA} (^{O}C/W)
SOIC Package 100
Maximum Junction Temperature . . . . . 150^{O}C
Maximum Storage Temperature Range, T_{STG} . . . . -65^{O}C to 150^{O}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{O}C
(Lead Tips Only)

Operating Conditions

HI3338KIB . . . . . -40^{O}C to 85^{O}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = 25^{O}C, V_{DD} = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{EE} = V_{REF}- = GND, LE clocked at 20MHz, $R_L \geq 1M\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		8	-	-	Bits
Integral Linearity Error	See Figure 4	-	-	±0.75	LSB
Differential Linearity Error	See Figure 4	-	-	±0.5	LSB
Gain Error	Input Code = FF_{HEX}, See Figure 3	-	-	±0.5	LSB
Offset Error	Input Code = 00_{HEX}, See Figure 3	-	-	±0.25	LSB
DIGITAL INPUT TIMING					
Update Rate	To Maintain $^1/_2$ LSB Settling	DC	50	-	MHz
Update Rate	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	DC	20	-	MHz
Set Up Time t_{SU1}	For Low Glitch	-	-2	-	ns
Set Up Time t_{SU2}	For Data Store	-	8	-	ns
Hold Time t_H	For Data Store	-	5	-	ns
Latch Pulse Width t_W	For Data Store	-	5	-	ns
Latch Pulse Width t_W	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	-	25	-	ns
OUTPUT PARAMETERS	R_L Adjusted for $1V_{P-P}$ Output				
Output Delay t_{D1}	From LE Edge	-	25	-	ns
Output Delay t_{D2}	From Data Changing	-	22	-	ns
Rise Time t_r	10% to 90% of Output	-	4	-	ns
Settling Time t_S	10% to Settling to $^1/_2$ LSB	-	20	-	ns
Output Impedance	V_{REF}+ = 6V, V_{DD} = 6V	120	160	200	Ω
Glitch Area		-	150	-	pV-s
Glitch Area	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	-	250	-	pV-s
REFERENCE VOLTAGE					
V_{REF}+ Range	(+) Full Scale (Note 1)	V_{REF}- + 3	-	V_{DD}	V
V_{REF}- Range	(-) Full Scale (Note 1)	V_{EE}	-	V_{REF}+ - 3	V
V_{REF}+ Input Current	V_{REF}+ = 6V, V_{DD} = 6V	-	40	50	mA

Electrical Specifications $T_A = 25^oC$, $V_{DD} = 5V$, $V_{REF}+ = 4.608V$, $V_{SS} = V_{EE} = V_{REF}- = GND$, LE clocked at 20MHz, $R_L \geq 1M\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE					
Static I_{DD} or I_{EE}	LE = Low, D0 - D7 = High	-	100	220	µA
	LE = Low, D0 - D7 = Low	-	-	100	µA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10MHz, 0V to 5V Square Wave	-	20	-	mA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10MHz, ±2.5V Square Wave	-	25	-	mA
V_{DD} Rejection	50kHz Sine Wave Applied	-	3	-	mV/V
V_{EE} Rejection	50kHz Sine Wave Applied	-	1	-	mV/V
DIGITAL INPUTS D0 - D7, LE, COMP					
High Level Input Voltage	Note 1	2	-	-	V
Low Level Input Voltage	Note 1	-	-	0.8	V
Leakage Current		-	±1	±5	µA
Capacitance		-	5	-	pF
TEMPERATURE COEFFICIENTS					
Output Impedance		-	200	-	ppm/×^oC

NOTE:

1. Parameter not tested, but guaranteed by design or characterization.

Timing Diagrams

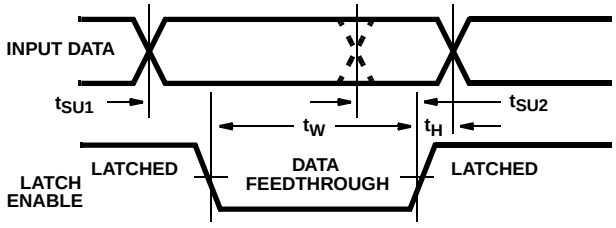


FIGURE 1. DATA TO LATCH ENABLE TIMING

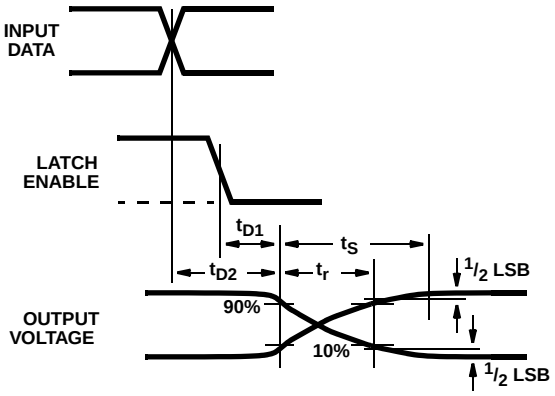


FIGURE 2. DATA AND LATCH ENABLE TO OUTPUT TIMING

Pin Descriptions

PIN	NAME	DESCRIPTION
1	D7	Most Significant Bit
2	D6	Input
3	D5	Data
4	D4	Bits
5	D3	(High = True)
6	D2	
7	D1	
8	V_{SS}	Digital Ground
9	D0	Least Significant Bit. Input Data Bit
10	V_{EE}	Analog Ground
11	V_{REF}-	Reference Voltage Negative Input
12	V_{OUT}	Analog Output
13	V_{REF}+	Reference Voltage Positive Input
14	COMP	Data Complement Control input. Active High
15	LE	Latch Enable Input. Active Low
16	V_{DD}	Digital Power Supply, +5V

Digital Signal Path

The digital inputs (LE, COMP, and D0 - D7) are of TTL compatible HCT High Speed CMOS design: the loading is essentially capacitive and the logic threshold is typically 1.5V.

The 8 data bits, D0 (weighted 2^0) through D7 (weighted 2^7), are applied to Exclusive OR gates (see Functional Diagram). The COMP (data complement) control provides the second input to the gates: if COMP is high, the data bits will be inverted as they pass through.

The input data and the LE (latch enable) signals are next applied to a level shifter. The inputs, operating between the levels of V_{DD} and V_{SS}, are shifted to operate between V_{DD} and V_{EE}. V_{EE} optionally at ground or at a negative voltage, will be discussed under bipolar operation. All further logic elements except the output drivers operate from the V_{DD} and V_{EE} supplies.

The upper 3 bits of data, D5 through D7, are input to a 3-to-7 line bar graph encoder. The encoder outputs and D0 through D4 are applied to a feedthrough latch, which is controlled by LE (latch enable).

Latch Operation

Data is fed from input to output while LE is low: LE should be tied low for non-clocked operation.

Non-clocked operation or changing data while LE is low is not recommended for applications requiring low output “glitch” energy: there is no guarantee of the simultaneous changing of input data or the equal propagation delay of all bits through the converter. Several parameters are given if the converter is to be used in either of these modes: t_{D2} gives the delay from the input changing to the output changing (10%), while t_{SU2} and t_H give the set up and hold times (referred to LE rising edge) needed to latch data. See Figures 1 and 2.

Clocked operation is needed for low “glitch” energy use. Data must meet the given t_{SU1} set up time to the LE falling edge, and the t_H hold time from the LE rising edge. The delay to the output changing, t_{D1}, is now referred to the LE falling edge.

There is no need for a square wave LE clock; LE must only meet the minimum t_W pulse width for successful latch operation. Generally, output timing (desired accuracy of settling) sets the upper limit of usable clock frequency.

Output Structure

The latches feed data to a row of high current CMOS drivers, which in turn feed a modified R2R ladder network.

The “N” channel (pull down) transistor of each driver plus the bottom “2R” resistor are returned to V_{REF}- this is the (-) full-scale reference. The “P” channel (pull up) transistor of each driver is returned to V_{REF}+, the (+) full-scale reference.

In unipolar operation, V_{REF}- would typically be returned to analog ground, but may be raised above ground (see specifications). There is substantial code dependent current that flows from V_{REF}+ to V_{REF}- (see V_{REF}+ input current in specifications), so V_{REF}- should have a low impedance path to ground.

In bipolar operation, V_{REF}- would be returned to a negative voltage (the maximum voltage rating to V_{DD} must be observed). V_{EE}, which supplies the gate potential for the output drivers, must be returned to a point at least as negative as V_{REF}-. Note that the maximum clocking speed decreases when the bipolar mode is used.

Static Characteristics

The ideal 8-bit D/A would have an output equal to V_{REF}- with an input code of 00_{HEX} (zero scale output), and an output equal to 255/256 of V_{REF}+ (referred to V_{REF}-) with an input code of FF_{HEX} (full scale output). The difference between the ideal and actual values of these two parameters are the OFFSET and GAIN errors, respectively; see Figure 3.

If the code into an 8-bit D/A is changed by 1 count, the output should change by 1/255 (full-scale output-zero scale output). A deviation from this step size is a differential linearity error, see Figure 4. Note that the error is expressed in fractions of the ideal step size (usually called an LSB). Also note that if the (-) differential linearity error is less (in absolute numbers) than 1 LSB, the device is monotonic. (The output will always increase for increasing code or decrease for decreasing code).

If the code into an 8-bit D/A is at any value, say “N”, the output voltage should be N/255 of the full-scale output (referred to the zero-scale output). Any deviation from that output is an integral linearity error, usually expressed in LSBs. See Figure 4.

Note that OFFSET and GAIN errors do not affect integral linearity, as the linearity is referenced to actual zero and full scale outputs, not ideal. Absolute accuracy would have to also take these errors into account.

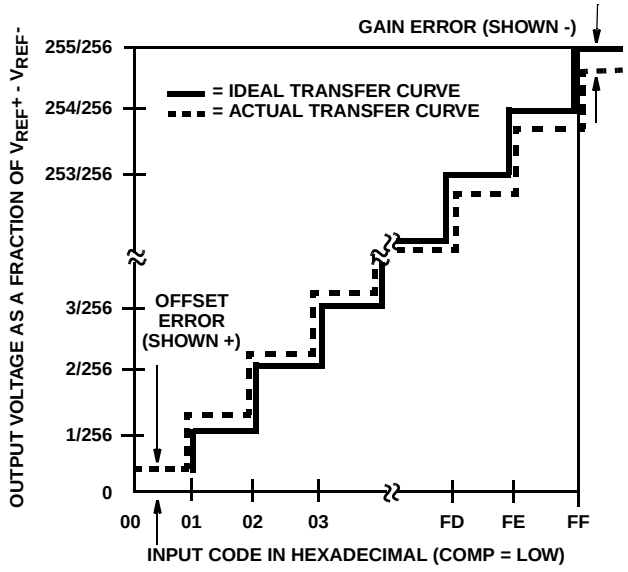


FIGURE 3. D/A OFFSET AND GAIN ERROR

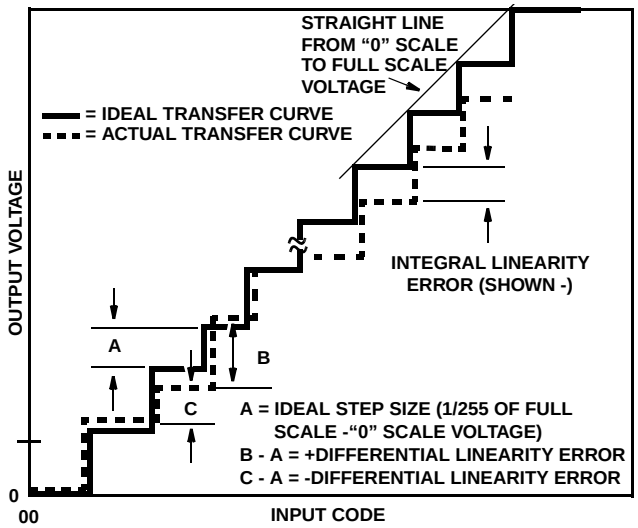


FIGURE 4. D/A INTEGRAL AND DIFFERENTIAL LINEARITY

Dynamic Characteristics

Keeping the full-scale range ($V_{REF}+ - V_{REF}-$) as high as possible gives the best linearity and lowest “glitch” energy (referred to 1V). This provides the best “P” and “N” channel gate drives (hence saturation resistance) and propagation delays. The $V_{REF}+$ (and $V_{REF}-$ if bipolar) terminal should be well bypassed as near the chip as possible.

“Glitch” energy is defined as a spurious voltage that occurs as the output is changed from one voltage to another. In a binary input converter, it is usually highest at the most significant bit transition ($7F_{HEX}$ to 80_{HEX} for an 8-bit device), and can be measured by displaying the output as the input code alternates around that point. The “glitch” energy is the area between the actual output display and an ideal one LSB step voltage (subtracting negative area from positive), at either the positive or negative-going step. It is usually expressed in pV-s.

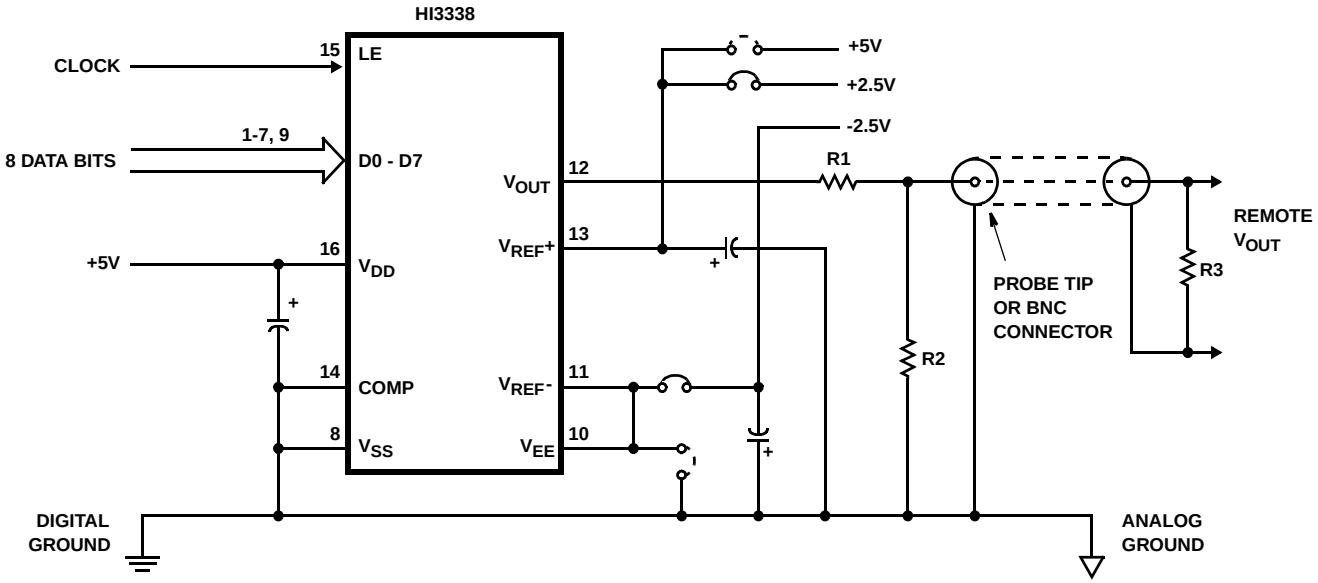
The HI3338 uses a modified R2R ladder, where the 3 most significant bits drive a bar graph decoder and 7 equally weighted resistors. This makes the “glitch” energy at each $^1/_8$ scale transition ($1F_{HEX}$ to 20_{HEX}, $3F_{HEX}$ to 40_{HEX}, etc.) essentially equal, and far less than the MSB transition would otherwise display.

For the purpose of comparison to other converters, the output should be resistively divided to 1V full scale. Figure 5 shows a typical hook-up for checking “glitch” energy or settling time.

The settling time of the A/D is mainly a function of the output resistance (approximately 160Ω in parallel with the load resistance) and the load plus internal chip capacitance. Both “glitch” energy and settling time measurements require very good circuit and probe grounding: a probe tip connector such as Tektronix part number 131-0258-00 is recommended.

TABLE 1. OUTPUT VOLTAGE vs INPUT CODE AND V_{REF}

$V_{REF}+$ $V_{REF}-$ STEP SIZE	5.12V 0 0.0200V	5.00V 0 0.0195V	4.608V 0 0.0180V	2.56V -2.56V 0.0200V	2.50V -2.50V 0.0195V
Input Code					
$11111112 = FF_{HEX}$	5.1000V	4.9805V	4.5900V	2.5400V	2.4805V
$11111102 = FE_{HEX}$	5.0800	4.9610	4.5720	2.5200	2.4610
• • •					
$10000001_2 = 81_{HEX}$	2.5800	2.5195	2.3220	0.0200	0.0195
$10000000_2 = 80_{HEX}$	2.5600	2.5000	2.3040	0.0000	0.0000
$01111111_2 = 7F_{HEX}$	2.5400	2.4805	2.2860	- 0.0200	-0.0195
• • •					
$00000001_2 = 01_{HEX}$	0.0200	0.0195	0.0180	-2.5400	-2.4805
$00000000_2 = 00_{HEX}$	0.0000	0.0000	0.0000	-2.5600	-2.5000

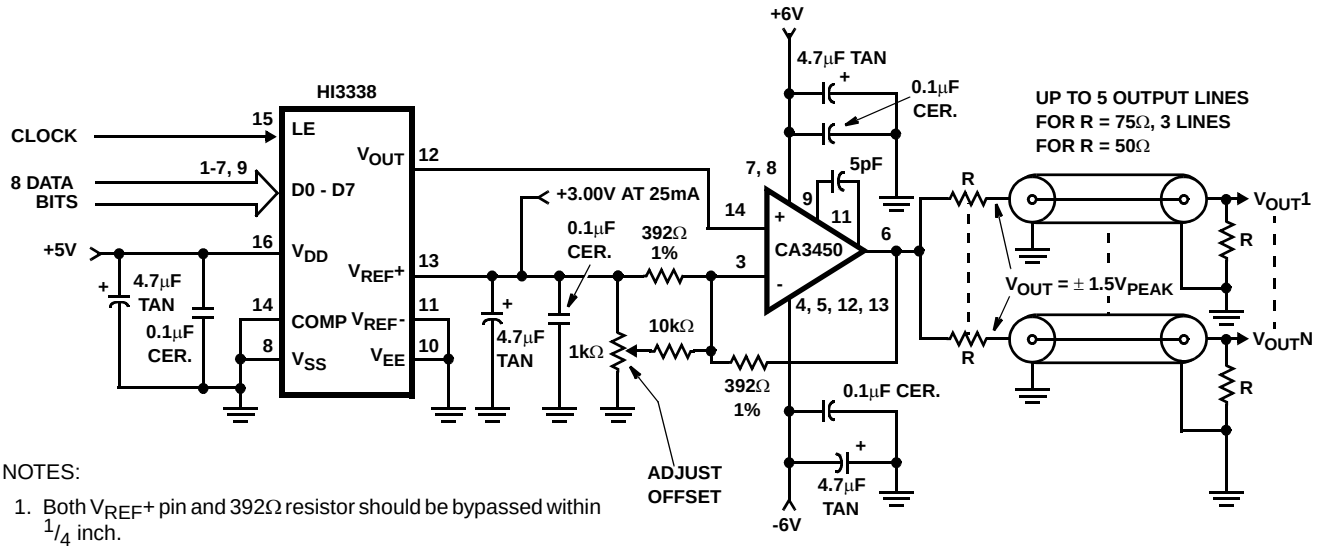


FUNCTION	CONNECTOR	R1	R2	R3	$V_{OUT(P-P)}$
Oscilloscope Display	Probe Tip	82Ω	62Ω	N/C	1V
Match 93Ω Cable	BNC	75	160	93	1V
Match 75Ω Cable	BNC	18	130	75	1V
Match 50Ω Cable	BNC	Short	75	50	0.79V

NOTES:

2. $V_{OUT(P-P)}$ is approximate, and will vary as R_{OUT} of D/A varies.
3. All drawn capacitors are 0.1μF multilayer ceramic/4.7μF tantalum.
4. Dashed connections are for unipolar operation. Solid connection are for bipolar operation.

FIGURE 5. HI3338 DYNAMIC TEST CIRCUIT



NOTES:

1. Both $V_{REF}+$ pin and 392Ω resistor should be bypassed within $^1/_4$ inch.
2. Keep nodal capacitance at CA3450 pin 3 as low as possible.
3. V_{OUT} Range = ±3V at CA3450.

FIGURE 6. HI3338 AND CA3450 FOR DRIVING MULTIPLE COAXIAL LINES

Applications

The output of the HI3338 can be resistively divided to match a doubly terminated 50Ω or 75Ω line, although peak-to-peak swings of less than 1V may result. The output magnitude will also vary with the converter's output impedance. Figure 5 shows such an application. Note that because of the HCT input structure, the HI3338 could be operated up to +7.5V V_{DD} and $V_{REF}+$ supplies and still accept 0V to 5V CMOS input voltages.

If larger voltage swings or better accuracy is desired, a high speed output buffer, such as the HA-5033, HA-2542, or CA3450, can be employed. Figure 6 shows a typical application, with the output capable of driving ±2V into multiple 50Ω terminated lines.

Operating and Handling Considerations

HANDLING

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. “Guide to Better Handling and Operation of CMOS Integrated Circuits.”

OPERATING

OPERATING VOLTAGE

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the absolute maximum ratings to be exceeded.

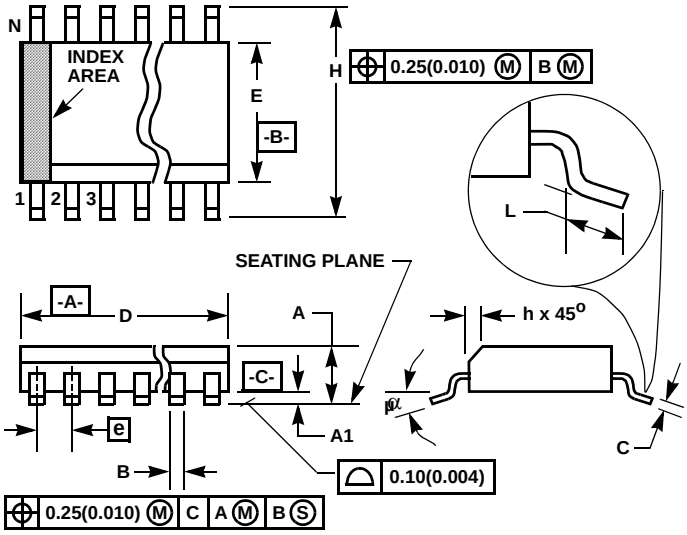
INPUT SIGNALS

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off.

UNUSED INPUTS

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or GND, whichever is appropriate.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93