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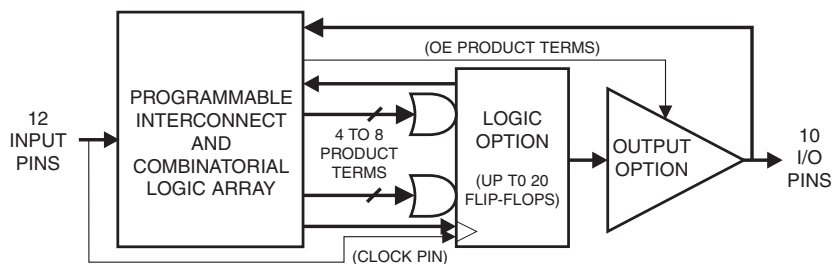
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Features

- 3.0V to 5.5V Operating Range
- Advanced, High-speed, Electrically-erasable Programmable Logic Device
 - Superset of 22V10
 - Enhanced Logic Flexibility
 - Architecturally Compatible with ATV750B and ATV750 Software and Hardware
- D- or T-type Flip-flop
- Product Term or Direct Input Pin Clocking
- 10 ns Maximum Pin-to-pin Delay with 5V Operation
- 15 ns Maximum Pin-to-pin Delay with 3V Operation
- Highest Density Programmable Logic Available in 24-pin Package
 - Advanced Electrically-erasable Technology
 - Reprogrammable
 - 100% Tested
- Increased Logic Flexibility
 - 42 Array Inputs, 20 Sum Terms and 20 Flip-flops
- Enhanced Output Logic Flexibility
 - All 20 Flip-flops Feed Back Internally
 - 10 Flip-flops are also Available as Outputs
- Programmable Pin-keeper Circuits
- Dual-in-line and Surface Mount Package in Standard Pinouts
- Commercial and Industrial Temperature Ranges
- 20-year Data Retention
- 2000V ESD Protection
- 1000 Erase/Write Cycles
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available

1. Block Diagram



2. Description

The Atmel® “750” architecture is twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations translate into more usable gates. High-speed logic and uniform, predictable delays guarantee fast in-system performance. The ATF750LVC is a high-performance CMOS (electrically-erasable) complex programmable logic device (CPLD) that utilizes Atmel’s proven electrically-erasable technology.



**High-speed
Complex
Programmable
Logic Device**

ATF750LVC



4. Absolute Maximum Ratings*

| | |
|----------------------------------------------------------------------------|--------------------------------|
| Temperature Under Bias..... | -40°C to +85°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7V ⁽¹⁾ |
| Voltage on Input Pins with Respect to Ground During Programming..... | -2.0V to +14.0V ⁽¹⁾ |
| Programming Voltage with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |

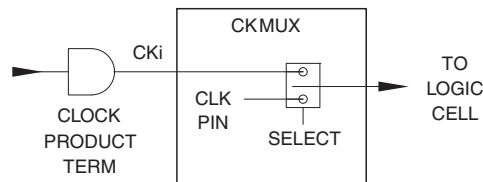
***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7V for pulses of less than 20 ns with V_{CC} at V_{CC} max.

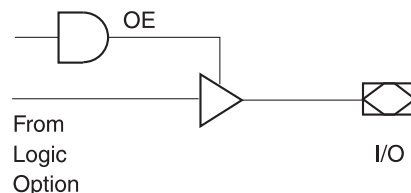
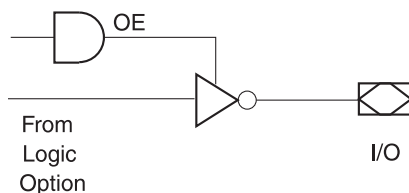
5. DC and AC Operating Conditions

| | Commercial | Industrial |
|---------------------------------|-------------|---------------|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - +85°C |
| V_{CC} Power Supply | 3.0 - 5.25V | 3.0 - 5.5V |

6. Clock Mux



7. Output Options



8. Bus-friendly Pin-keeper Input and I/Os

All input and I/O pins on the ATF750LVC have programmable “pin-keeper” circuits. If activated, when any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

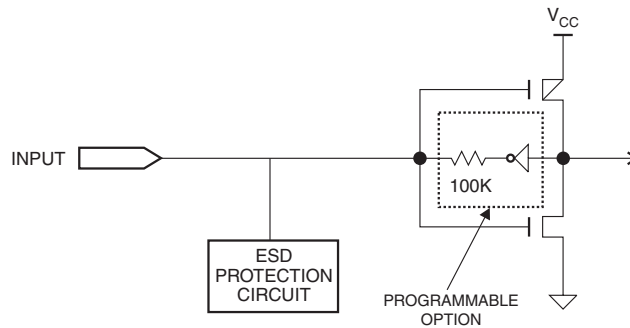
This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Enabling or disabling of the pin-keeper circuits is controlled by the device type chosen in the logic compiler device selection menu. Please refer to the software compiler table for more details. Once the pin-keeper circuits are disabled, normal termination procedures are required for unused inputs and I/Os.

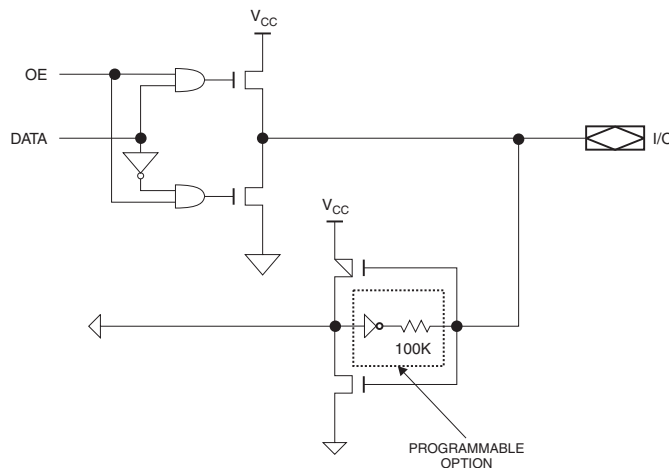
Table 1. Software Compiler Mode Selection

| Synario | WinCupl | Pin-keeper Circuit |
|-----------------|----------|--------------------|
| ATF750LVC | V750C | Disabled |
| ATF750LVC (PPK) | V750CPPK | Enabled |

9. Input Diagram



10. I/O Diagram

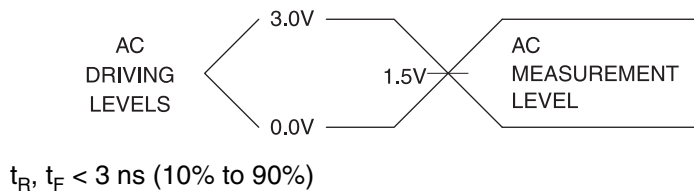


11. DC Characteristics

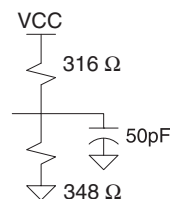
| Symbol | Parameter | Condition | | Min | Typ | Max | Units | |
|-------------------|-------------------------------|------------------------------------------------------|------|-------------------------|------------|-----------------|---------|----|
| V_{CC} | Power Supply Voltage | 3V Operation | | 3.0 | 3.3 | 3.6 | V | |
| | | 5V Operation | Com. | 4.75 | 5.0 | 5.25 | V | |
| | | | Ind. | 4.5 | 5.0 | 5.5 | V | |
| I_{LI} | Input Load Current | $V_{IN} = -0.1V$ to $V_{CC} + 1V$ | | | | 10 | μA | |
| I_{LO} | Output Leakage Current | $V_{OUT} = -0.1V$ to $V_{CC} + 0.1V$ | | | | 10 | μA | |
| I_{CC} | Power Supply Current, Standby | $V_{CC} = 3.6V$ $V_{IN} = 3.6V$ Outputs Open | C-15 | Com. | | 65 | 90 | mA |
| | | | | Ind. | | 70 | 100 | mA |
| I_{CC} | Power Supply Current, Standby | $V_{CC} = 5.25V$ $V_{IN} = 5.25V$ Outputs Open | C-15 | Com. | | 100 | 180 | mA |
| | | | | Ind. | | 110 | 190 | mA |
| $I_{OS}^{(1)(2)}$ | Output Short Circuit Current | $V_{OUT} = 0.5V$ | | | | -120 | mA | |
| V_{IL} | Input Low Voltage | $Min \leq V_{CC} \leq Max$ | | -0.6 | | 0.8 | V | |
| V_{IH} | Input High Voltage | | | 2.0 | | $V_{CC} + 0.75$ | V | |
| V_{OL} | Output Low Voltage | $V_{IN} = V_{IH}$ or V_{IL} , $V_{CC} = Min$ | | $I_{OL} = 16$ mA | Com., Ind. | | 0.5 | V |
| | | | | $I_{OL} = 12$ mA | Mil. | | 0.5 | V |
| | | | | $I_{OL} = 24$ mA | Com. | | 0.8 | V |
| V_{OH} | Output High Voltage | $V_{IN} = V_{IH}$ or V_{IL} , $V_{CC} = Min$ | | $I_{OH} = -100$ μA | | $V_{CC} - 0.3V$ | | V |
| | | | | $I_{OH} = -2.0$ mA | | 2.4 | | V |

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. This test is performed at initial characterisation only.

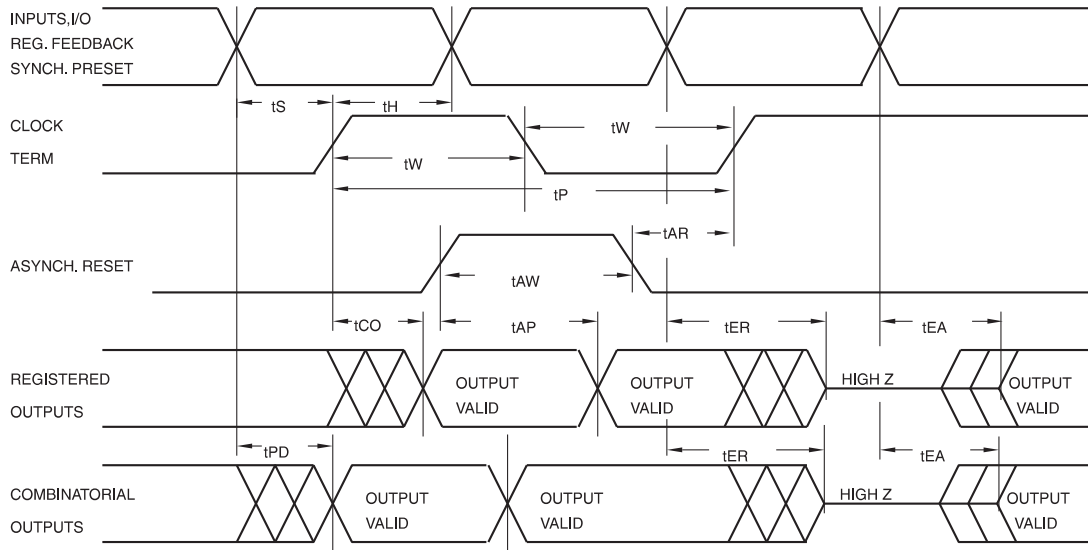
12. Input Test Waveforms and Measurement Levels



13. Output Test Load



14. AC Waveforms, Product Term Clock⁽¹⁾



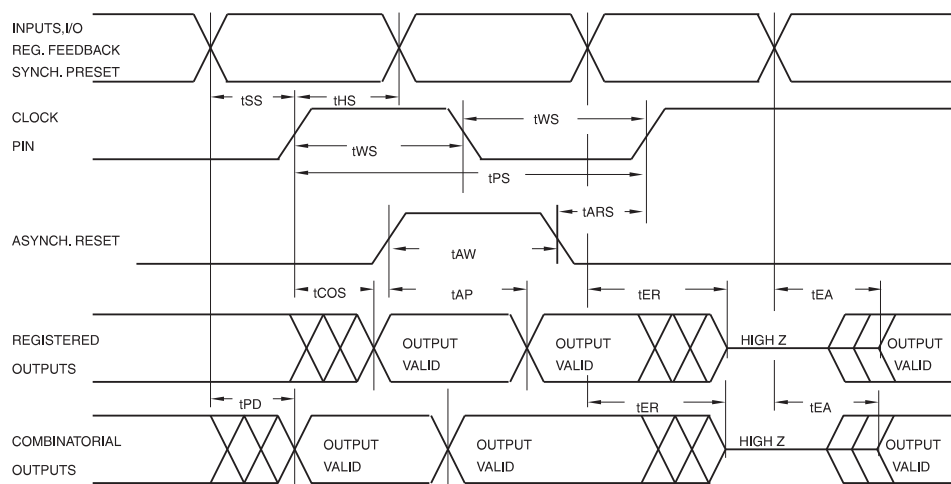
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

15. AC Characteristics, Product Term Clock⁽¹⁾

| Symbol | Parameter | -15 (5V Operation) | | -15 (3V Operation) | | Units |
|-----------|-----------------------------------------------|--------------------|-----|--------------------|-----|-------|
| | | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Non-registered Output | | 10 | | 15 | ns |
| t_{EA} | Input to Output Enable | | 10 | | 15 | ns |
| t_{ER} | Input to Output Disable | | 10 | | 15 | ns |
| t_{CO} | Clock to Output | 4 | 10 | 5 | 12 | ns |
| t_{CF} | Clock to Feedback | 4 | 7.5 | 5 | 9 | ns |
| t_S | Input Setup Time | 4 | | 8 | | ns |
| t_{SF} | Feedback Setup Time | 4 | | 7 | | ns |
| t_H | Hold Time | 2 | | 5 | | ns |
| t_P | Clock Period | 11 | | 14 | | ns |
| t_W | Clock Width | 5.5 | | 7 | | ns |
| f_{MAX} | External Feedback $1/(t_S + t_{CO})$ | | 71 | | 50 | MHz |
| | Internal Feedback $1/(t_{SF} + t_{CF})$ | | 86 | | 62 | MHz |
| | No Feedback $1/(t_P)$ | | 90 | | 71 | MHz |
| t_{AW} | Asynchronous Reset Width | 10 | | 15 | | ns |
| t_{AR} | Asynchronous Reset Recovery Time | 10 | | 15 | | ns |
| t_{AP} | Asynchronous Reset to Registered Output Reset | | 12 | | 15 | ns |
| t_{SP} | Setup Time, Synchronous Preset | 7 | | 8 | | ns |

Note: 1. See ordering information for valid part numbers.

16. AC Waveforms, Input Pin Clock⁽¹⁾

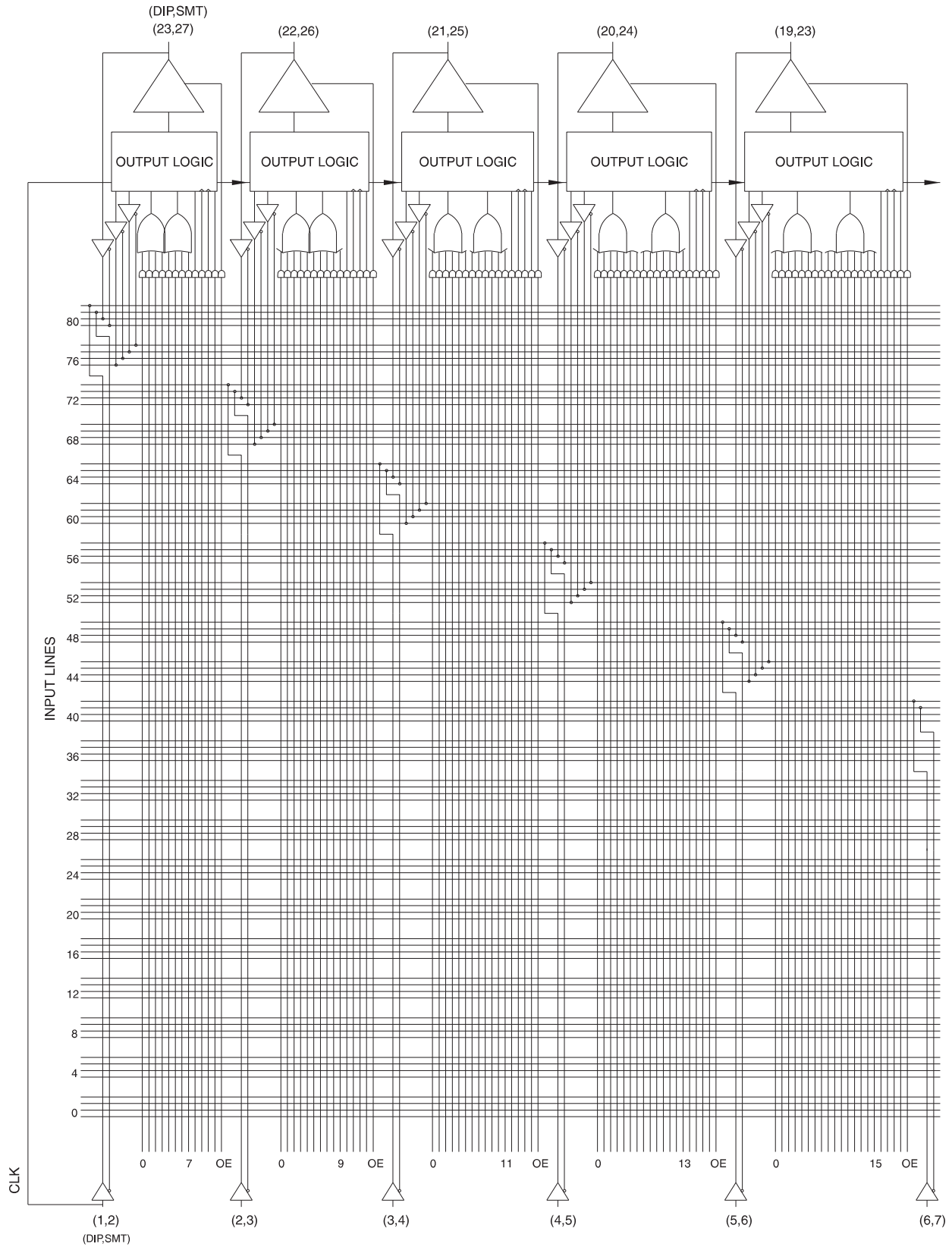


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

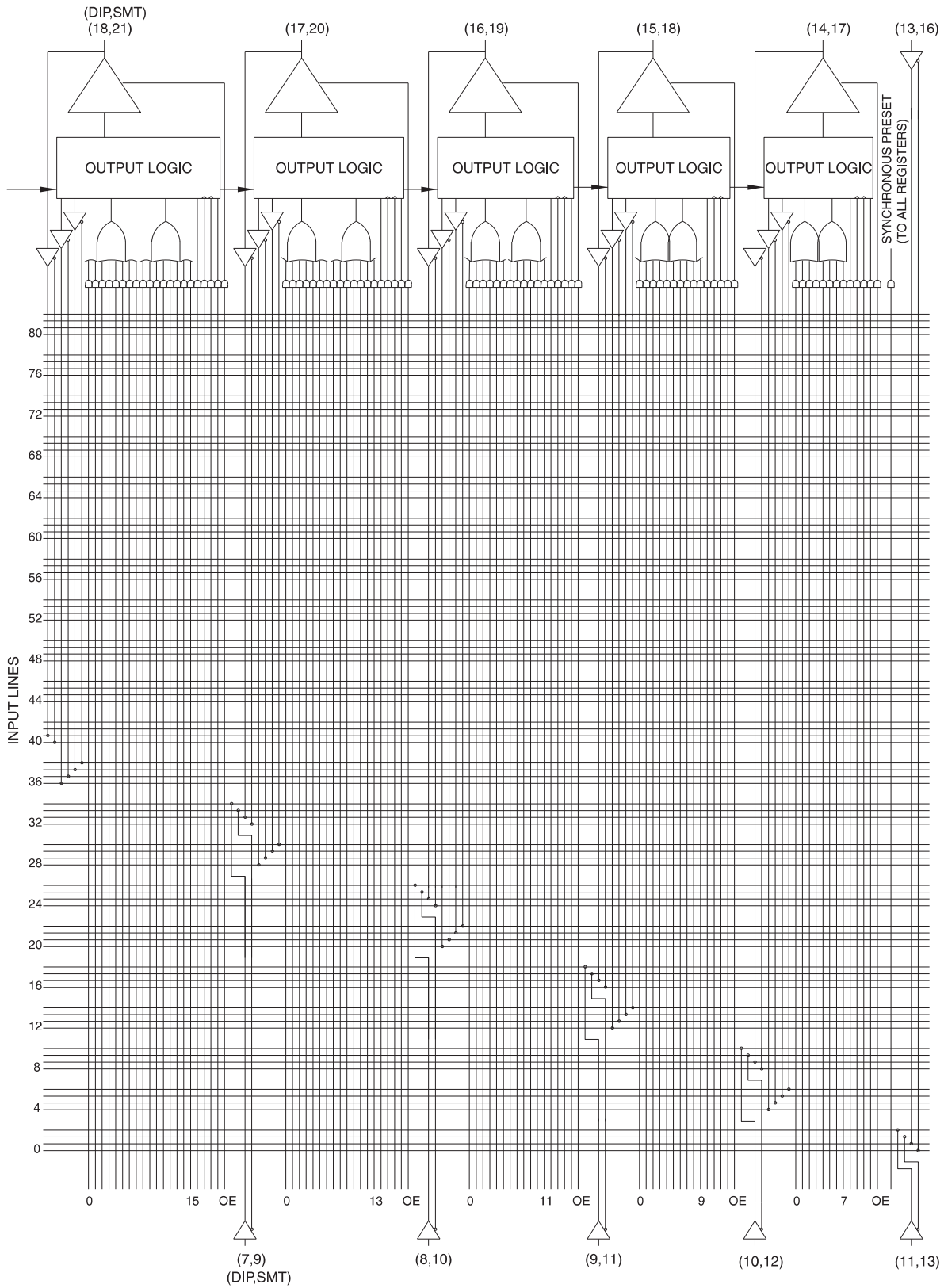
17. AC Characteristics, Input Pin Clock

| Symbol | Parameter | -15 (5V Operation) | | -15 (3V Operation) | | Units |
|------------|-----------------------------------------------|--------------------|-----|--------------------|-----|-------|
| | | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Non-registered Output | | 10 | | 15 | ns |
| t_{EA} | Input to Output Enable | | 10 | | 15 | ns |
| t_{ER} | Input to Output Disable | | 10 | | 15 | ns |
| t_{COS} | Clock to Output | 0 | 7 | 0 | 10 | ns |
| t_{CFS} | Clock to Feedback | 0 | 5 | 0 | 5.5 | ns |
| t_{SS} | Input Setup Time | 5 | | 8 | | ns |
| t_{SFS} | Feedback Setup Time | 5 | | 7 | | ns |
| t_{HS} | Hold Time | 0 | | 5 | | ns |
| t_{PS} | Clock Period | 10 | | 14 | | ns |
| t_{WS} | Clock Width | 5 | | 7 | | ns |
| f_{MAXS} | External Feedback $1/t_{SS} + t_{COS}$ | | 83 | | 55 | MHz |
| | Internal Feedback $1/t_{SFS} + t_{CFS}$ | | 100 | | 80 | MHz |
| | No Feedback $1/t_{PS}$ | | 100 | | 83 | MHz |
| t_{AW} | Asynchronous Reset Width | 10 | | 15 | | ns |
| t_{ARS} | Asynchronous Reset Recovery Time | 10 | | 15 | | ns |
| t_{AP} | Asynchronous Reset to Registered Output Reset | | 10 | | 15 | ns |
| t_{SPS} | Setup Time, Synchronous Preset | 5 | | 11 | | ns |

18. Functional Logic Diagram ATF750LVC, Upper Half



19. Functional Logic Diagram ATF750LVC, Lower Half



20. Using the ATF750LVC's Many Advanced Features

The ATF750LVC's advanced flexibility packs more usable gates into 24-pins than any other logic device. The ATF750LVCs start with the popular 22V10 architecture, and add several enhanced features:

- **Selectable D- and T-type Registers**

Each ATF750LVC flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.

- **Selectable Asynchronous Clocks**

Each of the ATF750LVC's flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.

- **A Full Bank of Ten More Registers**

The ATF750LVC provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.

- **Independent I/O Pin and Feedback Paths**

Each I/O pin on the ATF750LVC has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

21. Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATF750LVC. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

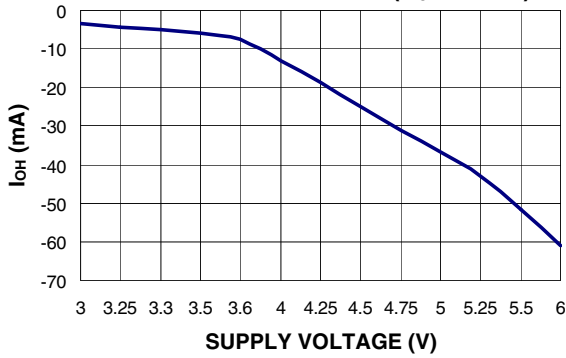
An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

22. Security Fuse Usage

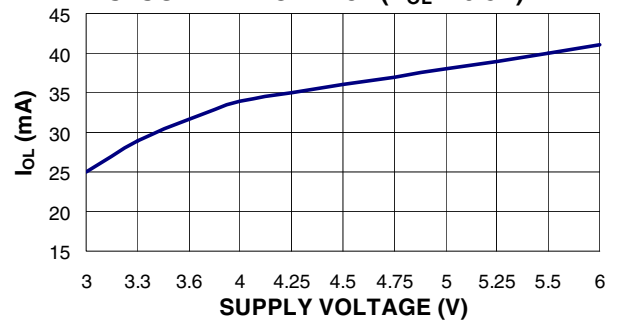
A single fuse is provided to prevent unauthorized copying of the ATF750LVC fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

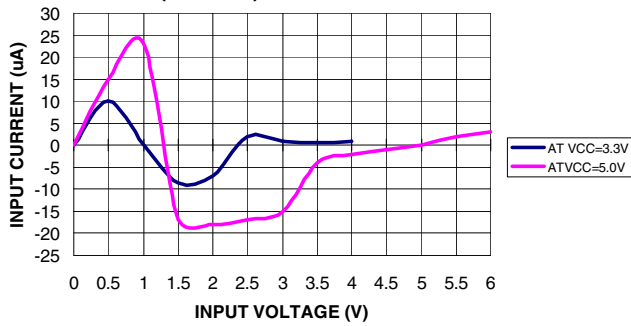
ATF750LVC OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE ($V_{OH} = 2.4V$)



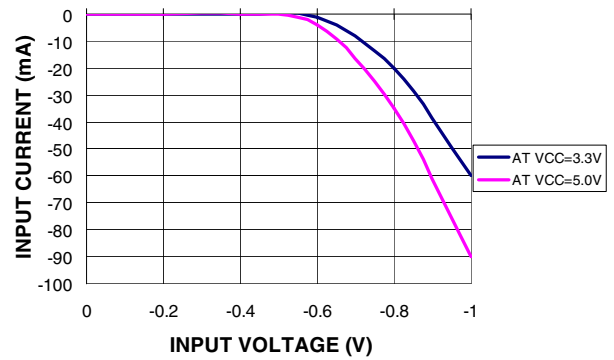
ATF750LVC OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE ($V_{OL} = 0.5V$)



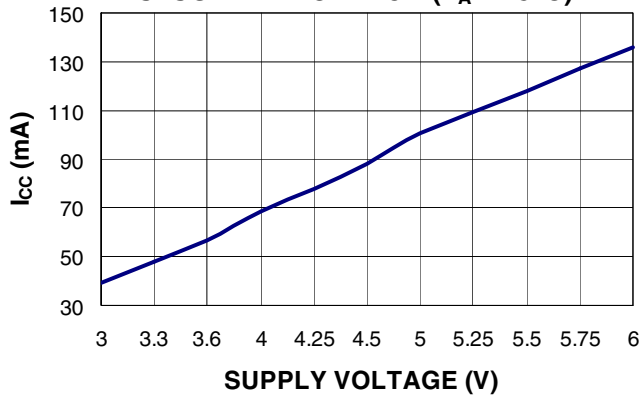
ATF750LVC INPUT CURRENT VS. INPUT VOLTAGE ($T_A = 25^\circ C$) WITH PIN KEEPER



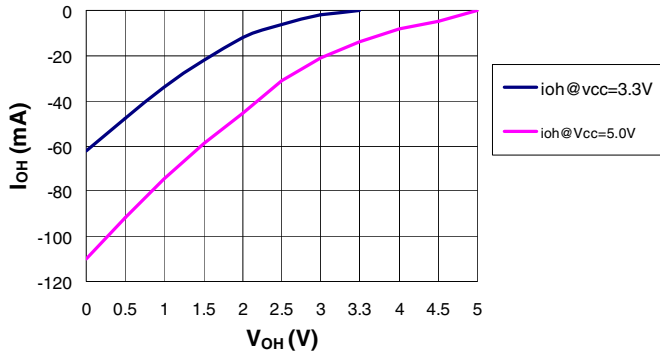
ATF750LVC INPUT CLAMP CURRENT VS. INPUT VOLTAGE ($T_A = 25^\circ C$)



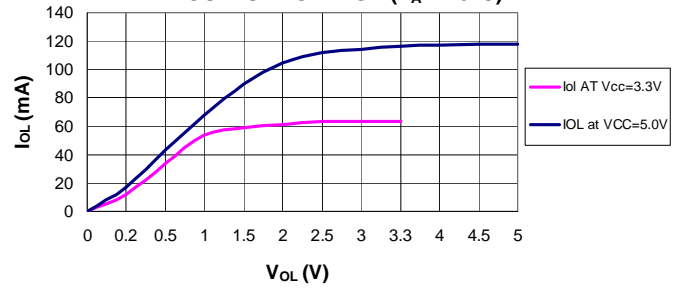
ATF750LVC SUPPLY CURRENT VS. SUPPLY VOLTAGE ($T_A = 25^\circ C$)



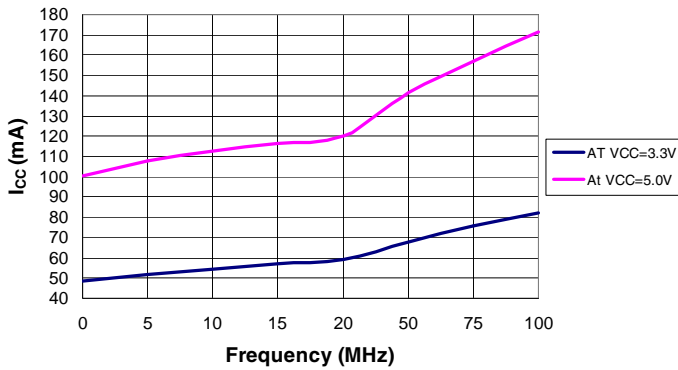
ATF750LVC OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE ($T_A = 25^\circ\text{C}$)



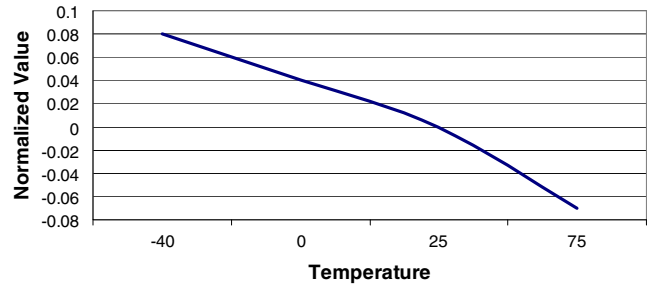
ATF750LVC OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE ($T_A = 25^\circ\text{C}$)



ATF750LVC SUPPLY CURRENT VS. INPUT FREQUENCY ($T_A = 25^\circ\text{C}$)



NORMALIZED SUPPLY CURRENT OVER TEMPERATURE (AT $V_{CC} = 3.3V$ & $5.0V$)



23. ATF750LVC Ordering Information

23.1 ATF750LVC Green Package Options (Pb/Halide-free/RoHS Compliant)

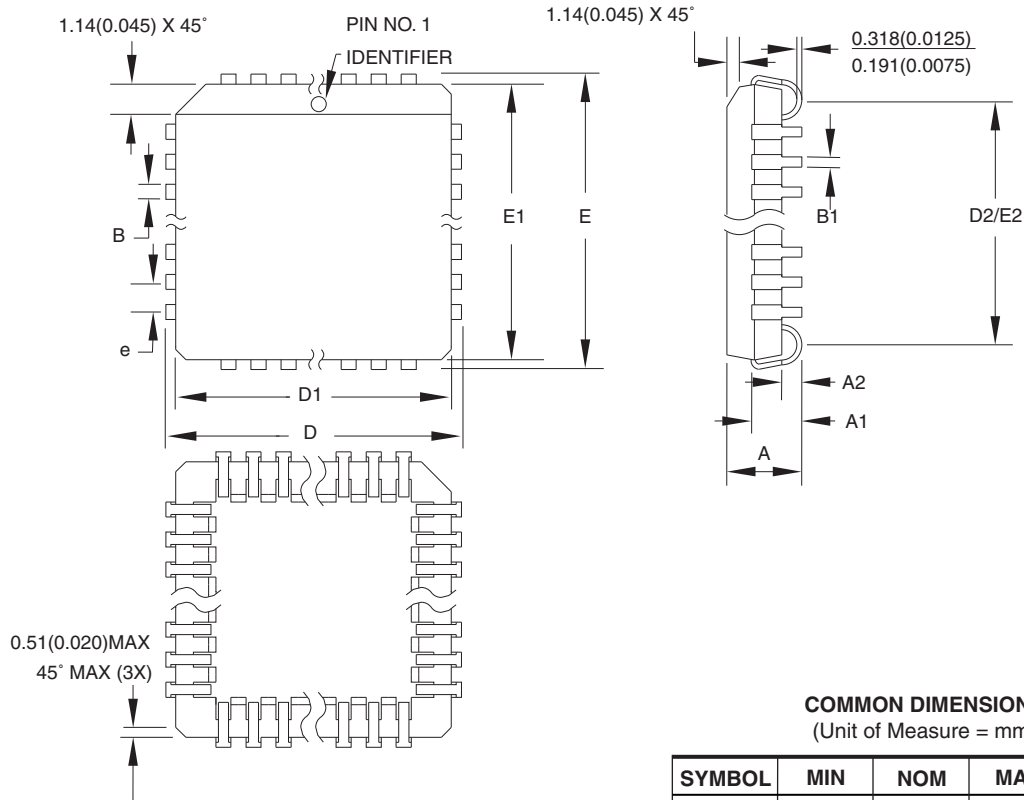
| t_{PD} (ns) | t_{COS} (ns) | Ext. f_{MAXS} (MHz) | Ordering Code | Package | Operation Range |
|------------------|-------------------|--------------------------|-------------------------------------------------------------------------------------|---------------------------|-------------------------------|
| 15 | 10 | 55 | ATF750LVC-15JU ATF750LVC-15PU ATF750LVC-15SU ATF750LVC-15XU ⁽¹⁾ | 28J 24P3 24S 24X | Industrial (-40°C to 85°C) |

Note: 1. Special order only; TSSOP package requires special thermal management.

| Package Type | |
|--------------|--------------------------------------------------------------|
| 28J | 28-Lead, Plastic J-leaded Chip Carrier (PLCC) |
| 24P3 | 24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 24S | 24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| 24X* | 24-lead, 0.173" Wide, Thin Shrink Small Outline (TSSOP) |

24. Package Information

24.1 28J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.430 | – | 11.582 | Note 2 |
| E | 12.319 | – | 12.573 | |
| E1 | 11.430 | – | 11.582 | Note 2 |
| D2/E2 | 9.906 | – | 10.922 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)

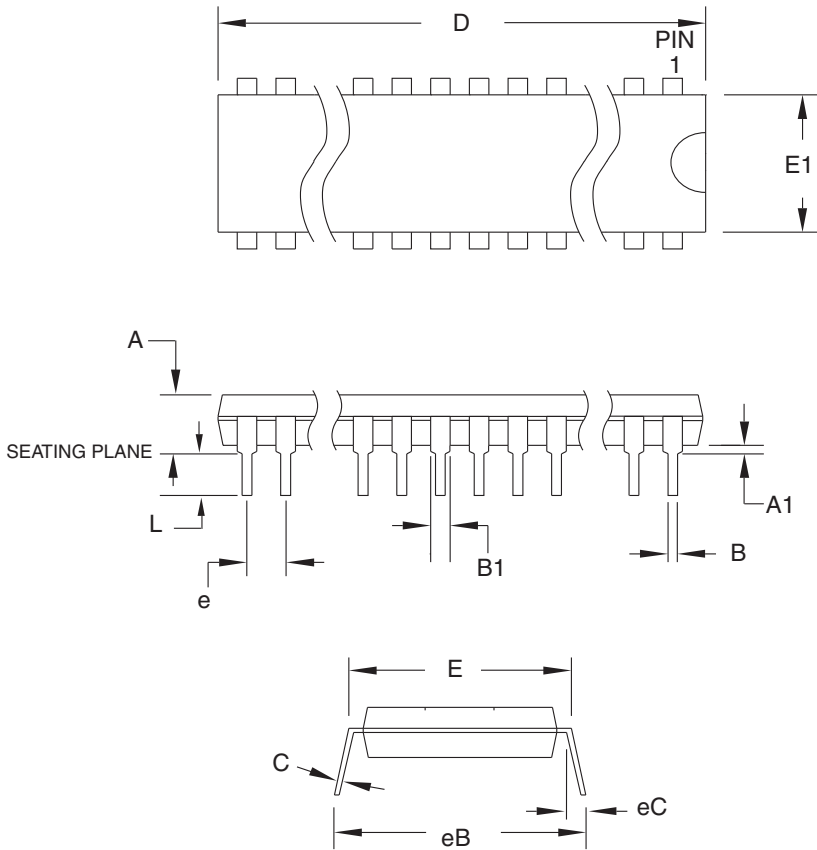
DRAWING NO.

28J

REV.

B

24.2 24P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | - | - | 5.334 | |
| A1 | 0.381 | - | - | |
| D | 31.623 | - | 32.131 | Note 2 |
| E | 7.620 | - | 8.255 | |
| E1 | 6.096 | - | 7.112 | Note 2 |
| B | 0.356 | - | 0.559 | |
| B1 | 1.270 | - | 1.651 | |
| L | 2.921 | - | 3.810 | |
| C | 0.203 | - | 0.356 | |
| eB | - | - | 10.922 | |
| eC | 0.000 | - | 1.524 | |
| e | 2.540 TYP | | | |

- Notes: 1. This package conforms to JEDEC reference MS-001, Variation AF.
 2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

6/1/04



2325 Orchard Parkway
San Jose, CA 95131

TITLE

**24P3, 24-lead (0.300"/7.62 mm Wide) Plastic Dual
Inline Package (PDIP)**

DRAWING NO.

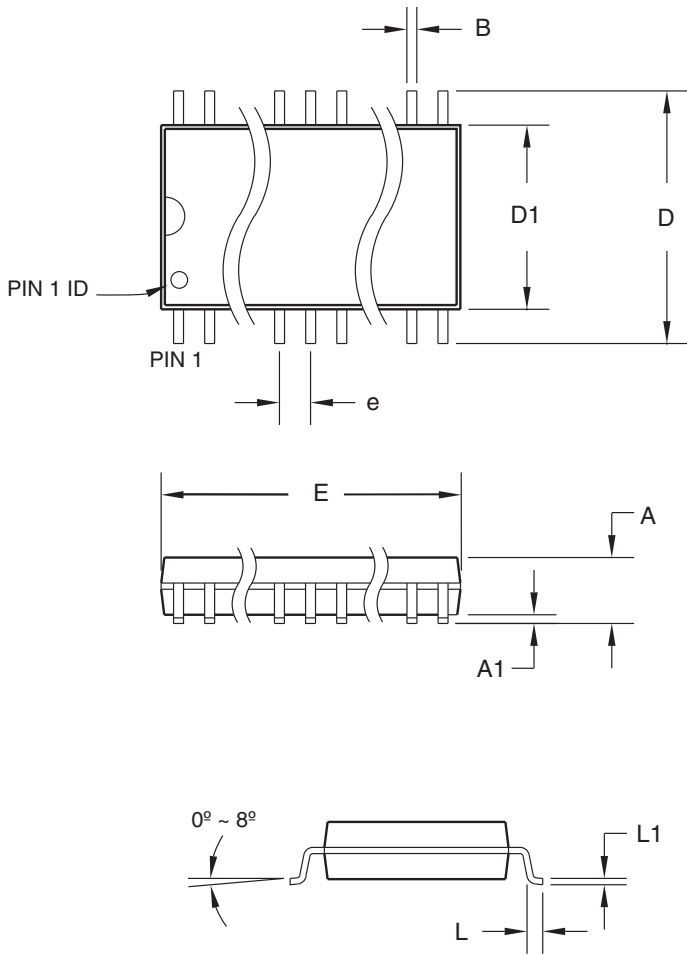
24P3

REV.

D



24.3 24S – SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|-------|------|
| A | – | – | 2.65 | |
| A1 | 0.10 | – | 0.30 | |
| D | 10.00 | – | 10.65 | |
| D1 | 7.40 | – | 7.60 | |
| E | 15.20 | – | 15.60 | |
| B | 0.33 | – | 0.51 | |
| L | 0.40 | – | 1.27 | |
| L1 | 0.23 | – | 0.32 | |
| e | 1.27 BSC | | | |

06/17/2002



2325 Orchard Parkway
San Jose, CA 95131

TITLE

24S, 24-lead (0.300" body) Plastic Gull Wing Small Outline (SOIC)

DRAWING NO.

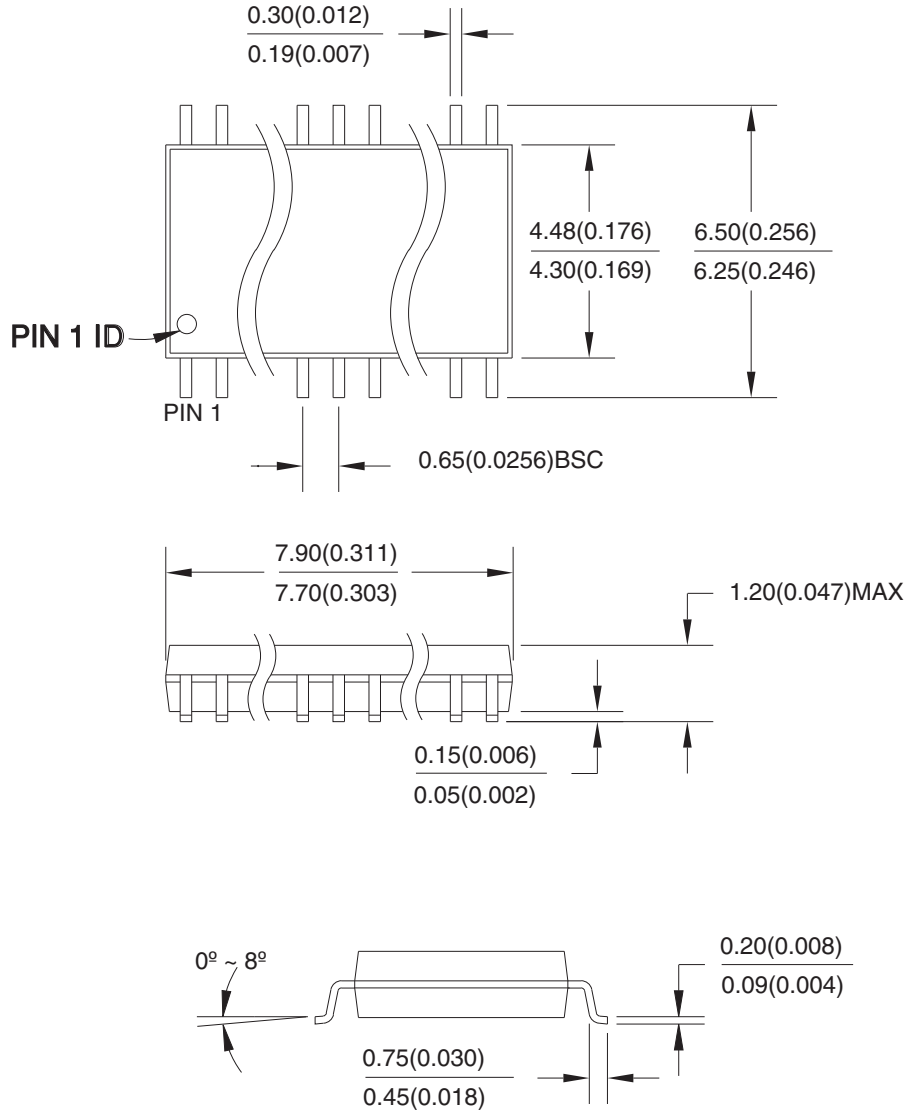
24S

REV.

B

24.4 24X – TSSOP

Dimensions in Millimeter and (Inches)*
 JEDEC STANDARD MO-153 AD
 Controlling dimension: millimeters



04/11/2001



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

24X, 24-lead (4.4 mm body width) Plastic Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.

24X

REV.

A





25. Revision History

| Revision Level – Release Date | History |
|-------------------------------|-----------------------------------------------------------------------------------------------|
| F – November 2008 | Updated datasheet with extended voltage range offering. Removed the leaded parts offering. |





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