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1.0 General Description

BelaSigna 200 is a high-performance, programmable, mixed-signal digital signal processor (DSP) that is based on ON Semiconductor's patented second-generation SignaKlara™ technology.

This single-chip solution is ideally suited for embedded applications where audio performance, low power consumption and miniaturization are critical. BelaSigna 200 targets a wide variety of digital speech- and audio-centric applications, including:

- Communication headsets
- Smart phones
- Personal digital assistants (PDAs)
- Hands-free car kits
- Bluetooth™ wireless technology systems

BelaSigna 200 provides numerous analog and digital interfaces including parallel, serial, synchronous, and asynchronous interfaces to facilitate the connection with transducers from various applications.

BelaSigna 200 contains two primary processing blocks, which all work together to provide a complete audio processing chain. The analog section includes two 16-bit A/D converters and two 16-bit D/A converters. Two on-chip direct digital output stages allow BelaSigna 200 to drive various output transducers directly, eliminating the need for external power amplifiers.

BelaSigna 200 features internal clock generation and power regulation for excellent noise and power performance. Two DSP subsystems operate concurrently: the RCore, which is a fully programmable DSP core, and the weighted overlap-add (WOLA) filterbank coprocessor, which is a dedicated, configurable processor that executes time-frequency domain transforms and other vector-based computations. In addition to these processors, there are several other peripherals, which optimize the architecture to audio processing, such as the onput/output processor (IOP) – an audio-targeted direct memory access (DMA) processor, which runs in the background and manages the data flow between the converters and the two processors. The BelaSigna 200 functional block diagram is shown in Figure 1.

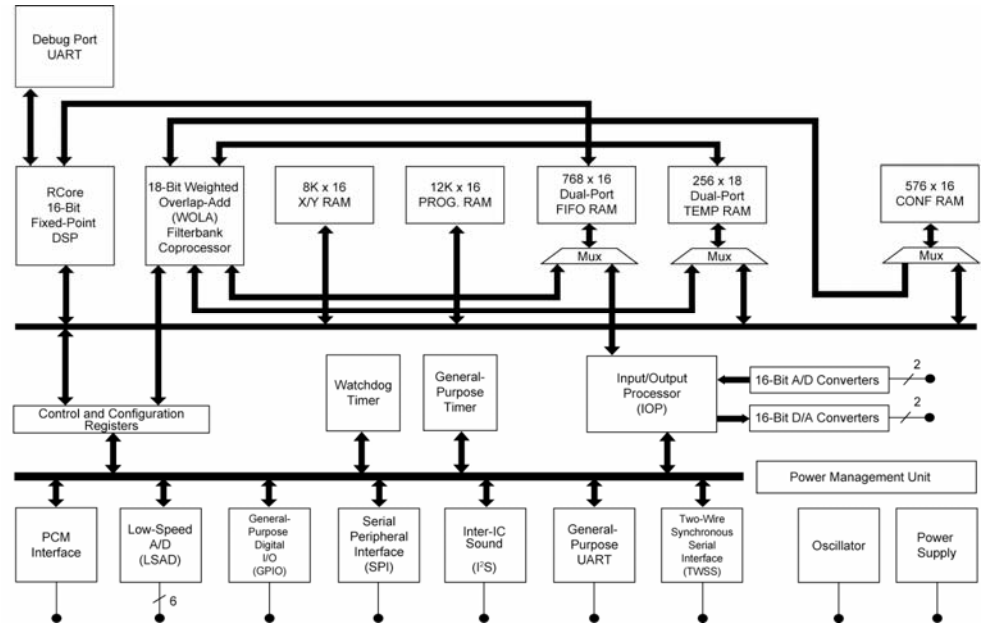


Figure 1: BelaSigna 200 Functional Block Diagram

2.0 Key Features

2.1 System

- 16-bit programmable fixed-point DSP core
- Configurable WOLA filterbank coprocessor optimized for filterbank calculations
- 12-Kword program memory (PRAM)
- Two 4-Kword data memories (XRAM and YRAM)
- Two 384-word dual-port FIFO memories
- Two 128-word dual-port 18-bit memories dedicated to WOLA output results
- 576-word memory dedicated to WOLA gain values, WOLA windows and other configuration data
- Internal oscillator
- Operating voltage of 1.8V nominal
- Ultra-low power: less than 1mW @ 1.28MHz system clock frequency, 1.8V nominal operating voltage, both processors running
- Available in a QFN package; other packages available upon request

2.2 RCore DSP

- Dual-Harvard architecture, 16-bit programmable fixed-point DSP with three execution units
- Single-cycle multiply-accumulate (MAC) with 40-bit accumulator
- Highly parallel instruction set with powerful addressing modes
- Flexible address generation (including modulo addressing) for accessing program memory and data memories, plus control and configuration registers
- Separate system and user stacks with dedicated stack pointers
- Fast normalization and de-normalization operations optimized for signal level calculation and block-floating point calculations
- Supports time-domain pre- and post-processing of input data stream and frequency-domain processing of WOLA output
- Master processor for entire system

2.3 WOLA Filterbank Coprocessor

- Mono and stereo time-frequency transforms providing real or complex data results
- Standard library of overlap-add (OLA) and WOLA filterbank configurations
    - Configurable number of frequency bands
    - Configurable number of frequency bands
    - Configurable oversampling and decimation factors
    - Configurable windows
- Low group delay (< 4ms for 16 bands possible)
- Fast real and complex gain application for magnitude and phase processing
- Block floating-point calculations (4-bit exponent, 18-bit mantissa) to achieve high fidelity
- Maximum digital gain of 90dB possible
- High-fidelity time-frequency domain processing
- Low-overhead interaction with the RCore through shared memories, control registers and interrupts

2.4 Input Output Processor (IOP)

- Block-based DMA for all audio data provides automatic management of input and output FIFOs that reduces processor overhead
- Mono (one in, one out), simple stereo (two in, one out), full stereo (two in, two out) and digital mixed (two in, one out) operating modes
- Interacts with the RCore through interrupts and shared memories
- Normal and smart FIFO audio data accessing schemes available

2.5 Input Stage

- Two separate input channels, each with two multiplexed inputs
- Two configurable preamplifiers for improved input dynamic range matching
- Two analog third-order anti-aliasing filters
- Two 16-bit oversampling ΣΔ A/D converters
- Two ninth-order low-delay wave digital filters (WDFs) for decimation and DC removal with configurable digital gains for optimal channel matching

2.6 Output Stage

- Two output channels (full stereo)
- Two 16-bit oversampling ΣΔ D/A converters
- Two line-level analog outputs
- Two configurable output attenuators for improved output dynamic range matching
- Two analog third-order anti-aliasing filters
- Two pulse-density modulation (PDM)-based direct digital outputs capable of driving low-impedance loads

2.7 Peripherals and Interfaces

2.7.1. Analog Interfaces

- Six external low-speed A/D converter (LSAD) inputs can be used with analog trimmers (e.g., potentiometers, analog switches, etc.)
- Two internal LSAD inputs tied directly to ground and supply can be used for supply monitoring

2.7.2. Digital Interfaces

- 16-pin general-purpose I/O (GPIO) interface
- Serial peripheral interface (SPI) communications port with interface speeds up to 640kbps at 1.28MHz system clock
- Pulse-code modulation (PCM) interface for high-bandwidth digital audio I/O
- Configurable RS-232 universal asynchronous receiver/transmitter (UART)
- RS-232-based communications port for debugging and in-circuit emulation
- Two-wire synchronous serial (TWSS) interface with speeds up to 100kbps at 1.28MHz system clock and up to 400kbps at higher system clocks (slave mode support only)

2.7.3. System

- Integrated watchdog timer
- General-purpose timer
- External clock input division circuitry to support a wide range of external clock speeds

3.0 BelaSigna 200 Design and Layout Strategies

BelaSigna 200 is designed to allow both digital and analog processing in a single system. Due to the mixed-signal nature of this system, the design of the printed circuit board (PCB) layout is critical to maintain the high audio fidelity of BelaSigna 200. To avoid coupling noise into the audio signal path, keep the digital traces away from the analog traces. To avoid electrical feedback coupling, isolate the input traces from the output traces.

3.1 Recommended Ground Design Strategy

The ground plane should be partitioned into two: the analog ground plane (AGND) and the digital ground plane (DGND). These two planes should be connected together at a single point, known as the star point. The star point should be located at the ground terminal of a capacitor on the output of the power regulator as illustrated in Figure 2.

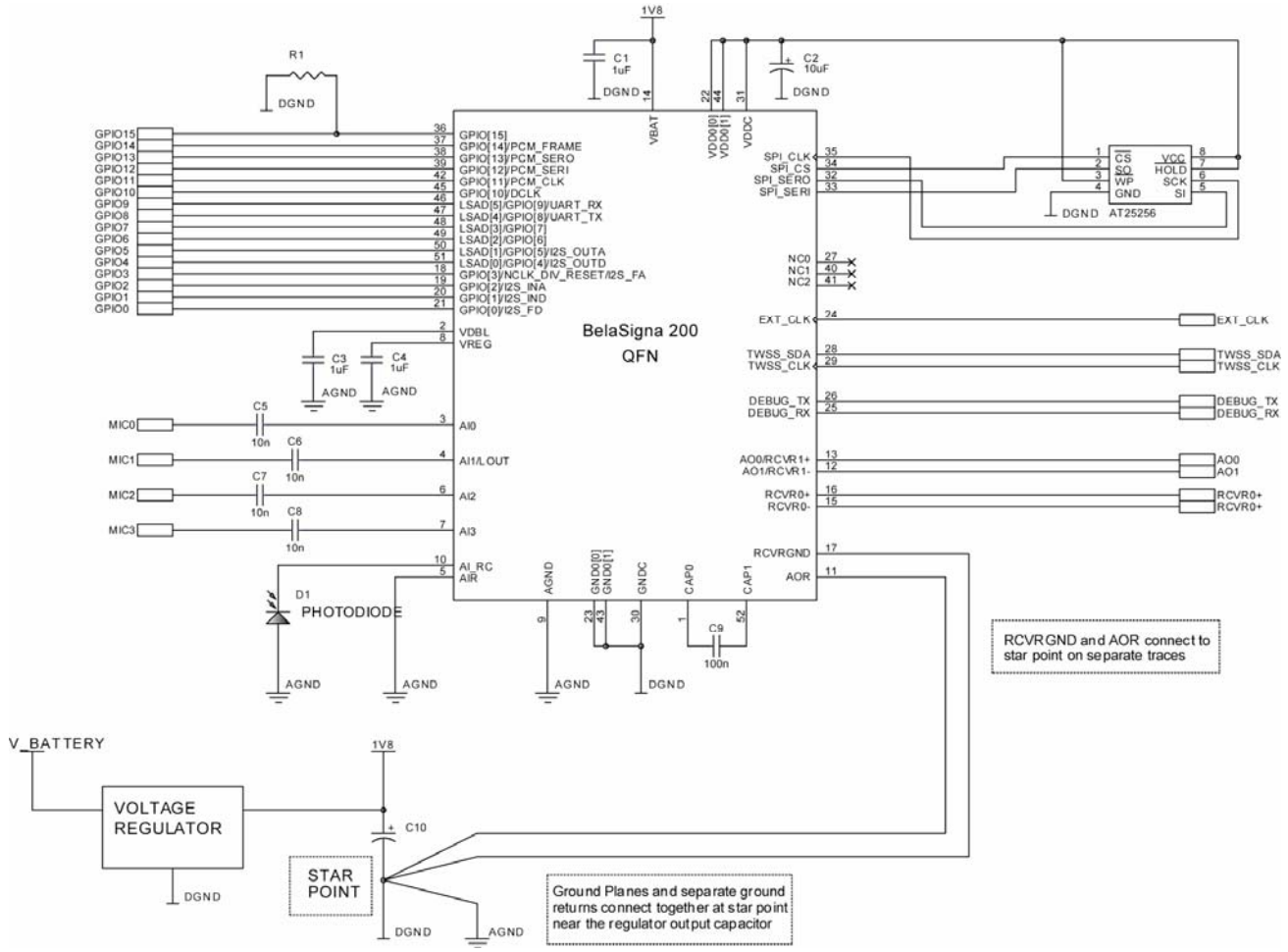


Figure 2: Schematic of Ground Scheme

The DGND plane is used as the ground return for digital circuits and should be placed under digital circuits.

The AGND plane should be kept as noise-free as possible. It is used as the ground return for analog circuits and it should surround analog components and pins. It should not be connected to or placed under any noisy circuits such as RF chips, switching supplies or

digital pads of BelaSigna 200 itself. Analog ground returns associated with the audio output stage should connect back to the star point on separate individual traces.

For more information on the recommended ground design strategy, see Table 1.

In some designs, space constraints may make separate ground planes impractical. In this case a star configuration strategy should be used. Each analog ground return should connect to the star point with separate traces.

3.2 Internal Power Supplies

Power management circuitry in BelaSigna 200 generates separate digital (VDDC) and analog (VREG, VDBL) regulated supplies. Each supply requires an external decoupling capacitor, even if the supply is not used externally. Decoupling capacitors should be placed as close as possible to the power pads. Further details are provided in Table 1. Non-critical signals are outlined in Table 2.

Table 1: Critical Signal

Pin Name	Description	Routing Guideline
VBAT	Power supply	Place 1µF (min) decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND plane.
VREG, VDBL	Internal regulator for analog sections	Place separate 1µF decoupling capacitors close to each pin. Connect negative capacitor terminal to AGND. Keep away from digital traces and output traces. VREG may be used to generate microphone bias. VDBL shall not be used to supply external circuitry.
AGND	Analog ground return	Connect to AGND plane.
VDDC	Internal regulator for digital sections	Place 10µF decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND. Should be connected to VDDO pins and to EEPROM power.
GNDO, GNDC	Digital ground return (pads and core)	Connect to digital ground.
AI0, AI1 / LOUT, AI2, AI3	Microphone inputs	Keep as short as possible. Keep away from all digital traces and audio outputs. Avoid routing in parallel with other traces. Connect unused inputs to AGND.
AIR	Input stage reference voltage	Connect to AGND. If no analog ground plane, should share trace with microphone grounds to star point.
AO0, AO1	Analog audio output	Keep away from microphone inputs.
RCVR0+, RCVR0-, RCVR1+, RCVR1-	Direct digital audio output	Keep away from analog traces, particularly microphone inputs. Corresponding traces should be of approximately the same length.
AOR	Output stage reference voltage	Connect to star point. Share trace with power amplifier (if present).
RCVRGND	Output stage ground return	Connect to star point.
EXT_CLK	External clock input / internal clock output	Minimize trace length. Keep away from analog signals. If possible, surround with digital ground.
AI_RC	Infrared receiver input	If used, minimize trace length to photodiode.

Table 2: Non-Critical Signal

Pin Name	Description	Routing Guideline
CAP0, CAP1	Internal charge pump - capacitor connection	Place 100nF capacitor close to pins
DEBUG_TX, DEBUG_RX	Debug port	Not critical Connect to test points
TWSS_SDA, TWSS_CLK	TWSS port	Not critical
GPIO[14..0]	General-purpose I/O	Not critical
GPIO[15]	General-purpose I/O Determines voltage mode during boot. For 1.8V operation, should be connected to DGND	Not critical
UART_RX, UART_TX	General-purpose UART	Not critical
PCM_FRAME, PCM_CLK, PCM_OUT, PCM_IN	Pulse code modulation port	Not critical
I2S_INA, I2S_IND, I2S_FA, I2S_FD, I2S_OUTA, I2S_OUTD	Philips I²S compatible port	Not critical
DCLK	Programmable clock output	Not critical If used, keep away from analog inputs/outputs
LSAD[5..0]	Low-speed A/D converters	Not critical
SPI_CLK, SPI_CS, SPI_SERI, SPI_SERO	Serial peripheral interface port Connect to EEPROM	Not critical

3.3 Audio Inputs

The audio input traces should be as short as possible. The input impedance of each audio input pad (e.g., AI0, AI1, etc.,) is high (approximately 500kΩ); therefore a 10nF capacitor is sufficient to decouple the DC bias[1]. Keep audio input traces strictly away from output traces. Microphone ground terminals should be connected to the AGND plane (if present) or share a trace with the input ground reference voltage pin (AIR) to the star point.

Analog and digital outputs MUST be kept away from microphone inputs.

3.4 Audio Outputs

The audio output traces should be as short as possible. If the direct digital output is used, the trace length of RCVRx+ and RCVRx- should be approximately the same to provide matched impedances. If the analog audio output is used, the ground return for the external power amplifier should share a trace with the output ground reference voltage pin (AOR) to the star point.

[1] The capacitor and the internal resistance form a first-order analog high pass filter whose cutoff frequency can be calculated by f_{3dB} (Hz) = 1/(R·C·2π), which results with ~30Hz for 10nF capacitor.

4.0 Mechanical and Environmental Information

BelaSigna 200 is available in two packages:

- The QFN package measures 8x8mm, has easy-to-probe signals and all I/O available.
- The CSP package is the ultra-miniature option, measuring only 2.3x3.7mm; this package has reduced I/O and flexibility, but still meets a wide range of application needs.

4.1 QFN Package Option

4.1.1. QFN Mechanical Information

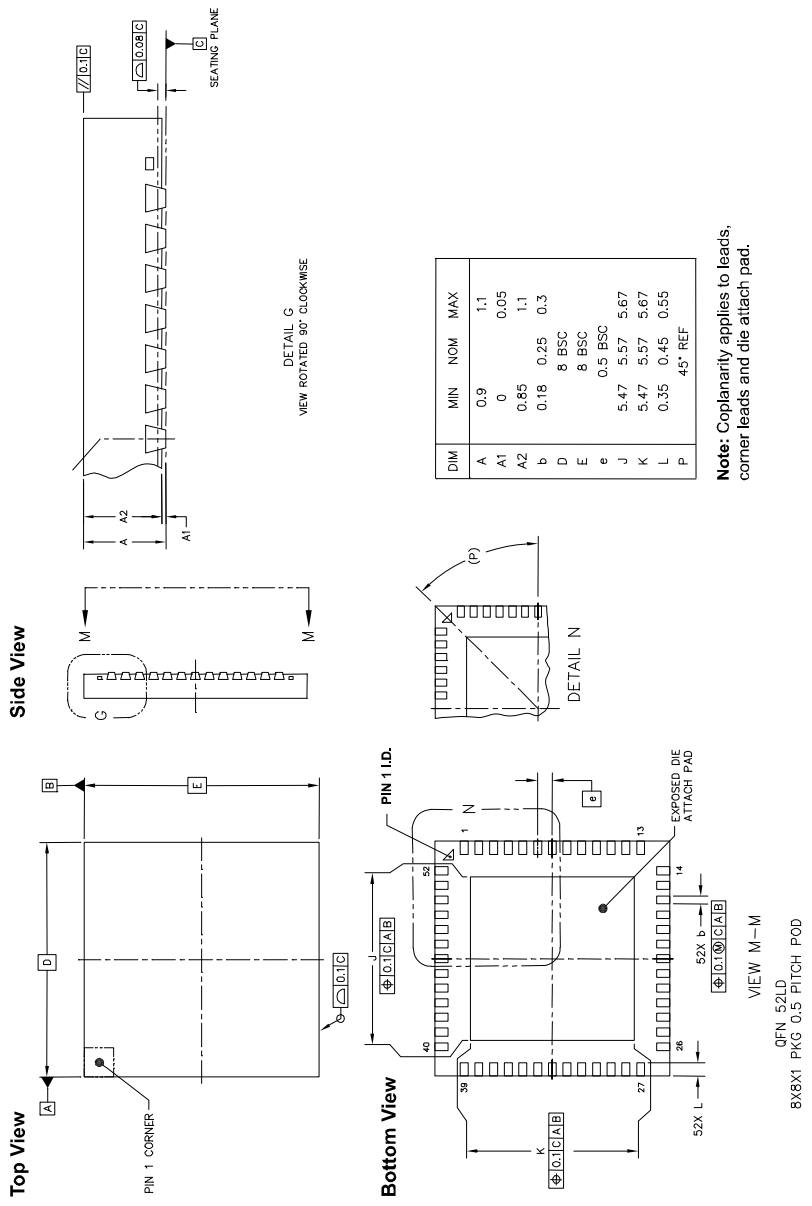
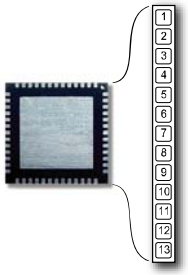


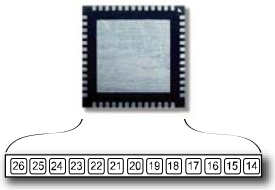
Figure 3: QFN Mechanical Drawings

4.1.2. QFN Pad Out

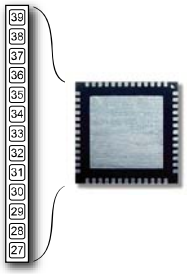
Pad #	Pad Name	Pad Function	I/O	U/D
1	CAP0	Charge pump capacitor pin 0	N/A	N/A
2	VDBL	Double voltage	O	N/A
3	A|0	Audio signal input to ADC0	I	N/A
4	A|1/LOUT	Audio signal input to ADC0/line level output signal from preamp 0	I/O	N/A
5	A|R	Reference voltage for microphone	N/A	N/A
6	A|2	Audio signal input to ADC1	I	N/A
7	A|3	Audio signal input to ADC1	I	N/A
8	VREG	Regulated voltage for microphone bias	O	N/A
9	AGND	Analog ground	N/A	N/A
10	AI_RC	Remote control input	I	N/A
11	AOR	Reference voltage for DAC	N/A	N/A
12	AO1/RCVR1-	Audio signal output from DAC1/output from direct digital drive 1-	O	N/A
13	AO0/RCVR1+	Audio signal output from DAC0/output from direct digital drive 1+	O	N/A



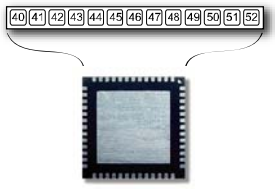
Pad #	Pad Name	Pad Function	I/O	U/D
14	VBAT	Positive power supply	I	N/A
15	RCVR0-	Output from direct digital drive 0	O	N/A
16	RCVR0+	Output from direct digital drive 0	O	N/A
17	RCVRGND	Receiver return current	N/A	N/A
18	GPIO[3]/ NCLK_DIV_RESET/I2S_FA	General-purpose I/O/clock divider reset/I2S interface analog blocks frame output	I/O	U
19	GPIO[2]/I2S_INA	General-purpose I/O/I2S interface analog blocks input	I/O	U
20	GPIO[1]/I2S_IND	General-purpose I/O/I2S interface analog blocks input	I/O	U
21	GPIO[0]/I2S_FD	General-purpose I/O/I2S interface digital blocks frame	I/O	U
22	VDDO	Digital pads supply input	I	N/A
23	GNDO	Digital pads ground	N/A	N/A
24	EXT_CLK	External clock input/internal clock output	I/O	U
25	DEBUG_RX	Debug port receive	I	U
26	DEBUG_TX	Debut port transmit	O	U



Pad #	Pad Name	Pad Function	I/O	U/D
27	RESERVED		N/A	N/A
28	TWSS_SDA	TWSS data	I/O	U
29	TWSS_CLK	TWSS clock	I	U
30	GNDC	Core logic ground	N/A	N/A
31	VDDC	Core logic, EEPROM and pad supply output	O	N/A
32	SPI_SERO	Serial peripheral interface serial data out	I/O	D
33	SPI_SERI	Serial peripheral interface serial data in	I	U
34	SPI_CS	Serial peripheral interface chip select	I/O	D
35	SPI_CLK	Serial peripheral interface clock	I/O	N/A
36	GPIO[15]	General-purpose I/O	I/O	U
37	GPIO[14]/PCM_FRAME	General-purpose I/O/PCM interface frame	I/O	U
38	GPIO[13]/PCM_OUT	General-purpose I/O/PCM interface output	I/O	U
39	GPIO[12]/PCM_IN	General-purpose I/O/PCM interface input	I/O	U



Pad #	Pad Name	Pad Function	I/O	U/D
40	N/C	No connection	N/A	N/A
41	N/C	No connection	N/A	N/A
42	GPIO[11]/PCM_CLK	General-purpose I/O/PCM interface clock	I/O	U
43	GNDO	Digital pads ground	N/A	N/A
44	VDDO	Digital pads supply input	I	N/A
45	GPIO[10]/DCLK	General-purpose I/O/class D receiver clock	I/O	U
46	LSAD[5]/GPIO[9]/UART_RX	Low-speed A/D/general-purpose I/O/general-purpose UART receive	I/O	U
47	LSAD[4]/GPIO[8]/UART_TX	Low-speed A/D input/general-purpose I/O/general-purpose UART transmit	I/O	U
48	LSAD[3]/GPIO[7]	Low-speed A/D input/general purpose I/P	I/O	U
49	LSAD[2]/GPIO[6]	Low-speed A/D input/general purpose I/P	I/O	U
50	LSAD[1]/GPIO[5]/I2S_OUTA	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
51	LSAD[0]/GPIO[4]/I2S_OUTD	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
52	CAP1	Charge pump capacitor pin 1	N/A	N/A



4.1.3. QFN Environmental Characteristics

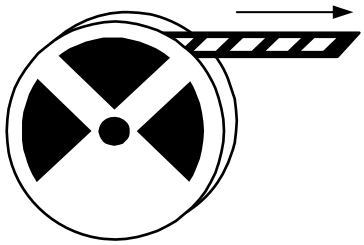
All parts supplied against this specification have been qualified as follows:

Table 3: Environmental Characteristics

Characteristics	
Packaging Level	
Moisture sensitivity level	JEDEC Level 3 30°C / 60% RH for 192 hours
Pressure cooker test (PCT)	121°C / 100% RH / 2 atm for 168 hours
Thermal cycling test (TCT)	-65°C to 150°C for 1000 cycles
Highly accelerated stress test (HAST)	130°C / 85% RH for 100 hours
High temperature stress test (HTST)	150°C for 1000 hours
Board Level	
Temperature	-40°C to 125°C for 2500 cycles with no failures
Drop	1m height with no failures
Bending	1mm deflection / 2Hz

4.1.4. QFN Carrier Information

ON Semiconductor offers tape and reel packing for BelaSigna 200 QFN packages. The packing consists of a pocketed carrier tape, a cover tape, and a molded anti-static polystyrene reel. The carrier and cover tape create an ESD safe environment, protecting the QFNs from physical and electro-static damage during shipping and handling.



Reel Diameter: 13 inches
Quantity Per Reel: 500 pieces
Date Codes: Max. of two date codes can be combined into one reel

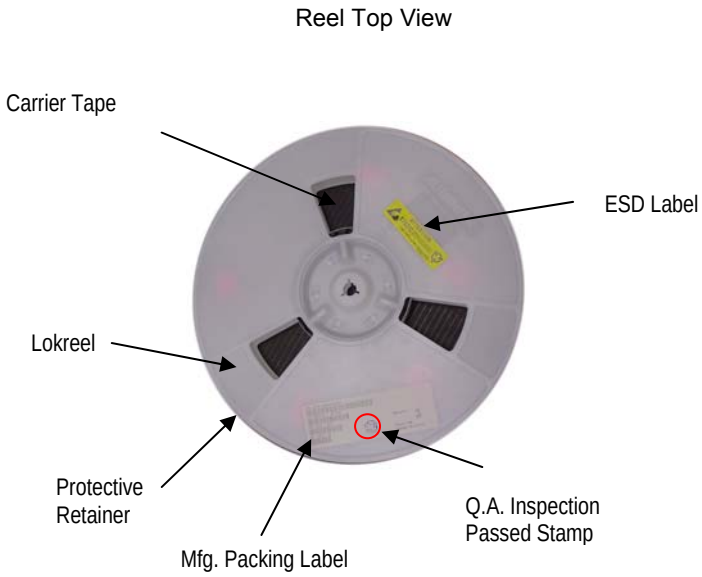
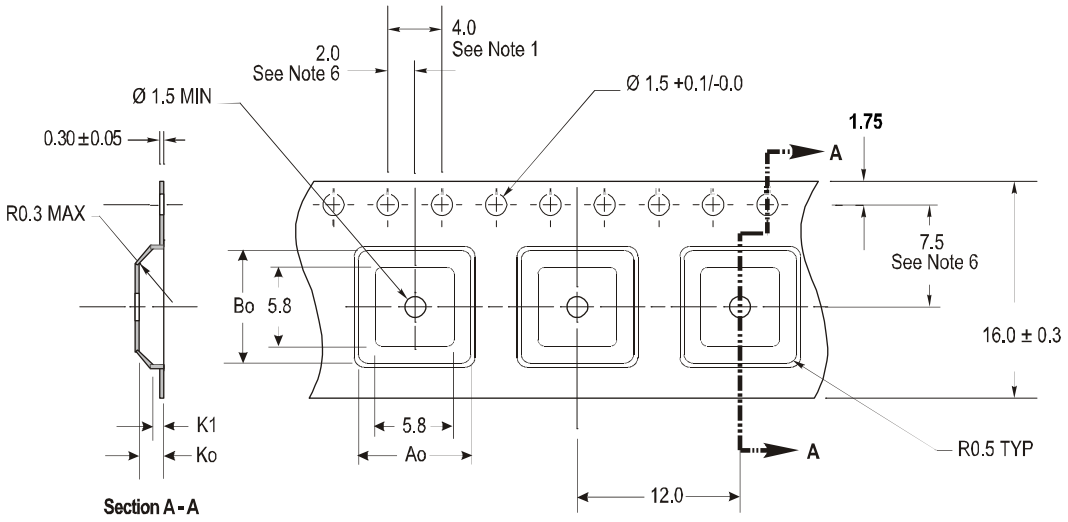


Figure 4: QFN Reel Format



All Dimensions in Millimeters
Ao = 8.3 mm
Bo = 8.3 mm
Ko = 2.0 mm
K1 = 1.0 mm

Figure 5: QFN Tape Dimensions

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.02.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: PS+C.2.
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

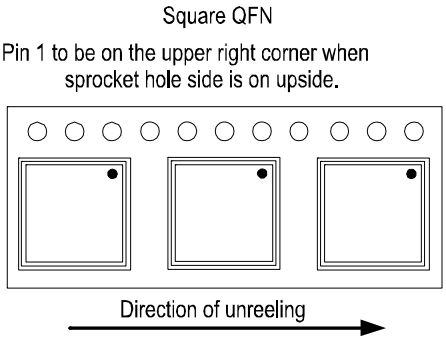


Figure 6: QFN Orientation in Tape

4.2 CSP Package Option

4.2.1. CSP Mechanical Information

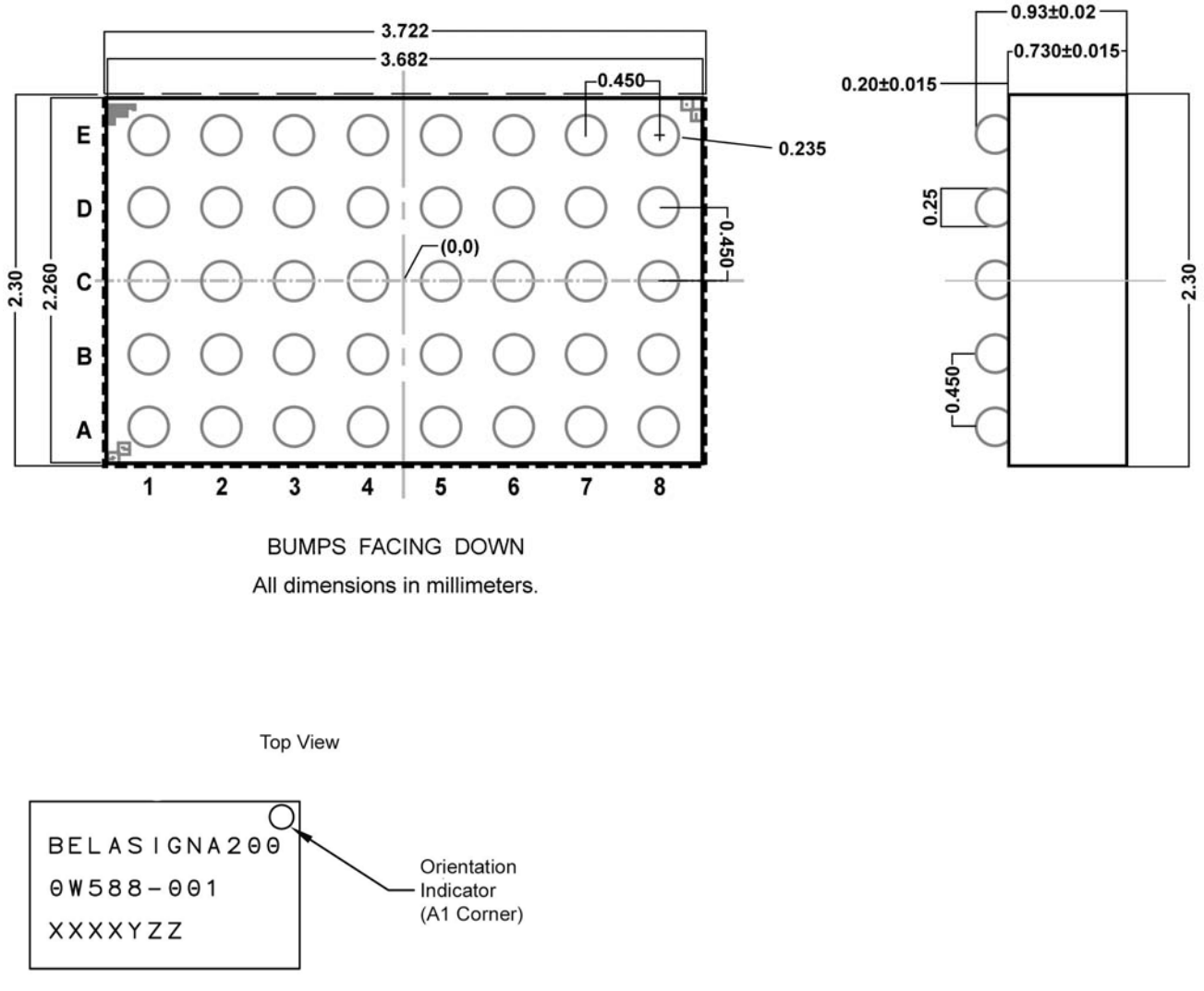


Figure 7: CSP Mechanical Drawings

4.2.2. CSP Pad Out

Table 4: Pad Out (Advance Information)

Pad Index	Pad Name	Pad Function	I/O	U/D
B2	CAP0	Charge pump capacitor pin 0	N/A	N/A
A2	CAP1	Charge pump capacitor pin 1	N/A	N/A
A1	VDBL	Double voltage	O	N/A
C3	VREG	Regulated voltage for microphone bias	O	N/A
B3	A|0	Audio signal input to ADC0	I	N/A
B1	A|1/LOUT	Audio signal input to ADC0/line level output signal from preamp 0	I/O	N/A
C2	A|2	Audio signal input to ADC1	I	N/A
C1	A|3	Audio signal input to ADC1	I	N/A
B4	A|R	Reference voltage for microphone	N/A	N/A
C4	AGND	Analog ground	N/A	N/A
D1	AOR	Reference voltage for DAC	N/A	N/A
E1	AO1/RCVR1-	Audio signal output from DAC1/output from direct digital drive 1-	O	N/A
D2	AO0/RCVR1+	Audio signal output from DAC0/output from direct digital drive 1+	O	N/A
D3	RCVR0-	Output from direct digital drive 0	O	N/A
E3	RCVR0+	Output from direct digital drive 0	O	N/A
D4	RCVRGND	Receiver return current	N/A	N/A
E2	VBAT	Positive power supply	I	N/A
E5	VDD	Core logic, EEPROM and pad supply	I	N/A
A6	GNDO	Digital pads ground	N/A	N/A
E6	GNDC	Core logic and pads ground	N/A	N/A
D6	EXT_CLK	External clock input/internal clock output	I/O	U
E7	DEBUG_RX	Debug port receive	I	U
D7	DEBUG_TX	Debut port transmit	O	U
E8	TWSS_SDA	TWSS data	I/O	U
D8	TWSS_CLK	TWSS clock	I	U
C8	SPI_SERO	Serial peripheral interface serial data out	I/O	D
C7	SPI_SERI	Serial peripheral interface serial data in	I	U
B8	SPI_CS	Serial peripheral interface chip select	I/O	D
C6	SPI_CLK	Serial peripheral interface clock	I/O	N/A
A8	GPIO[14]/PCM_FRAME	General-purpose I/O/PCM interface frame	I/O	U
B7	GPIO[13]/PCM_OUT	General-purpose I/O/PCM interface output	I/O	U
A7	GPIO[12]/PCM_IN	General-purpose I/O/PCM interface input	I/O	U
B6	GPIO[11]/PCM_CLK	General-purpose I/O/PCM interface clock	I/O	U
A5	GPIO[10]/DCLK	General-purpose I/O/class D receiver clock	I/O	U
B5	LSAD[5]/GPIO[9]/UART_RX	Low-speed A/D/general-purpose I/O/general-purpose UART receive	I/O	U
A4	LSAD[4]/GPIO[8]/UART_TX	Low-speed A/D input/general-purpose I/O/general-purpose UART transmit	I/O	U
C5	LSAD[3]/GPIO[7]	Low-speed A/D input/general purpose I/P	I/O	U
A3	LSAD[1]/GPIO[5]/I2S_OUT A	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
D5	LSAD[0]/GPIO[4]/I2S_OUT D	Low-speed A/D inputs/general-purpose I/O/I2S interface analog blocks output	I/O	U
E4	GPIO[3]/ NCLK_DIV_RESET/I2S_FA	General-purpose I/O/clock divider reset/I2S interface analog blocks frame output	I/O	U

4.2.3. CSP Environmental Characteristics

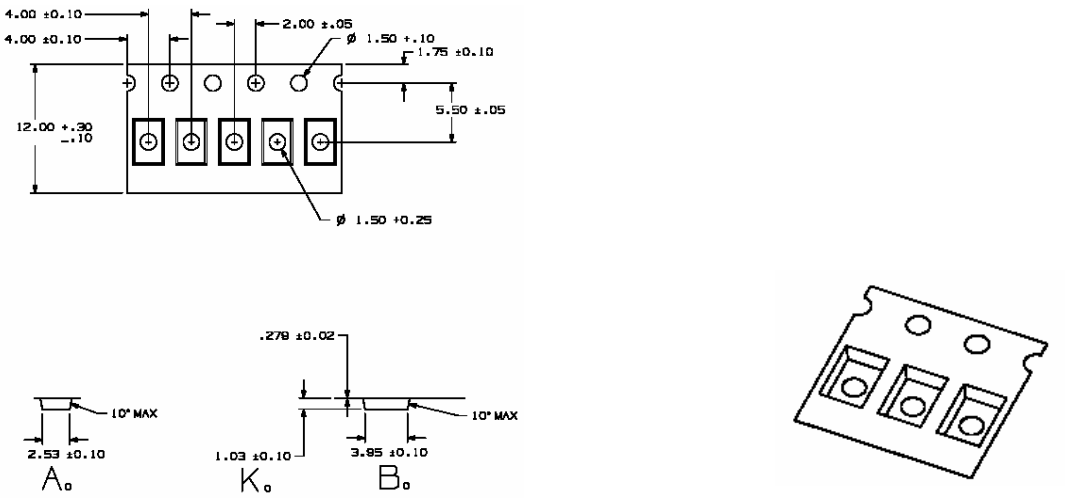
All parts supplied against this specification have been qualified as follows:

Table 5:

Packaging Level	
Moisture sensitivity level (MSL)	JEDEC Level 3 30°C / 60% RH for 192 hours
Pressure cooker test (PCT)	121°C / 100% RH / 2 atm for 168 hours
Thermal cycling test (TCT)	-65°C to 150°C for 1000 cycles
Highly accelerated stress test (HAST)	130°C / 85% RH for 100 hours
High temperature stress test (HTST)	150°C for 1000 hours
Board Level	
Temperature	-40°C to 125°C for 1000 cycles with no failures (for board thickness <40mils and underfilled CSP)
Drop	1m height with no failures

4.2.4. CSP Carrier Information

The devices will be provided in standard 7” Tape & Reel carrier with 5,000 parts per reel.



Note: all dimensions in millimeters

Figure 8: CSP Tape Dimensions

4.2.5. CSP Design Considerations

In order to achieve the highest level of miniaturization, the CSP package is constrained in ways that will factor into design decisions. The CSP will only operate in HV mode, and therefore requires a 1.8V operating voltage. The number of pins is reduced to 40 (compared to 49 active pins on the QFN). This reduction eliminates access to GPIOs (0,1,2,6,15), LSAD 2, the I2S interface, and the IR remote receiver.

For PCB manufacture with BelaSigna 200 CSP, ON Semiconductor recommends Solder-on-Pad (SoP) surface finish. With SoP, the solder mask opening should be solder mask-defined and copper pad geometry will be dictated by the PCB vendor’s design requirements.

BelaSigna 200

Alternative surface finishes are ENiG and OSP; volume of screened solder paste (#5) should be less than 0.0008mm^3. If no pre-screening of solder paste is used, then following conditions must be met:

(i) the solder mask opening should be >0.3mm in diameter,
(ii) the copper pad will have 0.25mm diameter, and
(iii) soldermask thickness should be less than 1mil thick above the copper surface.

ON Semiconductor can provide BelaSigna 200 CSP landpattern CAD files to assist your PCB design upon request.

5.0 Development Tools

5.1 Evaluation and Development Kit (EDK)

BelaSigna 200 is supported by a set of development tools included in the evaluation and development kit (EDK).

The EDK is intended for use by DSP software developers and hardware systems integrators. It consists of the following components:

- Hardware
    - BelaSigna 200 evaluation and development board (contains BelaSigna 200 device)
- Software
    - Complete assembly tool chain (assembler, linker, librarian, etc.)
    - Low-level hardware-specific libraries
    - Basic algorithm toolkit (BAT)
    - Basic operating system libraries (BOS)
    - WOLA windows and microcode
    - Real-time debugger
    - EEPROM file system manager
    - UltraEdit IDE
    - WOLA toolbox for Matlab for rapid application development and prototyping

BAT and BOS provide all the common processing routines in an easy-to-call macro structure. This streamlines the assembly level coding by encapsulating redundant work, while maintaining the true efficiency of hardware-level coding.

For advanced DSP developers or application developers, ON Semiconductor provides an application development extension to the EDK, which contains the following:

- Python language installer (version 2.2)
- The wxPython GUI toolkit
- Embedding toolkit (used to build standalone Python applications)
- ON Semiconductor extension
    - Python interface (pyLLCOM) to ON Semiconductor's low-level communications library (LLCOM)
    - File I/O library (supports standard ON Semiconductor file formats)
    - EEPROM access library
    - DSH (ON Semiconductor Python Shell – standard command-line shell with customizations for BelaSigna 200)

5.2 BelaSigna 200 Rapid Prototyping Module

The rapid prototyping module (RPM) is fast and easy for designers to integrate with existing and future products that are not yet DSP-enabled. It also allows for the quick implementation of field trials and rapid prototyping to evaluate the benefits of BelaSigna 200. The RPM features BelaSigna 200 along with a 256-Kbit EEPROM for storing a variety of custom algorithms. On-board power regulation circuitry allows the RPM to run off a wide variety of power supplies. A fast oscillator (included on the RPM) running at 24.576MHz provides a choice of many sampling frequencies and can be enabled for when heavy-duty signal processing is required.

5.3 BelaSigna 200 Demonstrator

The BelaSigna 200 demonstrator lets device manufacturers quickly and easily assess the speech- and audio-centric benefits delivered by BelaSigna 200 in a full-featured, self-contained portable unit. The demonstrator is housed in a durable, portable, lightweight package complete with belt clip to facilitate demonstrations in the field. This tool can be easily utilized in real world scenarios to experience the benefits of noise reduction, signal enhancement and a variety of other algorithms. The demonstrator can be connected to a wired headset and function like a dongle to communicate with a Bluetooth mobile phone.

Contact your account manager for more information.

6.0 Architecture Overview

6.1 RCore DSP

The RCore is a 16-bit fixed-point, dual-Harvard-architecture DSP. It includes efficient normalize and de-normalize instructions, plus support for double-precision operations to provide the additional dynamic range needed for many applications. All memory locations in the system are accessible by the RCore using several addressing modes including indirect and circular modes. The RCore generally assumes master functionality of the system.

6.1.1. RCore DSP Architecture

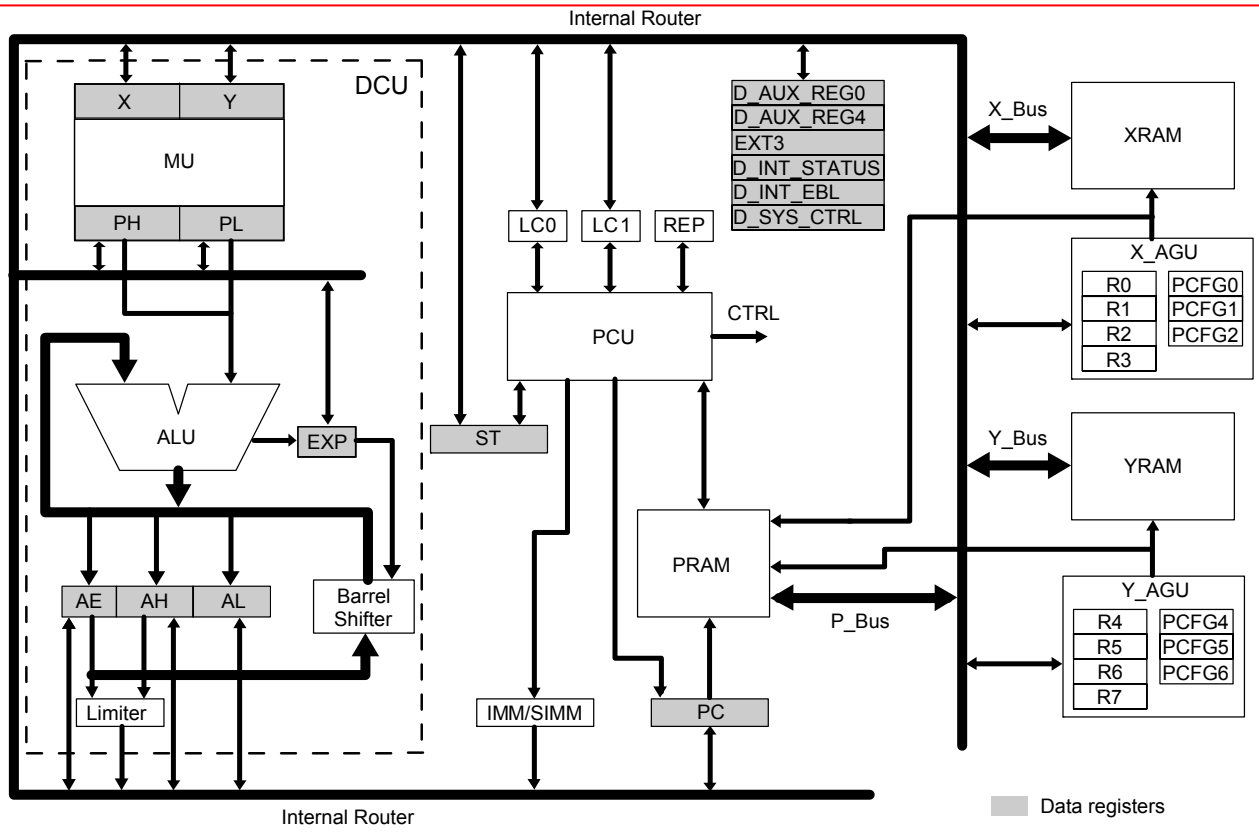


Figure 9: RCore Programming Model

The RCore is a single-cycle pipelined multiply-accumulate (MAC) architecture that feeds into a 40-bit accumulator complete with barrel shifter for fast normalization and de-normalization operations. Program execution is controlled by a sequencer that employs a three-stage pipeline (FETCH, DECODE, EXECUTE). Furthermore, the RCore incorporates pointer configuration registers for low cycle-count address generation when accessing the three memories: program memory (PRAM), X data memory (XRAM) and Y data memory (YRAM).

6.1.2. Instruction Set

The RCore instruction set can be divided into the following three classes:

1. Arithmetic and Logic Instructions

The RCore uses two's complement fractional as a native data format. Thus, the range of valid numbers is [-1; 1), which is represented by 0x8000 to 0x7FFF. Other formats can be utilized by applying appropriate shifts to the data.

The multiplier takes 16-bit values and performs a multiplication every time an operand is loaded into either the X or Y register. A number of instructions that allow loading of X and Y simultaneously and addition of the new product to the previous product (a MAC operation), are available. Single-cycle MAC with data pointer update and fetch is supported.

The arithmetic logic unit (ALU) receives its input from either the accumpulator (AE|AH|AL) or the product register (PH|PL). Although the RCORE is a 16-bit system, 32-bit additions or subtractions are also supported. Bit manipulation is also available on the accumulator as well as operations to perform arithmetic or logic shifts, toggling of specific bits, limiting, and other functions.

2. Data Movement Instructions

Data movement instructions transfer data between RAM, control registers and the RCore’s internal registers (accumulator, PH, PL, etc).

Two address generators are available to simultaneously generate two addresses in a single cycle. The address pointers R0..2 and R4..6 can be configured to support increment, decrement, add-by-offset, and two types of modulo-N circular buffer operations. Single-cycle access to low X memory or low Y memory as well as two-cycle instructions for immediate access to any address are also available.

3. Program Flow Control Instructions

The RCore supports repeating of both single-word instructions and larger segments of code using dedicated repeat instructions or hardware loop counters. Furthermore, instructions to manipulate the program counter (PC) register such as calls to subroutines, conditional branches and unconditional branches are also provided.

7.0 Instruction Set

Table 6: Instruction Set

Instruction	Description
ABS A [,Cond] [,DW]	Calculate absolute value of A on condition
ADD A, Reg [,C]	Add register to A
ADD A, (Rij) [,C]	Add memory to A
ADD A, DRAM [,B]	Add (DRAM) to A
ADD A, (Rij)p [,C]	Add program memory to A
ADD A, Rc [,C]	Add Rc register to A
ADDI A, IMM [,C]	Add IMM to A
ADSI A, SIMM	Add signed SIMM to A
AND A, Reg	AND register with AH to AH
AND A, (Rij)	AND memory with AH to AH
AND A, DRAM [,B]	AND (DRAM) with AH to AH
AND A, (Rij)p	AND program memory with AH to AH
AND A, Rc	AND Rc register with AH to AH
ANDI A, IMM	AND IMM with AH to AH
ANSI A, SIMM	AND unsigned SIMM with AH to AH
BRA PRAM [,Cond]	Branch to new address on condition
BREAK	Stop the DSP for debugging purposes
CALL PRAM [,Cond] [,B]	Push PC and branch to new address on condition
CLB A	Calculate the leading bits on A
CLR A [,DW]	Clear accumulator
CLR Reg	Clear register
CMP A, Reg [,C]	Compare register to A
CMP A, (Rij) [,C]	Compare memory to A
CMP A, DRAM [,B]	Compare (DRAM) to A
CMP A, (Rij)p [,C]	Compare program memory to A
CMP A, Rc [,C]	Compare Rc register to A
CMPI A, IMM [,C]	Compare IMM to A
CMSI A, SIMM	Compare signed SIMM to A
CMPL A [,Cond] [,DW]	Calculate logical inverse of A on condition
DADD [Cond] [,P]	Add PH | PL to A, update PH | PL on condition
DBNZ0/1 PRAM	Branch to new address if LC0/1 <> 0

Instruction	Description
DCMP	Compare PH | PL to A
DEC A [,Cond] [,DW]	Decrement A on condition
DEC Reg [Cond]	Decrement register on condition
DEC (Rij) [,Cond]	Decrement memory on condition
DSUB [Cond] [,P]	Subtract PH | PL from A, update PH | PL on condition
EOR A, Reg	Exclusive-OR register with AH to AH
EOR A, (Rij)	Exclusive-OR memory with AH to AH
EOR A, DRAM [,B]	Exclusive-OR (DRAM) with AH to AH
EOR A, (Rij)p	Exclusive-OR program memory with AH to AH
EOR A, Rc	Exclusive-OR Rc register with AH to AH
EORI A, IMM	Exclusive-OR IMM with AH to AH
EOSI A, SIMM	Exclusive-OR unsigned SIMM with AH to AH
INC A [,Cond] [,DW]	Increment A on condition
INC Reg [,Cond]	Increment register on condition
INC (Rij) [,Cond]	Increment memory on condition
LD Rc, Rc	Load Rc register with Rc register
LD Reg, Reg	Load register with register
LD Reg, (Rij)	Load register with memory
LD (Rij), Reg	Load memory with register
LD A, DRAM [,B]	Load A with (DRAM)
LD DRAM, A [,B]	Load (DRAM) with A
LD Rc, (Rij)	Load Rc register with memory
LD (Rij), Rc	Load memory with Rc register
LD Reg, (Rij)p	Load register with program memory
LD (Rij)p, Reg	Load program memory with register
LD Reg, (Reg)p	Load register with program memory via register
LD Reg, Rc	Load register with Rc register
LD Rc, Reg	Load Rc register with register
LDI Reg, IMM	Load register with IMM
LDI Rc, IMM	Load Rc register with IMM
LDI (Rij), IMM	Load memory with IMM

Table 7: Instruction Set Continued

Instruction	Description
LDLC0/1 SIMM	Load loop counter with 8-bit unsigned SIMM
LDSI A, SIMM	Load A with signed SIMM
LDSI Rij, SIMM	Load pointer register with unsigned SIMM
MLD (Rj), (Ri) [,SQ]	Multiplier load and clear A
MLD Reg, (Ri) [,SQ]	Multiplier load and clear A
MODR Rj, Ri	Pointer register modification
MPYA (Rj), (Ri) [,SQ]	Multiplier load and accumulate
MPYA Reg, (Ri) [,SQ]	Multiplier load and accumulate
MPYS (Rj), (Ri) [,SQ]	Multiplier load and accumulate negative
MPYS Reg, (Ri) [,SQ]	Multiplier load and accumulate negative
MSET (Rj), (Ri) [,SQ]	Multiplier load
MSET Reg, (Ri) [,SQ]	Multiplier load
MUL [Cond] [,A] [,P]	Update A and/or PH | PL with X*Y on condition
NEG A [,Cond] [,DW]	Calculate negative value of A on condition
NOP	No operation
OR A, Reg	OR register with AH to AH
OR A, (Rij)	OR memory with AH to AH
OR A, DRAM [,B]	OR (DRAM) with AH to AH
OR A, (Rij)p	OR program memory with AH to AH
OR A, Rc	OR Rc register with AH to AH
ORI A, IMM	OR IMM with AH to AH
ORSI A, SIMM	OR unsigned SIMM with AH to AH
POP Reg [,B]	Pop register from stack
POP Rc [,B]	Pop Rc register from stack
PUSH Reg [,B]	Push register on stack
PUSH Rc [,B]	Push Rc register on stack

Instruction	Description
PUSH IMM [,B]	Push IMM on stack
REP n	Repeat next instruction n+1 times (9-bit unsigned)
REP Reg	Repeat next instruction Reg+1 times
REP (Rij)	Repeat next instruction (Rij)+1 times
RES Reg, Bit	Clear bit in register
RES (Rij), Bit	Clear bit in memory
RET [B]	Return from subroutine
RND A	Round A with AL
SET Reg, Bit	Set bit in register
SET (Rij), Bit	Set bit in memory
SET_IE	Set interrupt enable flag
SHFT n	Shift A by +/- n bits (6-bit signed)
SHFT A [,Cond] [,INV]	Shift A by EXP bits on condition
SLEEP [IE]	Sleep
SUB A, Reg [,C]	Subtract register from A
SUB A, (Rij) [,C]	Subtract memory from A
SUB A, DRAM [,B]	Subtract (DRAM) from A
SUB A, (Rij)p [,C]	Subtract program memory from A
SUB A, Rc [,C]	Subtract Rc register from A
SUBI A, IMM [,C]	Subtract IMM from A
SUSI A, SIMM	Subtract signed SIMM from A
SWAP A [,Cond]	Swap AH, AL on condition
TGL Reg, Bit	Toggle bit in register
TGL (Rij), Bit	Toggle bit in memory
TST Reg, Bit	Test bit in register
TST (Rij), Bit	Test bit in memory

Table 8: Notation

Symbol	Meaning
A B	Accumulator update Memory bank selection (X or Y)
C	Carry bit
Cond	Condition in status register
DRAM	Low data (X or Y) memory address (8 bits)
DW	Double word
IE	Interrupt enable flag
IMM	Immediate data (16 bits)

Symbol	Meaning
INV	Inverse shift
P PRAM	PH | PL update Program memory address (16 bits)
Rc	Rc register (R0..7, PCFG0..2, PCFG4..6, LC0/1)
Reg	Data register (AL, AH, X, Y, ST, PC, PL, PH, EXT0, EXP, AE, EXT3..EXT7)
Ri / Rj / Rij	Pointer to X / Y / either data memory
SIMM	Short immediate data (10 bits)
SQ	Square

7.1 Weighted Overlap-Add (WOLA) Filterbank Coprocessor

The WOLA coprocessor performs low-delay, high-fidelity filterbank processing to provide efficient time-frequency processing. The coprocessor stores intermediate data values, program code and window coefficients in its own memory space. Audio data are accessed directly from the input and output FIFOs where they are automatically managed by the IOP.

The WOLA coprocessor can be configured to handle different sizes and types of transforms, such as mono, simple stereo or full stereo configurations. The number of bands, the stacking mode (even or odd), the oversampling factor, and the shape of the analysis and synthesis windows used are all configurable. The selected set of parameters affects both the frequency resolution, the group delay through the WOLA coprocessor and the number of cycles needed for complete execution.

The WOLA coprocessor can generate both real and complex data. Either real or complex gains can be applied. The RCore always has access to these values through shared memories. All parameters are configurable with microcode, which is used to control the WOLA during execution.

The RCore initiates all WOLA functions (analysis, gain applications, synthesis) through dedicated control registers. A dedicated interrupt is used to signal completion of a WOLA function.

Many standard WOLA microcode configurations are delivered with the EDK. These configurations have been specially designed for low group delay and high fidelity.

7.2 Input Output Processor (IOP)

The IOP is an audio-optimized configurable DMA unit for audio data samples. It manages the collection of data from the A/D converters to the input FIFO and feeds digital data to the audio output stage from the output FIFO. The IOP can be configured to access data in the FIFOs in four different ways:

- **Mono mode:** Input samples are stored sequentially in the input FIFO. Output samples are stored sequentially in the output FIFO.
- **Simple stereo mode:** Input samples from the two channels are stored interleaved in the input FIFO. Output samples for the single output channel are stored in the lower part of the output FIFO.
- **Digital mixed mode:** Input samples from the two channels are stored in each half of the input FIFO. Output samples for the single output channel are stored in the lower half of the output FIFO.
- **Full stereo mode:** Input samples from the two channels are stored interleaved in the input FIFO. Output samples for the two output channels are stored interleaved in the output FIFO. (Note: A one-in, two-out configuration can be achieved in this mode by leaving the second input unused).

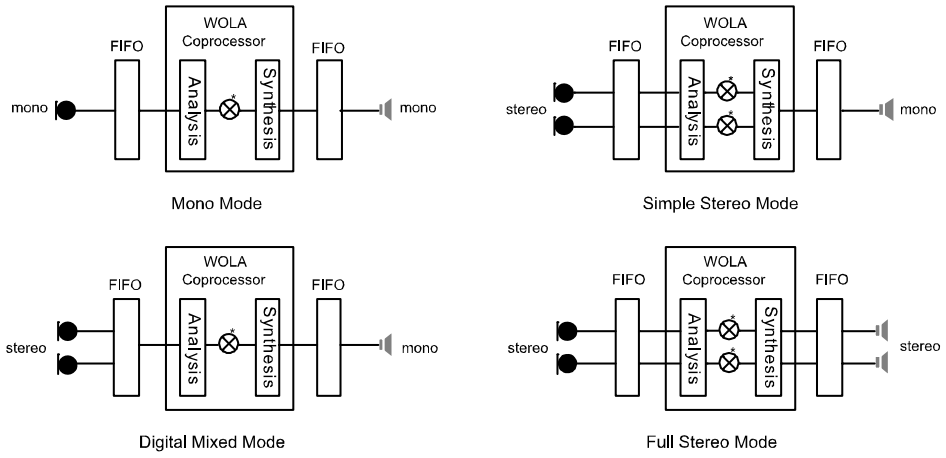


Figure 10: Four Audio Modes

The IOP places and retrieves FIFO data in memories shared with the RCore. Each FIFO (input and output) has two memory interfaces. The first corresponds with the normal FIFO. Here the address of the most recent input block changes as new blocks arrive. The second corresponds with the Smart FIFO. In this scheme the address of the most recent input block is fixed. The smart FIFO interface is especially useful for time-domain filters.

In the case where the WOLA and the IOP no longer work together as a result of a low battery condition, an IOP end-of-battery-life auto-mute feature is available.

7.3 General-Purpose Timer

The general-purpose timer is a 12-bit countdown timer with a 3-bit prescaler that interrupts the RCore when it reaches zero. It can operate in two modes, single-shot or continuous. In single-shot mode the timer counts down only once and then generates an interrupt. It will then have to be restarted from the RCore. In continuous mode the timer restarts with full timeout setting every time it hits zero and interrupts are generated continuously. This unit is often useful in scheduling tasks that are not part of the sample-based signal processing scheme, such as checking a battery voltage, or reading the value of a volume control.

7.4 Watchdog Timer

The watchdog timer is a configurable hardware timer that operates from the system clock and is used to prevent unexpected or unstable system states. It is always active and must be periodically acknowledged as a check that an application is still running. Once the watchdog times out, it generates an interrupt. If left to time out a second consecutive time without acknowledgement, a system reset will occur.

7.5 RAM and ROM

There are 20 Kwords of on-chip program and data RAM on BelaSigna 200. These are divided into three entities: a 12-Kword program memory, and two 4-Kword data memories ("X" and "Y" as are common in a dual-Harvard architecture).

There are also three RAM banks that are shared between the RCore and WOLA coprocessor. These memory banks contain the input and output FIFOs, gain tables for the WOLA coprocessor, temporary memory for WOLA calculations, WOLA coprocessor results, and the WOLA coprocessor microcode.

There is a 128-word lookup table (LUT) ROM that contains $\log_2(x)$, 2^x, 1/x and sqrt(x) values, and a 1-Kword ProgramROM that is used during booting and configuration of the system.

Complete memory maps for BelaSigna 200 are shown in Figure 11.

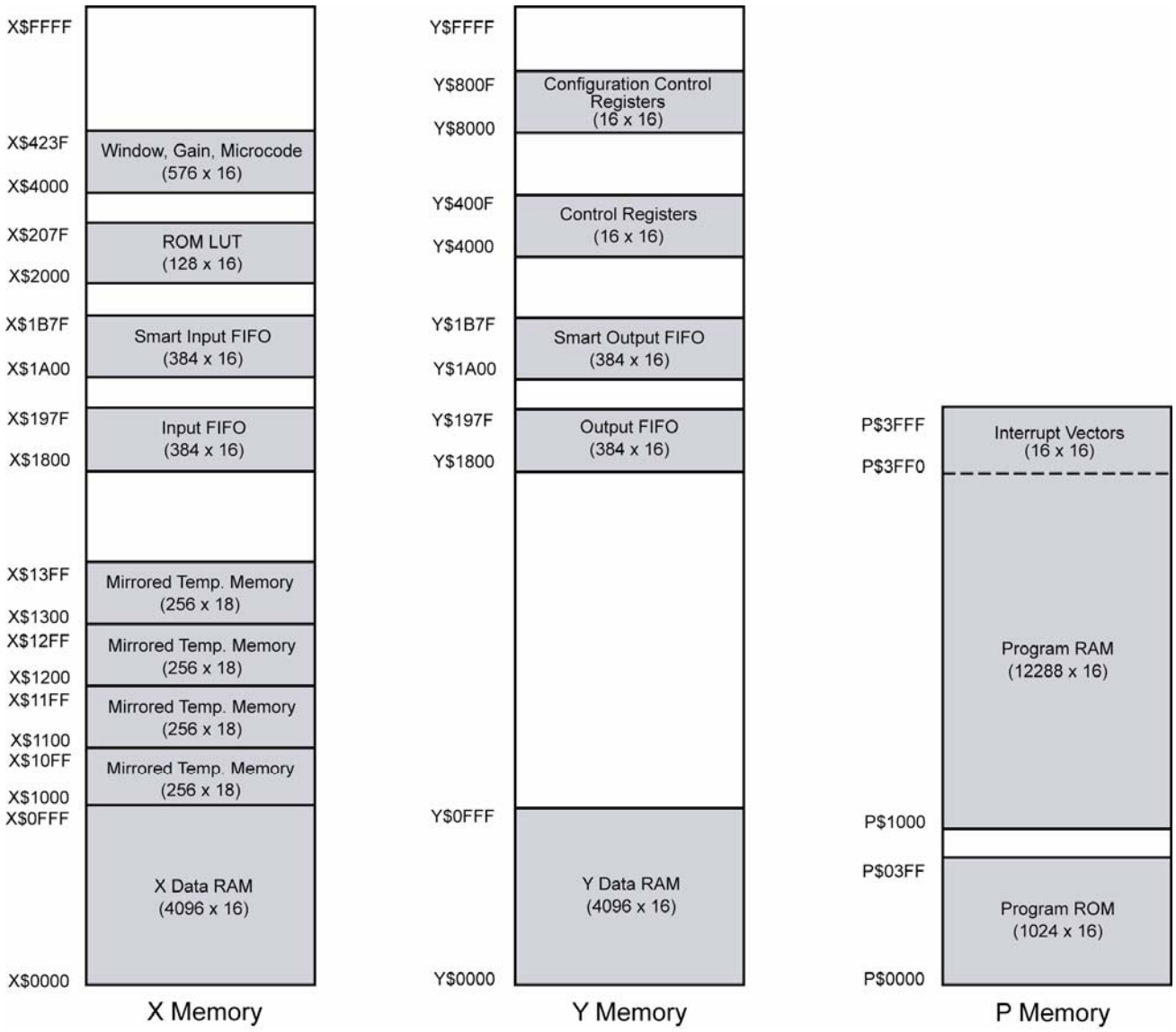


Figure 11: Memory Maps

7.6 Interrupts

The RCore DSP has a single interrupt channel that serves eleven interrupt sources in a prioritized manner. The interrupt controller also handles interrupt acknowledge flags. Every interrupt source has its own interrupt vector. Furthermore, the priority scheme of the interrupt sources can be modified. Refer to Table 9 for a description of all the interrupts.

Table 9: Interrupts

Interrupt	Description
WOLA_DONE	WOLA function done
IO_BLOCK_FULL	IOP interrupt
PCM	PCM interface interrupt
UART_RX	General-purpose UART receive interrupt
UART_TX	General-purpose UART transmit interrupt
GP_TIMER	General-purpose timer interrupt
WATCHDOG_TIMER	Watchdog timer interrupt
SPI_INTERFACE	SPI interface interrupt
TWSS_INTERFACE	TWSS interface interrupt
EXT3_RX	EXT3 register receive interrupt
EXT3_TX	EXT3 register transmit interrupt

8.0 Description of Analog Blocks

8.1 Input Stage

The analog audio input stage is comprised of two individual channels. For each channel, one of two possible inputs is routed to the input of the programmable preamplifier that can be configured for bypass or gain values of 12 to 30dB (3-dB steps).

The analog signal is filtered to remove frequencies above 10kHz before it is passed into the high-fidelity 16-bit oversampling ΣΔ A/D converter. Subsequently, any necessary sample rate decimation is performed to downsample the signal to the desired sampling rate. During decimation the level of the signal can be adjusted digitally for optimal gain matching between the two input channels. Any undesired DC component can be removed by a configurable DC-removal filter that is part of the decimation circuitry. The DC removal filter can be bypassed or configured for cut-off frequencies at 5, 10 and 20Hz.

A built-in feature allows a sampling delay to be configured between channel zero and channel one. This is useful in beam-forming applications.

For power consumption savings either of the input channels can be disabled via software.

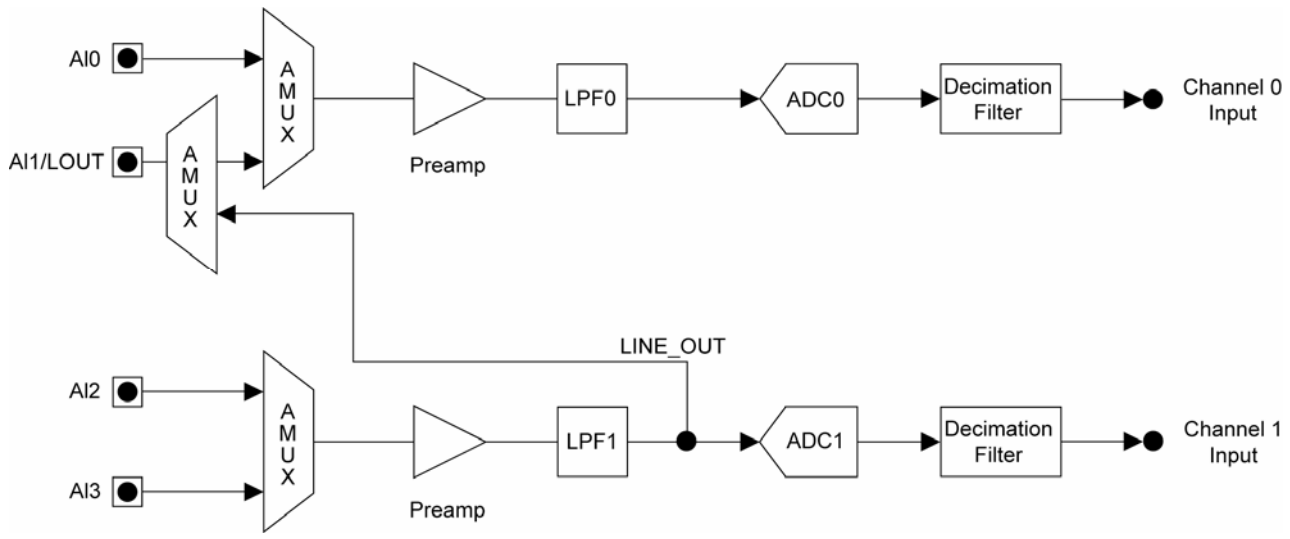


Figure 12: Input Stage

8.2 Output Stage

The analog audio output stage is composed of two individual channels. The first part of the output stage interpolates the signal for highly oversampled D/A conversion and automatically configures itself for the desired oversampling rate. Here, the signal is routed to both the ΣΔ D/A converter and the direct digital outputs. The D/A converter translates the signal into a high-fidelity analog signal and passes it into a reconstruction filter to smooth out the effects of sampling. The reconstruction filter has a fixed cut-off frequency at 10kHz.

From the reconstruction filter, the signal passes through the programmable output attenuator, which can adjust the signal for various line-level outputs or mute the signal altogether. The attenuator can be bypassed or configured to a value in the interval -12 to -30dB (3-dB steps).

The direct digital output provides a bridge driven by a pulse-density modulated output that can be used to directly drive an output transducer without the need for an external power amplifier.

Two analog outputs designed to drive external amplifiers are also available.

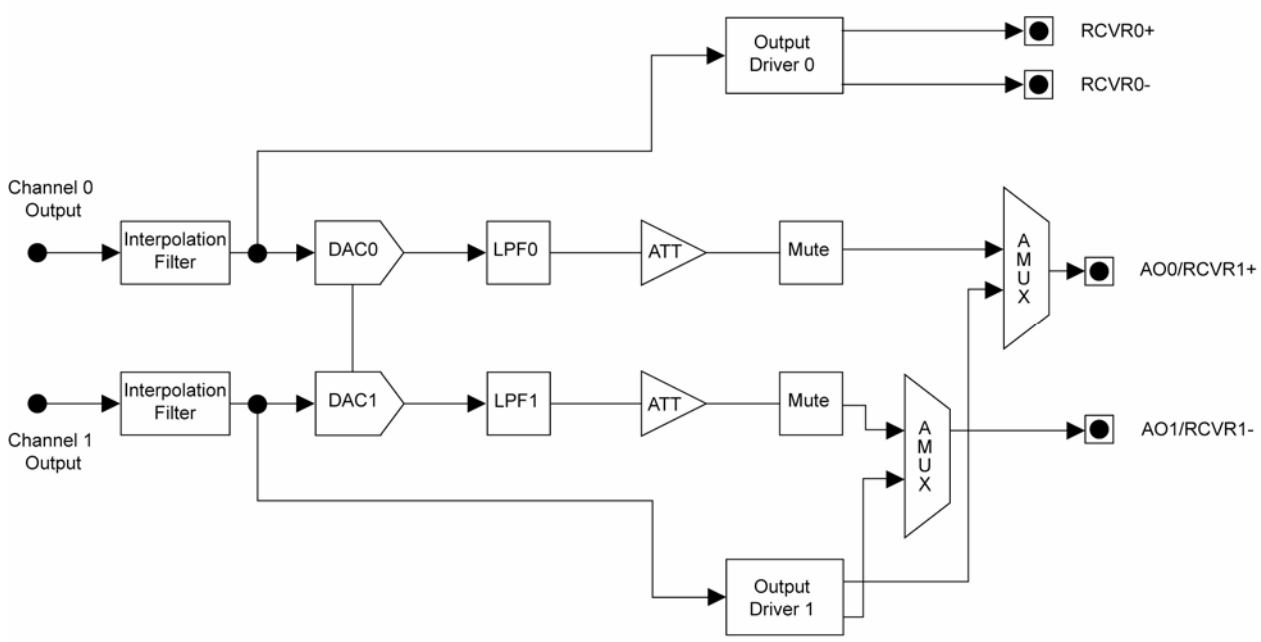


Figure 13: Output Stage

8.3 Clock-Generation Circuitry

BelaSigna 200 operates with two main clock domains: a domain running on the system clock (SYS_CLK) and a domain running on the main clock (MCLK). SYS_CLK can either be internally generated or externally delivered. It is used to drive all on-chip processors such as the RCore, the WOLA coprocessor and the IOP. MCLK is generated by division of SYS_CLK and is used to drive all A/D converters, D/A converters and external interfaces (except SPI, PCM, I^2S, and GPIO interfaces). The division factor used to create the desired MCLK from SYS_CLK is configurable to support external clocks with a wide range of frequencies.

The sampling frequency of all A/D converters and D/A converters also depends on MCLK. When MCLK is 1.28MHz, sampling frequencies in the interval 10.7kHz to 20kHz can be selected. Sampling frequencies up to 60kHz can be obtained with other MCLK frequencies.

8.4 Battery Monitor

A programmable on-chip battery monitor is available for power management. The battery monitor works by incrementing a counter value every time the battery voltage goes below a desired, configurable threshold value. This counter value can be used in an application-specific power-management algorithm running on the RCore. The RCore can initiate any desired actions in case the battery hits a predetermined value.

8.5 Multi-Chip Sample Clock Synchronization

BelaSigna 200 allows MCLK synchronization between two or more BelaSigna 200 chips connected in a multi-chip configuration. Samples on multiple chips occur at the same instant in time. This is useful in applications using microphone arrays where synchronous sampling is required. The sample clock synchronization is enabled using a control bit and a GPIO assignment that brings all MCLKs across chips to zero phase at the same instant in time.

9.0 External Interfaces

9.1 External Digital Interfaces

9.1.1. Pulse-Code Modulation Interface (PCM I/F)

The PCM interface is a bi-directional, four-wire synchronous serial interface suitable for high-speed digital audio transfer. This externally-clocked interface is capable of sending data serially at rates up to the clock speed of the RCore, providing the necessary bandwidth for digital audio. This interface can also be used for a number of other functions, including multi-processing BelaSigna 200 chips. The interface is configurable for glueless connections to four-wire PCM interfaces as well as other BelaSigna 200 chips in a BelaSigna 200 multi-chip configuration. Both master and slave modes are supported. The interface is configured via a memory-mapped configuration register and interacts with the RCore through memory-mapped control registers and interrupts. Refer to Section 12.1 for timing specifications.

9.1.2. General-Purpose Input/Output (GPIO)

Up to 16 GPIO pins are available to be configured as inputs or as outputs. All GPIO pins are pulled up internally. Data are read or written via a memory-mapped control register. GPIO pins can be used to interface to digital switches, other devices, etc. The direction of each bit is programmable via a direction register. Refer to Section 12.2 for timing specifications.

9.1.3. Serial Peripheral Interface (SPI) Port

The SPI port allows BelaSigna 200 to communicate synchronously with other devices such as external memory or EEPROM. This SPI interface conforms to the standard SPI bus protocol supporting modes zero and two as a master, and transfer speeds up to half the system clock frequency. The interface is configured via a memory-mapped configuration register and interacts with the RCore through memory-mapped control registers and interrupts. Refer to Section 12.3 for timing specifications.

9.1.4. RS-232 Universal Asynchronous Receiver/Transmitter (UART)

The general-purpose UART is a low-voltage RS-232-compatible interface. All data are transmitted and received with eight data bits, no parity and one stop bit (8N1). A range of standard data rates, up to a maximum of 115.2kbps, is supported. The interface is configured via a memory-mapped configuration register and interacts with the RCore through memory-mapped control registers and interrupts.

9.1.5. Debug Port

The debug port is also a low-voltage RS-232-based UART, and it interfaces directly to the program controller. This interface differs from the general-purpose UART in its access path to the RCore. It is used primarily by the evaluation and development tools to interface to, program and debug BelaSigna 200 applications. Data rates up to 115.2kbps are supported. The protocol uses eight data bits, no parity and one stop bit (8N1).

9.1.6. Two-Wire Synchronous Serial (TWSS) Interface

This industry standard two-wire high-speed synchronous serial interface allows communication to a variety of other integrated circuits and memories. On BelaSigna 200, this interface operates in slave mode only. Data rates up to 400kbps are supported for MCLK frequencies higher than 1.28MHz; for lower MCLK frequencies, the maximum rate is 100kbps. The interface is configured via memory mapped configuration registers and interacts with the RCore through memory-mapped control registers and interrupts. The TWSS interface is compatible with the Philips' I^2C protocol.

9.1.7. I^2S Interface

This industry standard digital audio interface uses a three-wire serial protocol to transmit and receive audio between BelaSigna 200 and other systems. The interface operates at the system clock frequency and BelaSigna 200 always assumes master functionality.

9.2 External Analog Interfaces

9.2.1. Low-Speed A/D Converters (LSAD)

Six LSAD inputs are available on BelaSigna 200. Combined with two internal LSAD inputs (supply and ground) this gives a total of eight multiplexed inputs to the LSAD converter. The multiplexed inputs are sampled sequentially at 1.6kHz per channel. The native data format for the LSAD is 10-bit two's complement. However, a total of eight operation modes are provided that allow a configurable input dynamic range in cases where certain minimum and maximum values for the converted inputs are desired; such as in the case of a volume control where only input values up to a certain magnitude are allowed.

10.0 Boot Sequence

BelaSigna 200 boots in a two-stage boot sequence. The ProgramROM begins loading the bootloader from an external SPI EEPROM 200ms after power is applied to the chip. In this process the ProgramROM checks the EEPROM file structure to ensure validity. If the file structure is validated, the bootloader is written to PRAM. In case of an error while reading the external EEPROM, all outputs are muted. The system will then reset due to a watchdog timeout.

Once the bootloader is loaded into PRAM the program counter is set to point to the beginning of the bootloader code. Subsequently, the signal-processing application that is stored in the EEPROM is downloaded to PRAM by the bootloader. The boot process generally takes less than one second. ON Semiconductor provides a standard full-featured bootloader.

An alternative to bootloading is often used in development - program code can be loaded through the debug port after powering BelaSigna 200. In this case, an SPI EEPROM may or may not be attached, and the debug port takes over control of the system. Some products use this technique when an EEPROM is not suitable to the application.

11.0 Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 10: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply voltage		2.0	V
Operating temperature range[2]	-40	85	°C
Storage temperature range	-55	125	°C
Voltage at any input pin	-0.3	2.1	V
Caution: Class 2 ESD sensitivity, JESD22-A114-B (2000V)			

11.2 Electrical Characteristics

Conditions: Temperature = 25°C, f_{SYS_CLK} = 1.28MHz (internal), f_{MCLK} = 1.28MHz, f_{SAMP} = 16kHz, V_{bat} = 1.8V

Table 11: Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Overall (1µF VBAT external capacitor)						
Supply voltage	Vbat		1.03	1.25	1.8	V
Current consumption[4]	Ibat	Vbat = 1.8V		650		µA
VREG (1µF external capacitor)						
Regulated output	VREG	unloaded	0.9	1.0	1.1	V
PSRR		@ 1kHz	35	50		dB
Load current	Ireg				2	mA
Load regulation				12	18	mV/mA
Line regulation				2	5	mV/V
VDBL (1µF external capacitor)						
Regulated output	VDBL		1.8	2.0	2.2	V
PSRR		@ 1kHz		45		dB
Load current	Ireg				2	mA
Load regulation		Charge pump cap = 100nF		130	200	mV/mA
Line regulation				5	8	mV/V
VDDC (1µF external capacitor)						
HV output	HV	HV mode		Vbat		V

[2] Audio performance parameters may degrade outside the range of 0 to 70 degrees C. Internal oscillator speed will vary with temperature
[3] Device will operate down to 0.9V but with degraded system specifications
[4] DSP core active; single channel; direct digital output enabled and connected to 100kΩ resistance

11.3 Analog Characteristics

Conditions: Temperature = 25°C, f_{SYS_CLK} = 1.28MHz (internal), f_{MCLK} = 1.28MHz, f_{SAMP} = 16kHz, V_{bat} = 1.8V

Table 12: Analog Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Stage						
Input voltage	Vin	AI0, AI1, AI2, AI3 inputs 0dB preamp gain	-1		1	Vp
Input impedance[5]	Rin	Preamplifier gain 12, 15, 18, 21, 24, 27, 30dB	385	550	715	kΩ
Input referred noise	IRN	Unweighted, 20Hz to 8kHz BW, 30dB preamp gain		3		µVrms
Input dynamic range		Unweighted, 20Hz to 8kHz BW, 0dB preamp gain		85		dB
Input THD+N		Unweighted, 20Hz to 8kHz BW, 0dB preamp gain, input at 1 kHz		-60		dB
Preamplifier gain tolerance (0, 12, 15, 18, 21, 24, 27, 30dB)		50% re. FS input at 1kHz	-1.5		1.5	dB
Output Stage						
Line out output level	Vlo	AI1	-1		1	Vp
Line out output impedance	Rlo	AI1		5		kΩ
Output impedance[6]	Rao	AO0. Attenuator = 12, 15, 18, 21, 24, 27, 30dB	8.9	12.8	16.6	kΩ
Output dynamic range		Unweighted, 100Hz to 22kHz BW, 0dB output attenuation		75		dB
Output THD+N		Unweighted, 100Hz to 22kHz BW, 0dB output attenuation, input at 1kHz		-60		dB
Output attenuator tolerance (0,12,15,18,21,24,27,30dB)		50% re. FS input at 1kHz	-2		2	dB
Low-Speed A/D						
Input voltage		Peak input voltage, HV mode	-0.3		2.1	V
Sampling frequency		All channels sequentially MCLK = 1.28MHz		12.8		kHz
Channel frequency		8 channels		1.6		kHz
Anti-Aliasing Filters (Input and Output)						
Cut-off frequencies			7	10	13	kHz
Passband flatness			-1		1	dB
Stopband attenuation				80		dB

[5] Depends slightly on the preamp gain
[6] Depends strongly on the attenuator

11.4 Digital Characteristics

Conditions: Temperature = 25°C, f_{SYS_CLK} = 1.28MHz (internal), f_{MCLK} = 1.28MHz, f_{SAMP} = 16kHz, V_{bat} = 1.8V

Table 13: Digital Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Stage						
Direct digital output load current	Ido				25	mA
Direct digital output resistance	Rdo			10	20	Ω
Direct digital output 0 dynamic range		Unweighted, 100Hz to 22kHz BW		77		dB
Direct digital output 0 THD+N		Unweighted, 100Hz to 10kHz BW input at 1kHz		-63		dB
Direct digital output 1 dynamic range		Unweighted, 100Hz to 22kHz BW		75		dB
Direct digital output 1 THD+N		Unweighted, 100Hz to 10kHz BW input at 1kHz		-62		dB
Internal Oscillator Characteristics						
Clock frequency (internal)	f_{SYS_CLK}			1.28		MHz
Oscillator jitter				0.4	1.0	ns
Oscillator start-up voltage			0.55	0.7	0.85	V
Oscillator settling time		Time required for frequency change of ±20%		1		ms
Other						
Clock frequency (external)	f_{SYS_CLK}	HV mode			33	MHz
High-level input voltage	VIH[7]		1.45	1.8	2.0	V
Low-level input voltage	VIL[7]			0	0.35	V
High-level output voltage Rout = 50ohm	VOH[7]	Isource = 1mA	1.45	1.8		V
Low-level output voltage Rout = 50ohm	VOL	Isink = 1mA		0.05	0.1	V
Input capacitance (digital I/O pads)	CIN				5	pF
Output capacitance (digital I/O pads)	COUT	Maximum load			100	pF
Pull-up resistors	Rup		215	430	645	KΩ
Pull-down resistors	Rdown		215	430	645	kΩ

[7] Digital low (0) represented below 20% of Vbat. Digital high (1) represented above 80% of Vbat.

12.0 Timing Diagrams

12.1 PCM Interface Timing Diagrams

12.1.1. 16-bit

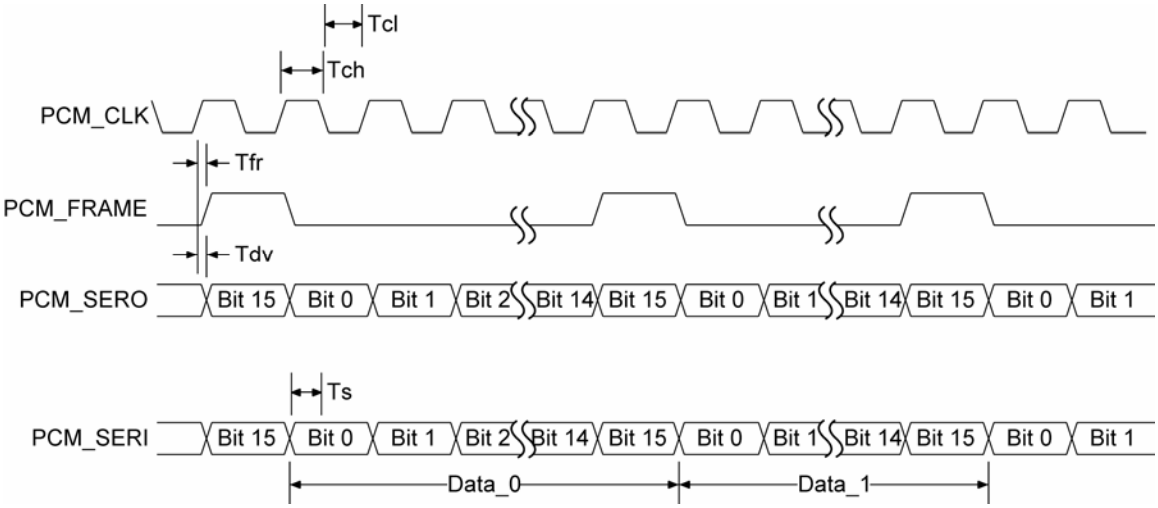


Figure 14: LSB Advanced Short

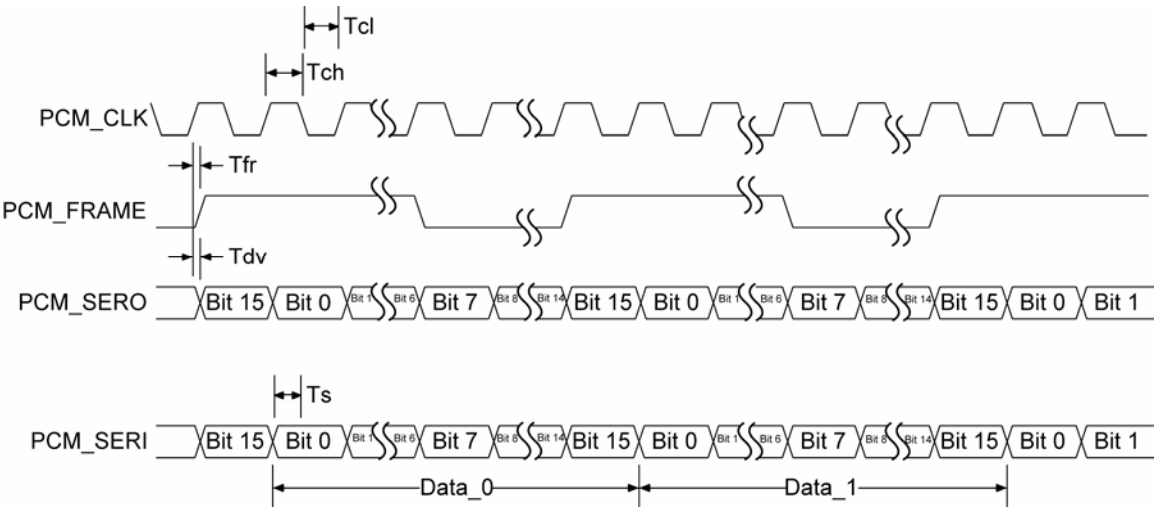


Figure 15: LSB Advanced Wide

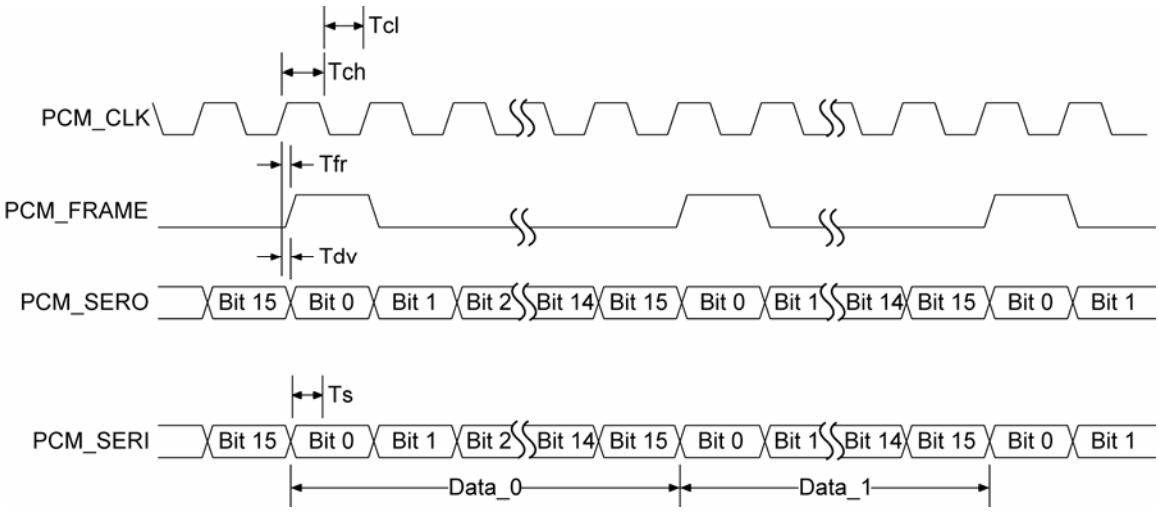


Figure 16: LSB Del Short

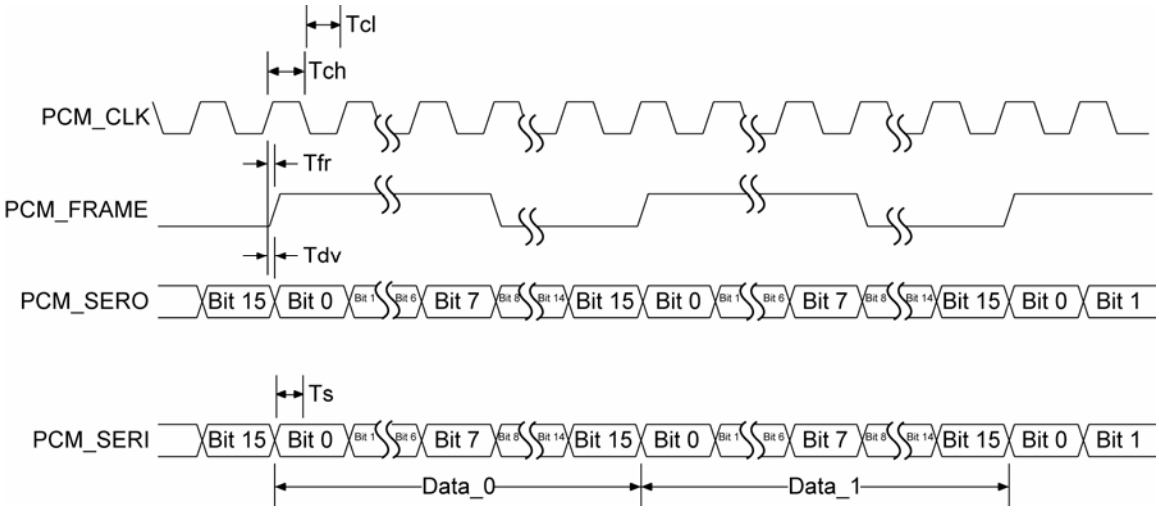


Figure 17: LSB Del Wide

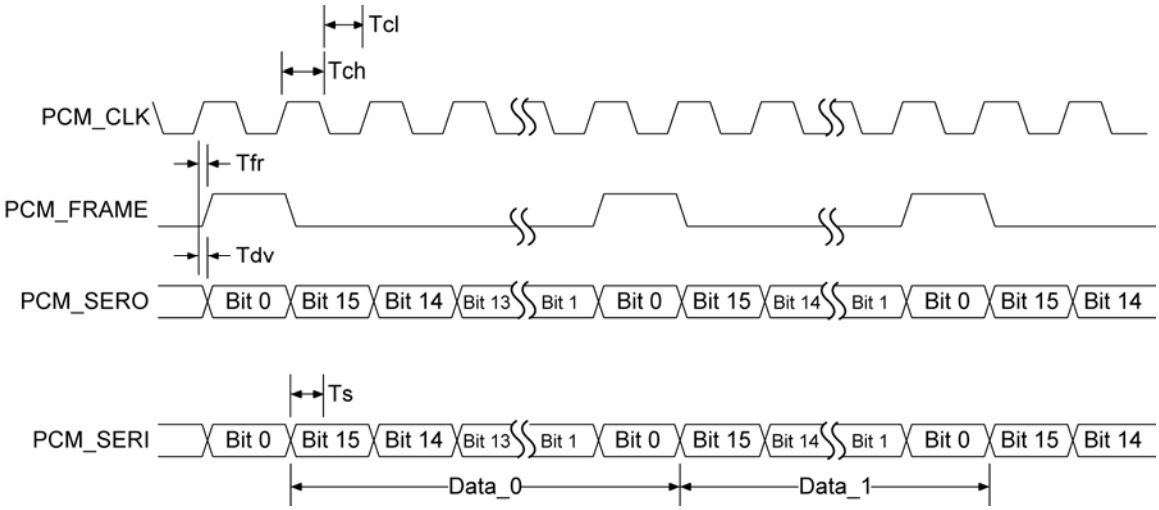


Figure 18: MSB Advanced Short

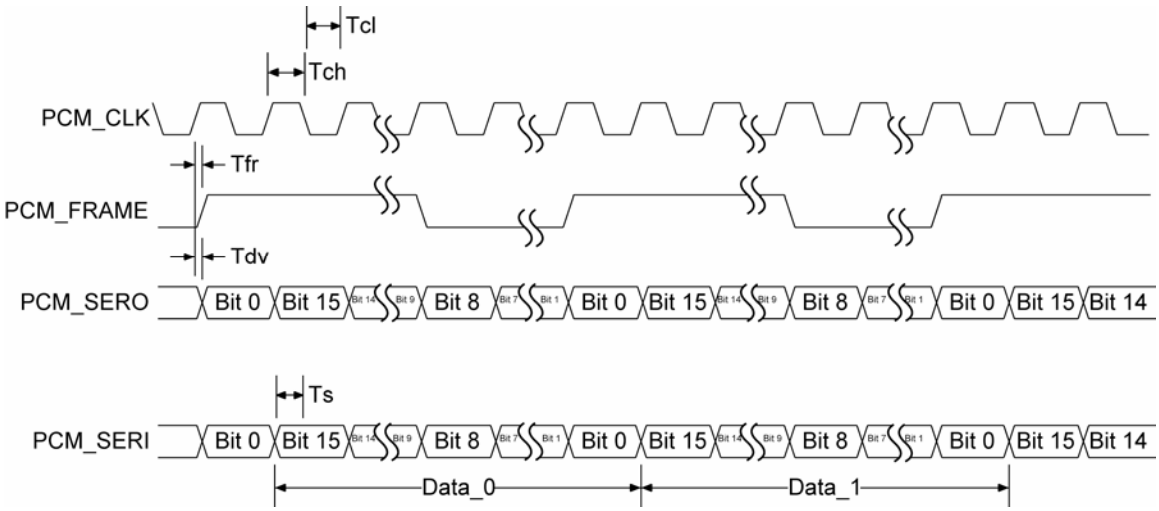


Figure 19: MSB Advanced Wide

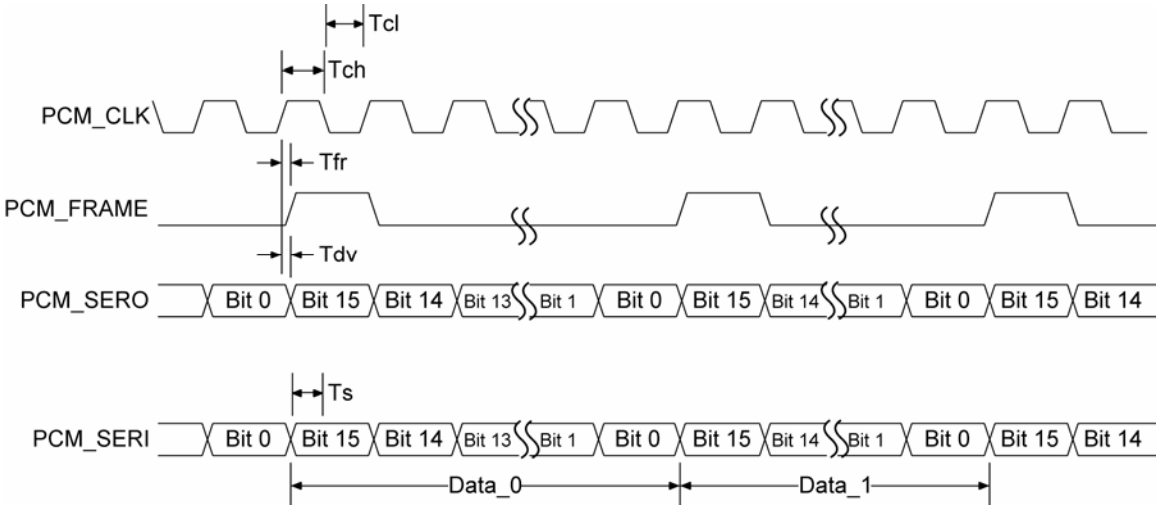


Figure 20: MSB Del Short

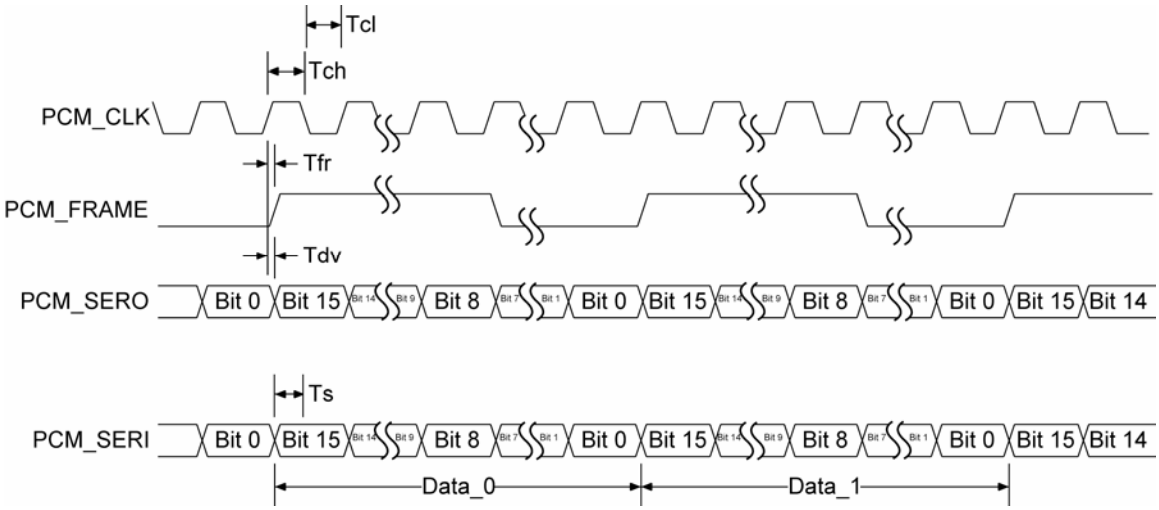


Figure 21: MSB Del Wide

12.1.2. 32-bit

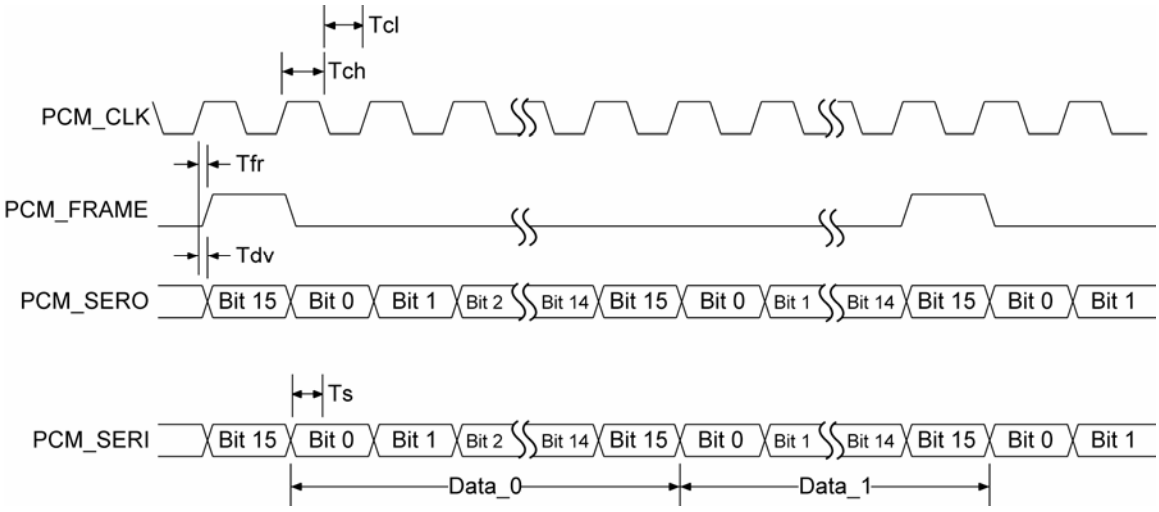


Figure 22: LSB Advanced Short

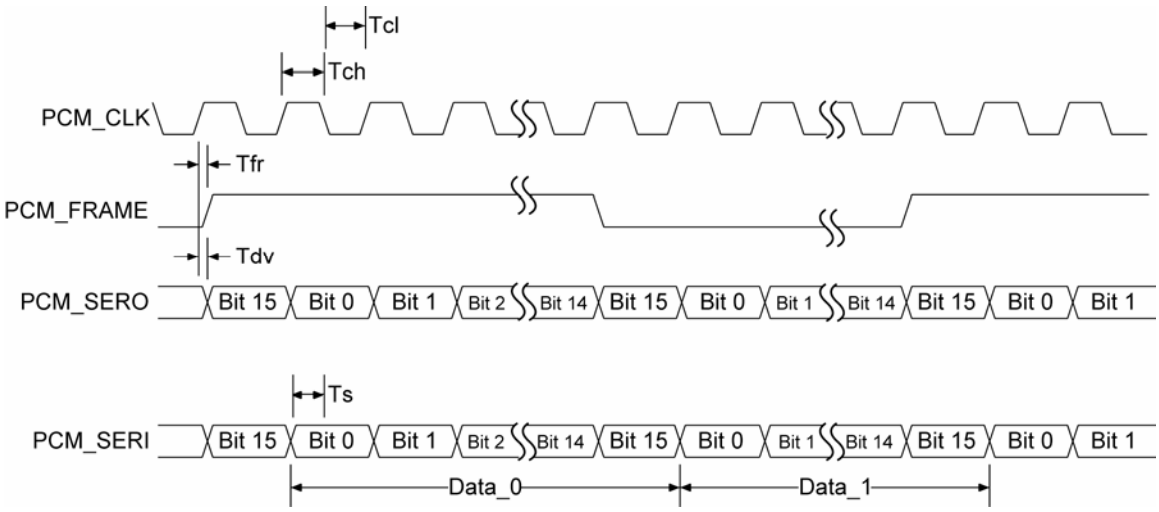


Figure 23: LSB Advanced Wide

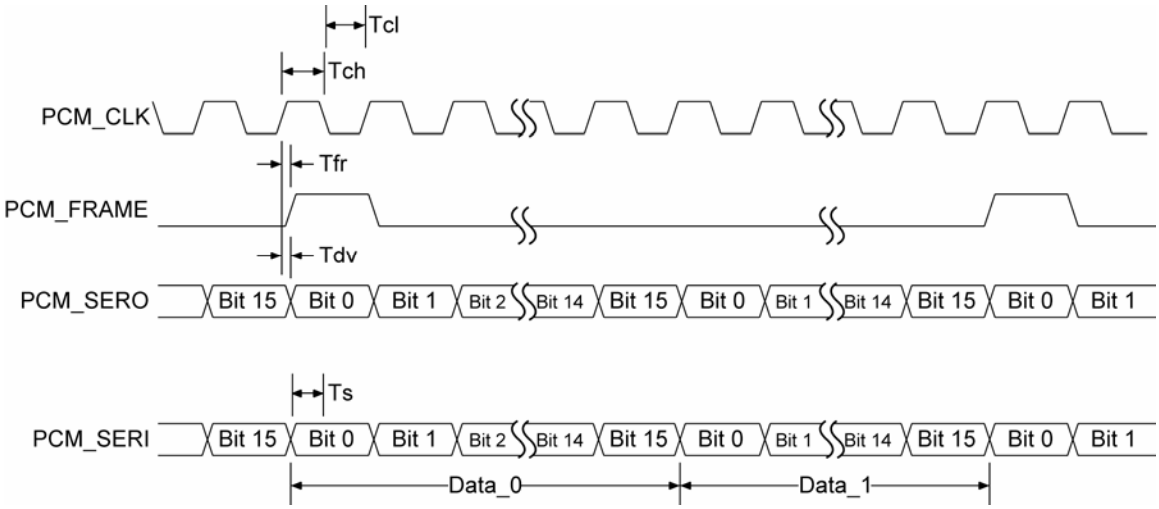


Figure 24: LSB Del Short

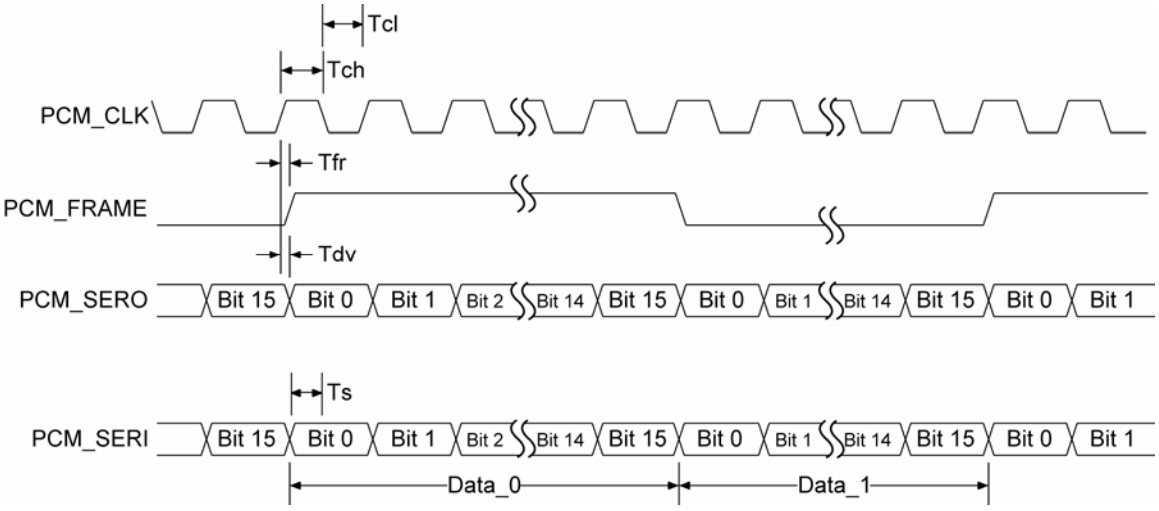


Figure 25: LSB Del Wide

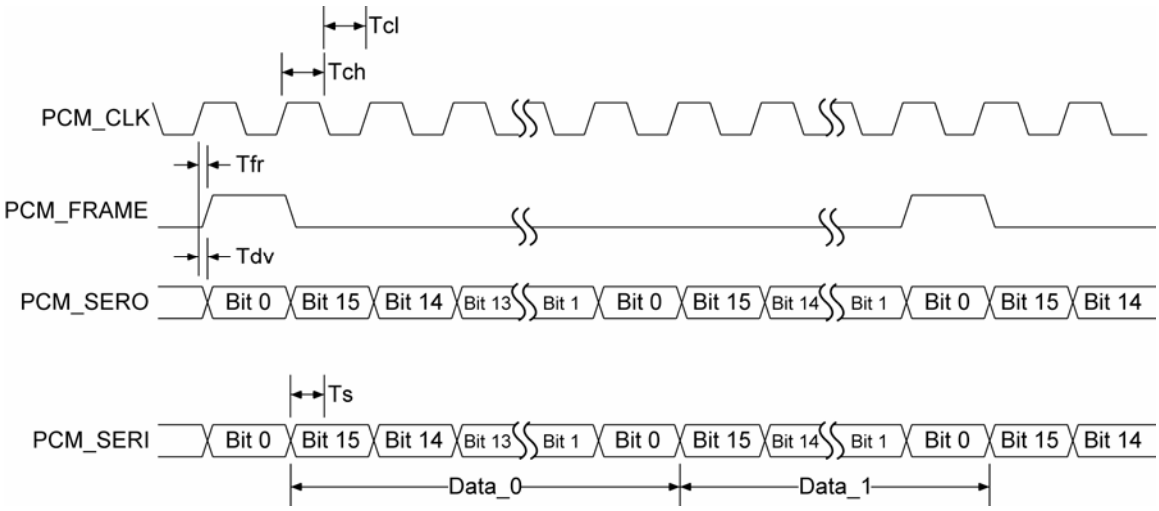


Figure 26: MSB Advanced Short

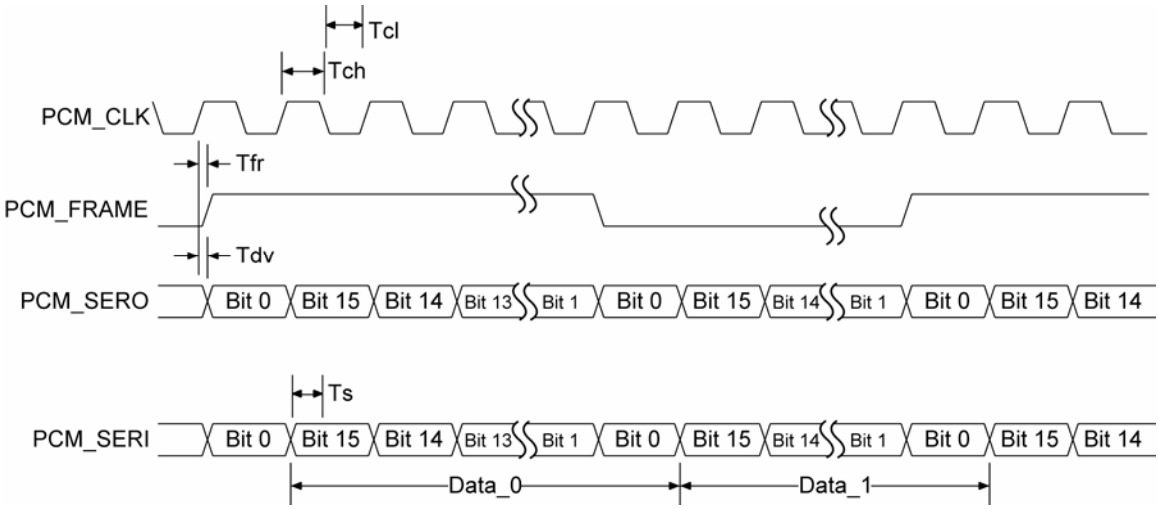


Figure 27: MSB Advanced Wide

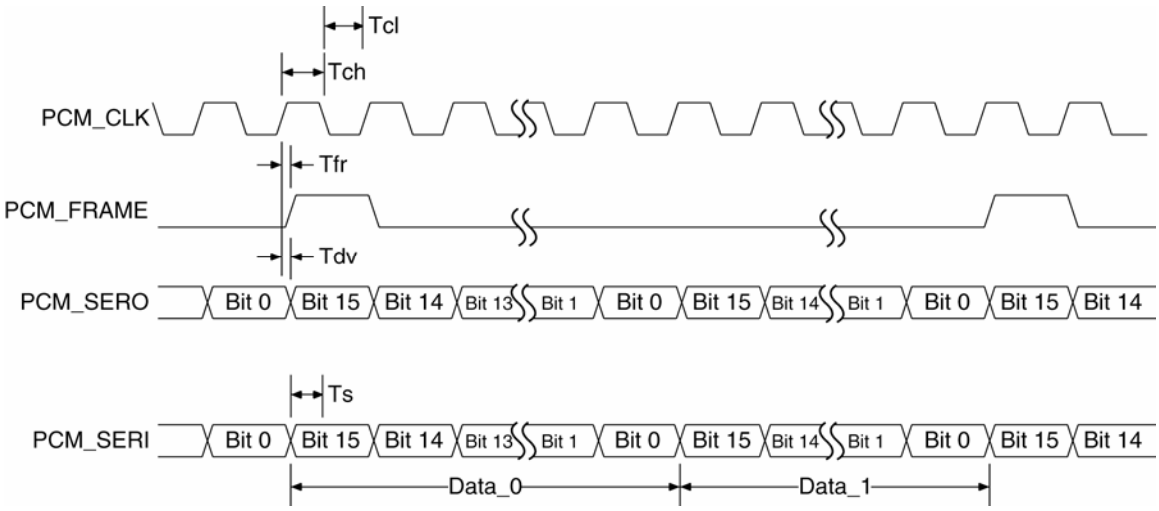


Figure 28: MSB Del Short

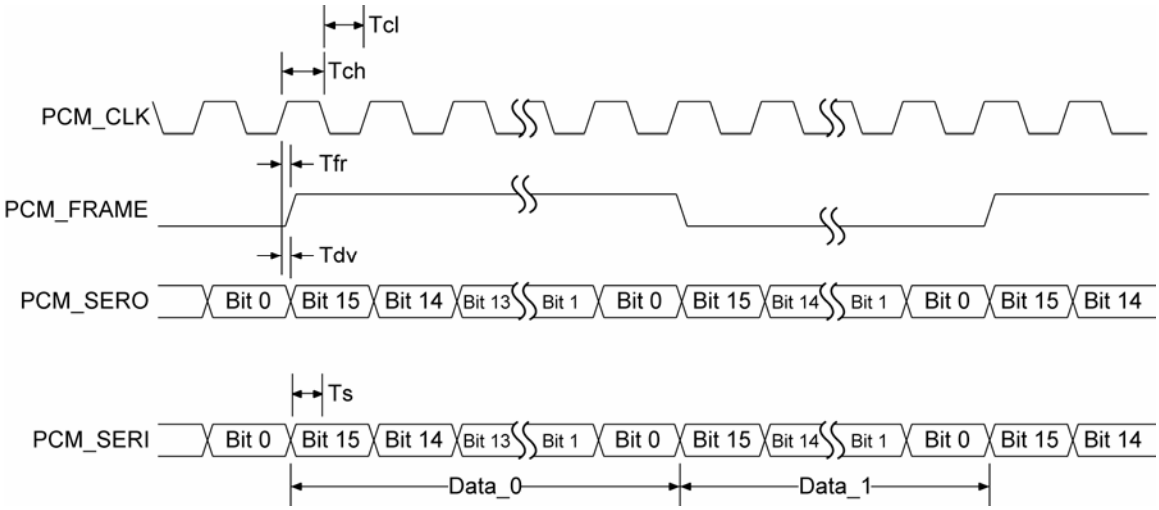


Figure 29: MSB Del Wide

Table 14: PCM Interface Descriptions

Parameter	Description	Min.	Max.	Unit
T_{dv}	PCM_CLK high to data valid		50	ns
T_s	Setup time before PCM_CLK high		10	ns
T_{fr}	PCM_CLK high to PCM_FRAME high		50	ns
T_{ch}	PCM_CLK high period (1.28MHz)		390	ns
T_{cl}	PCM_CLK low period (1.28MHz)		390	ns

12.2 GPIO Timing Diagram

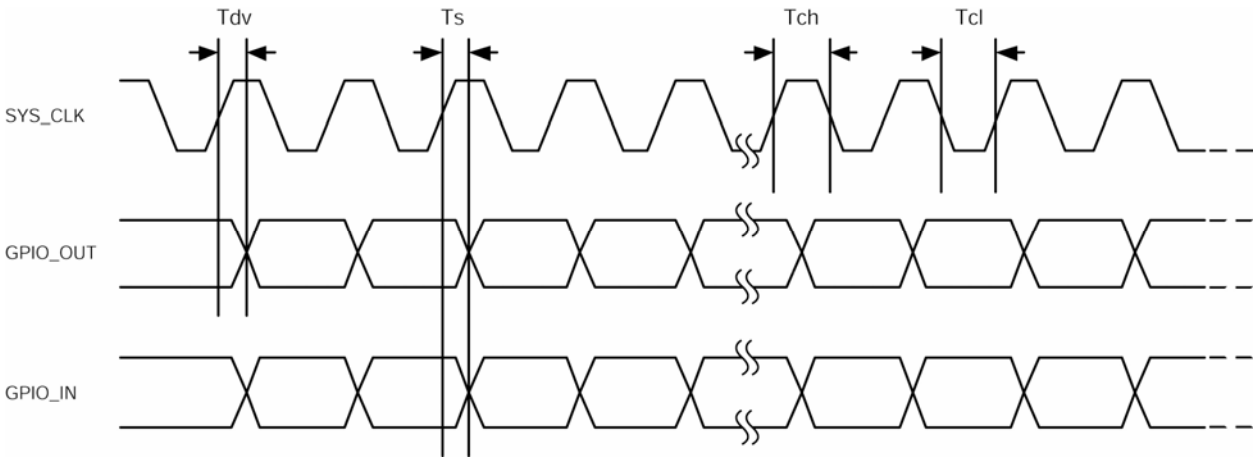


Figure 30: GPIO Timing Diagram

Table 15: GPIO Interface Descriptions

Parameter	Description	Min.	Max.	Unit
T_{dv}	SYS_CLK high to data valid		50	ns
T_s	Setup time before SYS_CLK high		10	ns
T_{ch}	SYS_CLK high period (1.28MHz)		390	ns
T_{cl}	SYS_CLK low period (1.28MHz)		390	ns

12.3 SPI Port Timing Diagram

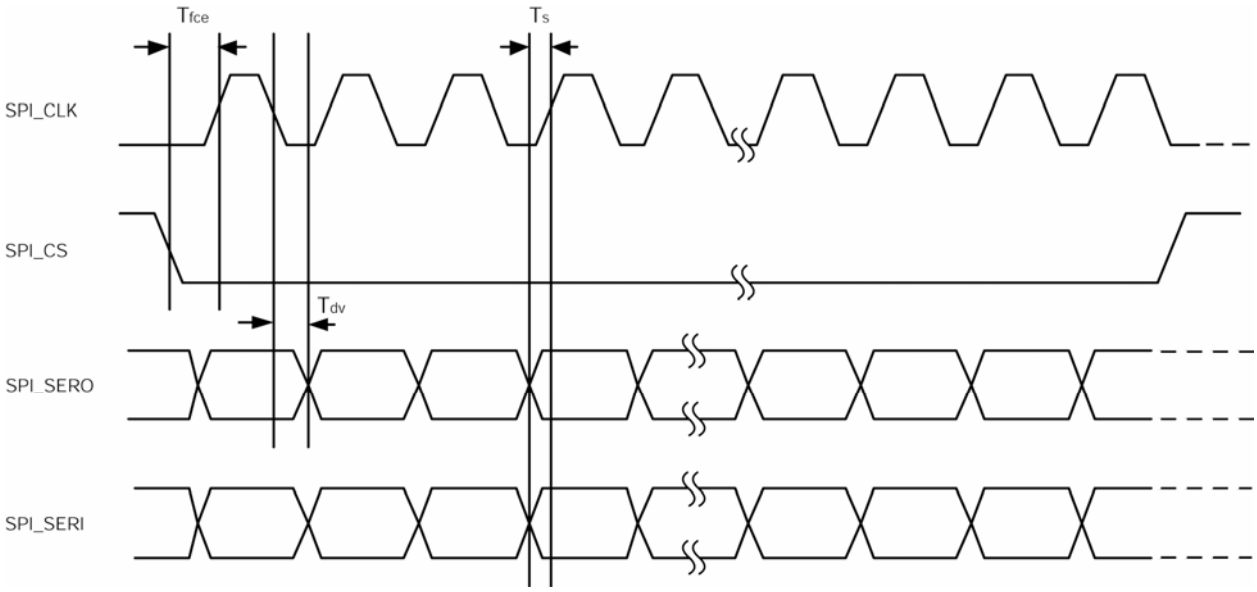


Figure 31: SPI Port Timing Diagram

Table 16: SPI Interface Descriptions

Parameter	Description	Min.	Max.	Unit
T_{dv}	SPI_CLK high to output data valid		50	ns
T_s	Setup time before SPI_CLK high		10	ns
T_{fce}	SPI_CS low to first SPI_CLK high			ns

13.0 Re-flow Information

The re-flow profile depends on the equipment that is used for the reflow and the assembly that is being reflowed. Use the following table from the JEDEC Standard 22-A113D Para 3.1.6 for Sn-Pb Eutectic Assembly as a guideline:

Table 17: Re-flow Information

Profile Feature	Sn-Pb Eutectic Assembly	Pb-free Assembly
Average Ramp-Up Rate (TL to TP)	3°C/second maximum	3°C/second maximum
Preheat		
Temperature minimum (TSMIN)	100°C	150°C
Temperature maximum (TSMAX)	150°C	200°C
Time (min. to max.) (ts)	60-120 seconds	60-180 seconds
TSMAX to TL		
Ramp-up rate		3°C/second maximum
Time Maintained Above		
Temperature (TL)	183°C	217°C
Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature (TP)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of Actual Peak Temperature	10-30 seconds	10-30 seconds
Ramp-Down Rate	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

All BelaSigna 200 QFNs with part number revisions 003 (i.e. 0W344-003-XTP) and higher are Pb-free and should follow the re-flow guidelines for Pb-free assemblies. All BelaSigna 200 CSPs are Pb-free.

14.0 ESD Sensitive Device

CAUTION: Electrostatic discharge (ESD) sensitive device. Permanent damage may occur on devices subjected to high-energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

15.0 Training

To facilitate development on the BelaSigna 200 platform, training is available upon request. Contact your account manager for more information.

16.0 Ordering Information

Part Number	Package	Shipping Configuration	Temperature Range
0W344-004-XTP	8x8mm QFN	Tape & Reel (500 parts per reel)	-85 to 40 °C
0W344-005-XTP	8x8mm QFN	Tape & Reel (1000 parts per reel)	-85 to 40 °C
0W588-002-XUA	2.3x2.8mm WLCSP	Tape & Reel (5000 parts per reel)	-85 to 40 °C

17.0 Company or Product Inquiries

For more information about ON Semiconductor's products or services visit our Web site at http://onsemi.com.

PUBLICATION ORDERING INFORMATION

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