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MAX 10 FPGA Device Overview

M10-OVERVIEW
2017.02.21

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1 MAX[®] 10 FPGA Device Overview

MAX[®] 10 devices are single-chip, non-volatile low-cost programmable logic devices (PLDs) to integrate the optimal set of system components.

The highlights of the MAX 10 devices include:

- Internally stored dual configuration flash
- User flash memory
- Instant on support
- Integrated analog-to-digital converters (ADCs)
- Single-chip Nios II soft core processor support

MAX 10 devices are the ideal solution for system management, I/O expansion, communication control planes, industrial, automotive, and consumer applications.

Related Links

[MAX 10 FPGA Device Datasheet](#)

1.1 Key Advantages of MAX 10 Devices

Table 1. Key Advantages of MAX 10 Devices

| Advantage | Supporting Feature |
|--------------------------------|--|
| Simple and fast configuration | Secure on-die flash memory enables device configuration in less than 10 ms |
| Flexibility and integration | <ul style="list-style-type: none"> • Single device integrating PLD logic, RAM, flash memory, digital signal processing (DSP), ADC, phase-locked loop (PLL), and I/Os • Small packages available from 3 mm × 3 mm |
| Low power | <ul style="list-style-type: none"> • Sleep mode—significant standby power reduction and resumption in less than 1 ms • Longer battery life—resumption from full power-off in less than 10 ms |
| 20-year-estimated life cycle | Built on TSMC's 55 nm embedded flash process technology |
| High productivity design tools | <ul style="list-style-type: none"> • Quartus[®] Prime Lite edition (no cost license) • Qsys system integration tool • DSP Builder for Intel[®] FPGAs • Nios[®] II Embedded Design Suite (EDS) |

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1.2 Summary of MAX 10 Device Features

Table 2. Summary of Features for MAX 10 Devices

| Feature | Description |
|---|--|
| Technology | 55 nm TSMC Embedded Flash (Flash + SRAM) process technology |
| Packaging | <ul style="list-style-type: none"> • Low cost, small form factor packages—support multiple packaging technologies and pin pitches • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS6-compliant |
| Core architecture | <ul style="list-style-type: none"> • 4-input look-up table (LUT) and single register logic element (LE) • LEs arranged in logic array block (LAB) • Embedded RAM and user flash memory • Clocks and PLLs • Embedded multiplier blocks • General purpose I/Os |
| Internal memory blocks | <ul style="list-style-type: none"> • M9K—9 kilobits (Kb) memory blocks • Cascadable blocks to create RAM, dual port, and FIFO functions |
| User flash memory (UFM) | <ul style="list-style-type: none"> • User accessible non-volatile storage • High speed operating frequency • Large memory size • High data retention • Multiple interface option |
| Embedded multiplier blocks | <ul style="list-style-type: none"> • One 18 × 18 or two 9 × 9 multiplier modes • Cascadable blocks enabling creation of filters, arithmetic functions, and image processing pipelines |
| ADC | <ul style="list-style-type: none"> • 12-bit successive approximation register (SAR) type • Up to 17 analog inputs • Cumulative speed up to 1 million samples per second (MSPS) • Integrated temperature sensing capability |
| Clock networks | <ul style="list-style-type: none"> • Global clocks support • High speed frequency in clock network |
| Internal oscillator | Built-in internal ring oscillator |
| PLLs | <ul style="list-style-type: none"> • Analog-based • Low jitter • High precision clock synthesis • Clock delay compensation • Zero delay buffering • Multiple output taps |
| General-purpose I/Os (GPIOs) | <ul style="list-style-type: none"> • Multiple I/O standards support • On-chip termination (OCT) • Up to 830 megabits per second (Mbps) LVDS receiver, 800 Mbps LVDS transmitter |
| External memory interface (EMIF) ¹ | Supports up to 600 Mbps external memory interfaces: |

continued...

¹ EMIF is only supported in selected MAX 10 device density and package combinations. Refer to the *External Memory Interface User Guide* for more information.



| Feature | Description |
|-------------------------------|---|
| | <ul style="list-style-type: none"> • DDR3, DDR3L, DDR2, LPDDR2 (on 10M16, 10M25, 10M40, and 10M50.) • SRAM (Hardware support only) <p><i>Note:</i> For 600 Mbps performance, -6 device speed grade is required. Performance varies according to device grade (commercial, industrial, or automotive) and device speed grade (-6 or -7). Refer to the <i>MAX 10 Device Data Sheet</i> or <i>External Memory Interface Spec Estimator</i> for more details.</p> |
| Configuration | <ul style="list-style-type: none"> • Internal configuration • JTAG • Advanced Encryption Standard (AES) 128-bit encryption and compression options • Flash memory data retention of 20 years at 85 °C |
| Flexible power supply schemes | <ul style="list-style-type: none"> • Single- and dual-supply device options • Dynamically controlled input buffer power down • Sleep mode for dynamic power reduction |

1.3 MAX 10 Device Ordering Information

Figure 1. Sample Ordering Code and Available Options for MAX 10 Devices



Note: The -I6 and -A6 speed grades of the MAX 10 FPGA devices are not available by default in the Quartus Prime software. Contact your local Intel sales representatives for support.

Related Links

[Intel FPGA Product Selector](#)

Provides the latest information about Intel FPGAs.



1.3.1 MAX 10 Device Feature Options

Table 3. Feature Options for MAX 10 Devices

| Option | Feature |
|---------|--|
| Compact | Devices with core architecture featuring single configuration image with self-configuration capability |
| Flash | Devices with core architecture featuring: <ul style="list-style-type: none"> • Dual configuration image with self-configuration capability • Remote system upgrade capability • Memory initialization |
| Analog | Devices with core architecture featuring: <ul style="list-style-type: none"> • Dual configuration image with self-configuration capability • Remote system upgrade capability • Memory initialization • Integrated ADC |

1.4 MAX 10 Device Maximum Resources

Table 4. Maximum Resource Counts for MAX 10 Devices

| Resource | | Device | | | | | | |
|-------------------------------------|-----------------------|--------|-------|-------|-------|-------|-------|-------|
| | | 10M02 | 10M04 | 10M08 | 10M16 | 10M25 | 10M40 | 10M50 |
| Logic Elements (LE) (K) | | 2 | 4 | 8 | 16 | 25 | 40 | 50 |
| M9K Memory (Kb) | | 108 | 189 | 378 | 549 | 675 | 1,260 | 1,638 |
| User Flash Memory (Kb) ² | | 96 | 1,248 | 1,376 | 2,368 | 3,200 | 5,888 | 5,888 |
| 18 × 18 Multiplier | | 16 | 20 | 24 | 45 | 55 | 125 | 144 |
| PLL | | 2 | 2 | 2 | 4 | 4 | 4 | 4 |
| GPIO | | 160 | 246 | 250 | 320 | 360 | 500 | 500 |
| LVDS | Dedicated Transmitter | 9 | 15 | 15 | 22 | 24 | 30 | 30 |
| | Emulated Transmitter | 73 | 114 | 116 | 151 | 171 | 241 | 241 |
| | Dedicated Receiver | 73 | 114 | 116 | 151 | 171 | 241 | 241 |
| Internal Configuration Image | | 1 | 2 | 2 | 2 | 2 | 2 | 2 |
| ADC | | — | 1 | 1 | 1 | 2 | 2 | 2 |

² The maximum possible value including user flash memory and configuration flash memory. For more information, refer to [MAX 10 User Flash Memory User Guide](#).



1.5 MAX 10 Devices I/O Resources Per Package

Table 5. Package Plan for MAX 10 Single Power Supply Devices

| Device | Package | | | |
|--------|------------|----------------------|----------------------|----------------------|
| | Type | M153 153-pin MBGA | U169 169-pin UBGA | E144 144-pin EQFP |
| | Size | 8 mm × 8 mm | 11 mm × 11 mm | 22 mm × 22 mm |
| | Ball Pitch | 0.5 mm | 0.8 mm | 0.5 mm |
| 10M02 | | 112 | 130 | 101 |
| 10M04 | | 112 | 130 | 101 |
| 10M08 | | 112 | 130 | 101 |
| 10M16 | | — | 130 | 101 |
| 10M25 | | — | — | 101 |
| 10M40 | | — | — | 101 |
| 10M50 | | — | — | 101 |

Table 6. Package Plan for MAX 10 Dual Power Supply Devices

| Device | Package | | | | | | |
|--------|------------|------------------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| | Type | V36 36-pin WLCSP | V81 81-pin WLCSP | U324 324-pin UBGA | F256 256-pin FBGA | F484 484-pin FBGA | F672 672-pin FBGA |
| | Size | 3 mm × 3 mm | 4 mm × 4 mm | 15 mm × 15 mm | 17 mm × 17 mm | 23 mm × 23 mm | 27 mm × 27 mm |
| | Ball Pitch | 0.4 mm | 0.4 mm | 0.8 mm | 1.0 mm | 1.0 mm | 1.0 mm |
| 10M02 | | 27 | — | 160 | — | — | — |
| 10M04 | | — | — | 246 | 178 | — | — |
| 10M08 | | — | 56 | 246 | 178 | 250 | — |
| 10M16 | | — | — | 246 | 178 | 320 | — |
| 10M25 | | — | — | — | 178 | 360 | — |
| 10M40 | | — | — | — | 178 | 360 | 500 |
| 10M50 | | — | — | — | 178 | 360 | 500 |

Related Links

- [MAX 10 General Purpose I/O User Guide](#)
- [MAX 10 High-Speed LVDS I/O User Guide](#)

1.6 MAX 10 Vertical Migration Support

Vertical migration supports the migration of your design to other MAX 10 devices of different densities in the same package with similar I/O and ADC resources.

1.6.1 MAX 10 I/O Vertical Migration Support

Figure 2. Migration Capability Across MAX 10 Devices

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Some packages have several migration paths. Devices with lesser I/O resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os usage to match the product line with the lowest I/O count.

| Device | Package | | | | | | | | |
|--------|---------|-----|------|------|------|------|------|------|------|
| | V36 | V81 | M153 | U169 | U324 | F256 | E144 | F484 | F672 |
| 10M02 | | | ↑ | ↑ | ↑ | | | | |
| 10M04 | | | ↓ | ↓ | ↓ | ↑ | ↑ | | |
| 10M08 | | | | | | ↑ | ↑ | ↑ | |
| 10M16 | | | | ↓ | ↓ | | | | |
| 10M25 | | | | | | ↑ | ↓ | ↑ | |
| 10M40 | | | | | | ↑ | ↑ | ↑ | ↑ |
| 10M50 | | | | | | ↓ | ↓ | ↓ | ↓ |

Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

1.6.2 MAX 10 ADC Vertical Migration Support

Figure 3. ADC Vertical Migration Across MAX 10 Devices

The arrows indicate the ADC migration paths. The devices included in each vertical migration path are shaded.

| Device | Package | | | | | | |
|--------|---------|------|------|------|------|------|------|
| | M153 | U169 | U324 | F256 | E144 | F484 | F672 |
| 10M04 | ↑ | ↑ | ↑ | ↑ | ↑ | | |
| 10M08 | ↓ | | | | | ↑ | |
| 10M16 | | ↓ | ↓ | | | | |
| 10M25 | | | | ↑ | ↓ | ↑ | |
| 10M40 | | | | ↑ | ↑ | ↑ | ↑ |
| 10M50 | | | | ↓ | ↓ | ↓ | ↓ |

- Dual ADC Device:** Each ADC (ADC1 and ADC2) supports 1 dedicated analog input pin and 8 dual function pins.
- Single ADC Device:** Single ADC that supports 1 dedicated analog input pin and 16 dual function pins.
- Single ADC Device:** Single ADC that supports 1 dedicated analog input pin and 8 dual function pins.



Table 7. Pin Migration Conditions for ADC Migration

| Source | Target | Migratable Pins |
|-------------------|-------------------|--|
| Single ADC device | Single ADC device | You can migrate all ADC input pins |
| Dual ADC device | Dual ADC device | |
| Single ADC device | Dual ADC device | <ul style="list-style-type: none"> One dedicated analog input pin. Eight dual function pins from the ADC1 block of the source device to the ADC1 block of the target device. |
| Dual ADC device | Single ADC device | |

1.7 Logic Elements and Logic Array Blocks

The LAB consists of 16 logic elements (LE) and a LAB-wide control block. An LE is the smallest unit of logic in the MAX 10 device architecture. Each LE has four inputs, a four-input look-up table (LUT), a register, and output logic. The four-input LUT is a function generator that can implement any function with four variables.

Figure 4. MAX 10 Device Family LEs



1.8 Analog-to-Digital Converter

MAX 10 devices feature up to two ADCs. You can use the ADCs to monitor many different signals, including on-chip temperature.

Table 8. ADC Features

| Feature | Description |
|--|--|
| 12-bit resolution | <ul style="list-style-type: none"> Translates analog signal to digital data for information processing, computing, data transmission, and control systems Provides a 12-bit digital representation of the observed analog signal |
| Up to 1 MSPS sampling rate | Monitors single-ended external inputs with a cumulative sampling rate of 25 kilosamples per second to 1 MSPS in normal mode |
| Up to 17 single-ended external inputs for single ADC devices | One dedicated analog and 16 dual function input pins |
| Up to 18 single-ended external inputs for dual ADC devices | <ul style="list-style-type: none"> One dedicated analog and eight dual-function input pins in each ADC block Simultaneous measurement capability for dual ADC devices |
| On-chip temperature sensor | Monitors external temperature data input with a sampling rate of up to 50 kilosamples per second |

1.9 User Flash Memory

The user flash memory (UFM) block in MAX 10 devices stores non-volatile information.

UFM provides an ideal storage solution that you can access using Avalon Memory-Mapped (Avalon-MM) slave interface protocol.

Table 9. UFM Features

| Features | Capacity |
|---------------------|---|
| Endurance | Counts to at least 10,000 program/erase cycles |
| Data retention | <ul style="list-style-type: none"> 20 years at 85 °C 10 years at 100 °C |
| Operating frequency | Maximum 116 MHz for parallel interface and 7.25 MHz for serial interface |
| Data length | Stores data up to 32 bits length in parallel |

1.10 Embedded Multipliers and Digital Signal Processing Support

MAX 10 devices support up to 144 embedded multiplier blocks. Each block supports one individual 18 × 18-bit multiplier or two individual 9 × 9-bit multipliers.

With the combination of on-chip resources and external interfaces in MAX 10 devices, you can build DSP systems with high performance, low system cost, and low power consumption.

You can use the MAX 10 device on its own or as a DSP device co-processor to improve price-to-performance ratios of DSP systems.

You can control the operation of the embedded multiplier blocks using the following options:

- Parameterize the relevant IP cores with the Quartus Prime parameter editor
- Infer the multipliers directly with VHDL or Verilog HDL

System design features provided for MAX 10 devices:



- DSP IP cores:
 - Common DSP processing functions such as finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions
 - Suites of common video and image processing functions
- Complete reference designs for end-market applications
- DSP Builder for Intel FPGAs interface tool between the Quartus Prime software and the MathWorks Simulink and MATLAB design environments
- DSP development kits

1.11 Embedded Memory Blocks

The embedded memory structure consists of M9K memory blocks columns. Each M9K memory block of a MAX 10 device provides 9 Kb of on-chip memory capable of operating at up to 284 MHz. The embedded memory structure consists of M9K memory blocks columns. Each M9K memory block of a MAX 10 device provides 9 Kb of on-chip memory. You can cascade the memory blocks to form wider or deeper logic structures.

You can configure the M9K memory blocks as RAM, FIFO buffers, or ROM.

The MAX 10 device memory blocks are optimized for applications such as high throughput packet processing, embedded processor program, and embedded data storage.

Table 10. M9K Operation Modes and Port Widths

| Operation Modes | Port Widths |
|------------------|--|
| Single port | ×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36 |
| Simple dual port | ×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36 |
| True dual port | ×1, ×2, ×4, ×8, ×9, ×16, and ×18 |

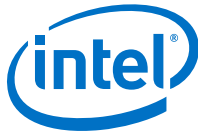
1.12 Clocking and PLL

MAX 10 devices offer the following resources: global clock (GCLK) networks and phase-locked loops (PLLs) with a 116-MHz built-in oscillator.

MAX 10 devices support up to 20 global clock (GCLK) networks with operating frequency up to 450 MHz. The GCLK networks have high drive strength and low skew.

The PLLs provide robust clock management and synthesis for device clock management, external system clock management, and I/O interface clocking. The high precision and low jitter PLLs offers the following features:

- Reduction in the number of oscillators required on the board
- Reduction in the device clock pins through multiple clock frequency synthesis from a single reference clock source
- Frequency synthesis
- On-chip clock de-skew
- Jitter attenuation
- Dynamic phase-shift



- Zero delay buffer
- Counter reconfiguration
- Bandwidth reconfiguration
- Programmable output duty cycle
- PLL cascading
- Reference clock switchover
- Driving of the ADC block

1.13 FPGA General Purpose I/O

The MAX 10 I/O buffers support a range of programmable features.

These features increase the flexibility of I/O utilization and provide an alternative to reduce the usage of external discrete components such as a pull-up resistor and a PCI clamp diode.

1.14 External Memory Interface

Dual-supply MAX 10 devices feature external memory interfaces solution that uses the I/O elements on the right side of the devices together with the UniPHY IP.

With this solution, you can create external memory interfaces to 16-bit SDRAM components with error correction coding (ECC).

Note: The external memory interface feature is available only for dual-supply MAX 10 devices.

Table 11. External Memory Interface Performance

| External Memory Interface ³ | I/O Standard | Maximum Width | Maximum Frequency (MHz) |
|--|--------------|--------------------|-------------------------|
| DDR3 SDRAM | SSTL-15 | 16 bit + 8 bit ECC | 303 |
| DDR3L SDRAM | SSTL-135 | 16 bit + 8 bit ECC | 303 |
| DDR2 SDRAM | SSTL-18 | 16 bit + 8 bit ECC | 200 |
| LPDDR2 SDRAM | HSUL-12 | 16 bit without ECC | 200 ⁴ |

Related Links

[External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in Intel FPGAs.

3 The device hardware supports SRAM. Use your own design to interface with SRAM devices.

4 To achieve the specified performance, constrain the memory device I/O and core power supply variation to within $\pm 3\%$. By default, the frequency is 167 MHz.



1.15 Configuration

Table 12. Configuration Features

| Feature | Description |
|--------------------------------|--|
| Dual configuration | <ul style="list-style-type: none"> Stores two configuration images in the configuration flash memory (CFM) Selects the first configuration image to load using the CONFIG_SEL pin |
| Design security | <ul style="list-style-type: none"> Supports 128-bit key with non-volatile key programming Limits access of the JTAG instruction during power-up in the JTAG secure mode Unique device ID for each MAX 10 device |
| SEU Mitigation | <ul style="list-style-type: none"> Auto-detects cyclic redundancy check (CRC) errors during configuration Provides optional CRC error detection and identification in user mode |
| Dual-purpose configuration pin | <ul style="list-style-type: none"> Functions as configuration pins prior to user mode Provides options to be used as configuration pin or user I/O pin in user mode |
| Configuration data compression | <ul style="list-style-type: none"> Decompresses the compressed configuration bitstream data in real-time during configuration Reduces the size of configuration image stored in the CFM |
| Instant-on | Provides the fastest power-up mode for MAX 10 devices. |

Table 13. Configuration Schemes for MAX 10 Devices

| Configuration Scheme | Compression | Encryption | Dual Image Configuration | Data Width |
|------------------------|-------------|------------|--------------------------|------------|
| Internal Configuration | Yes | Yes | Yes | — |
| JTAG | — | — | — | 1 |

1.16 Power Management

Table 14. Power Options

| Power Options | Advantage |
|------------------------------------|--|
| Single-supply device | Saves board space and costs. |
| Dual-supply device | <ul style="list-style-type: none"> Consumes less power Offers higher performance |
| Power management controller scheme | <ul style="list-style-type: none"> Reduces dynamic power consumption when certain applications are in standby mode Provides a fast wake-up time of less than 1 ms. |

1.17 Document Revision History for MAX 10 FPGA Device Overview

| Date | Version | Changes |
|---------------------|------------|--|
| February 2017 | 2017.02.21 | <ul style="list-style-type: none"> Rebranded as Intel. |
| December 2016 | 2016.12.20 | <ul style="list-style-type: none"> Updated EMIF information in the <i>Summary of Features for MAX 10 Devices</i> table. EMIF is only supported in selected MAX 10 device density and package combinations, and for 600 Mbps performance, -6 device speed grade is required. Updated the device ordering information to include P for leaded package. |
| <i>continued...</i> | | |



| Date | Version | Changes |
|----------------|------------|---|
| May 2016 | 2016.05.02 | <ul style="list-style-type: none"> • Removed all preliminary marks. • Update the ADC sampling rate description. The ADC feature monitors single-ended external inputs with a cumulative sampling rate of 25 kilosamples per second to 1 MSPS in normal mode. |
| November 2015 | 2015.11.02 | <ul style="list-style-type: none"> • Removed SF feature from the device ordering information figure. • Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>. |
| May 2015 | 2015.05.04 | <ul style="list-style-type: none"> • Added clearer descriptions for the feature options listed in the device ordering information figure. • Updated the maximum dedicated LVDS transmitter count of 10M02 device from 10 to 9. • Removed the F672 package of the MAX 10 10M25 device : <ul style="list-style-type: none"> – Updated the devices I/O resources per package. – Updated the I/O vertical migration support. – Updated the ADC vertical migration support. • Updated the maximum resources for 10M25 device: <ul style="list-style-type: none"> – Maximum GPIO from 380 to 360. – Maximum dedicated LVDS transmitter from 26 to 24. – Maximum emulated LVDS transmitter from 181 to 171. – Maximum dedicated LVDS receiver from 181 to 171. • Added ADC information for the E144 package of the 10M04 device. • Updated the ADC vertical migration diagram to clarify that there are single ADC devices with eight and 16 dual function pins. • Removed the note about contacting Altera for DDR3, DDR3L, DDR2, and LPDDR2 external memory interface support. The Quartus Prime software supports these external memory interfaces from version 15.0. |
| December 2014 | 2014.12.15 | <ul style="list-style-type: none"> • Changed terms: <ul style="list-style-type: none"> – "dual image" to "dual configuration image" – "dual-image configuration" to dual configuration" • Added memory initialization feature for Flash and Analog devices. • Added maximum data retention capacity of up to 20 years for UFM feature. • Added maximum operating frequency of 7.25 MHz for serial interface for UFM feature. |
| September 2014 | 2014.09.22 | Initial release. |