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PL 3170 Power Line Smart Transceivers
Models 15330R-1000 and 15330R-2500

- Combines an ANSI-709.2 compliant Power Line Transceiver with an ANSI 709.1 compliant Neuron® 3120 processor core
- Designed to comply with FCC, Industry Canada, Japan MPT, and European CENELEC EN 50065-1 power line communications regulations
- Supports CENELEC C-band operation
- Dual carrier frequency mode and digital signal processing
- 4K Bytes of embedded EEPROM for application code and configuration data
- 2K Bytes of embedded RAM for buffering network data and network variables
- Full duplex hardware UART and SPI serial interfaces
- 12 I/O pins with 38 programmable standard I/O modes to minimize external interface circuitry
- Includes Interoperable Self Installation (ISI) functions in the firmware image
- -40 to +85°C operating temperature range
- RoHS-compliant

Overview

The Power Line Smart Transceivers integrate a Neuron processor core with a power line transceiver, making them ideal for appliance, audio/video, lighting, heating/cooling, security, and irrigation applications. The PL 3170 Smart Transceiver is the latest addition to the family of Power Line Smart Transceivers. It includes Interoperable Self Installation (ISI) functions built into the firmware stored in the ROM so that complete 4KB of application space is available to the developer even when using ISI functions in the application. The Power Line Smart Transceivers feature a highly reliable narrow-band power line transceiver, an 8-bit Neuron processor core for running applications and managing network communications, a choice of on-board or external memory, and an extremely small form factor – all at a price that is compelling for even the most cost-sensitive consumer product applications.

A Global Product

Designed to Comply with FCC, Industry Canada, Japan MPT, and European CENELEC EN50065-1 regulations, the Power Line Smart Transceivers can be used in applications worldwide. The CENELEC access protocol, implemented in the Power Line Smart Transceivers, can be enabled or disabled by the user. This eliminates the need for users to develop the complex timing and access algorithms mandated under CENELEC EN50065-1.

Unmatched Performance

Intermittent noise sources, impedance changes, and attenuation make the power line a hostile signaling environment. The Power Line Smart Transceivers incorporate a variety of technical innovations to insure reliable operation:

- Unique dual carrier frequency feature automatically selects an alternate secondary communication frequency should the primary frequency be blocked by noise;
- Highly efficient, patented, low-overhead forward error correction (FEC) algorithm to overcome errors induced by noise;
- Sophisticated digital signal processing, noise cancellation, and distortion correction algorithms. These features correct for a wide variety of signaling impediments, including impulsive noise, continuous tone noise, and phase distortion;
- High output, low distortion external amplifier design that can deliver 1Ap-p into low impedance loads, eliminating the need for expensive phase couplers in typical residential applications.

The combination of these special features enable the Power Line Smart Transceivers to operate reliably in the presence of consumer electronics, power line intercoms, motor noise, electronic ballasts, dimmers, and other typical sources of interference. The Power Line Smart Transceivers can communicate over virtually any AC or DC power mains, as well as unpowered twisted pair, by way of a low-cost, external coupling circuit.

The PL 3170 Power Line Smart Transceiver is targeted at very low cost designs that require up to 4K Bytes of application code, and a compact 38 TSSOP package. The chip includes 4K Bytes of EEPROM and 2K Bytes of RAM. The Neuron system firmware and software application libraries are contained in on-chip ROM.

Applications that need more than 4KB of EEPROM can use PL 3150 Smart Transceiver. The PL 3150 Smart Transceiver allows applications to address up to 58KB of external memory (16KB

is dedicated to the Neuron system firmware) using a 64 LQFP package.

The PL 3170 Power Line Smart Transceiver operates at 10.0MHz and supports the CENELEC C-band, which is used for general purpose signaling and all non-utility related applications.

Application programs stored in the embedded EEPROM may be updated over the power line network. This valuable feature enables products to be updated without physically accessing them, i.e., from a local PC with a power line interface or from a remote service center through an i.LON® Internet Server. The embedded EEPROM may be written up to 10,000 times with no data loss. Data stored in the EEPROM will be retained for at least ten years.

Interoperable Self-Installation (ISI)

Interoperable Self-Installation is an application layer protocol that allows LonWorks devices to be self-installed automatically or at the push of a button. When using ISI, no network management tool is required to install the devices or manage the network configuration. ISI is a licensed protocol that can be used royalty-free when used with Echelon transceivers. The PL 3170 Power Line Smart Transceiver includes ISI library functions in the firmware image stored in the ROM. Some of the features of the ISI protocol are:

- Supports up to 32 devices for simple networks
- Supports up to 200 devices for networks with a simple domain address server
- Leverages LonMark standards to allow devices from different manufacturers to work together
- Enables network isolation for power line networks
- Installs simply and reliably, even if many devices are off when new ones are added
- Operates on top of the ANSI/CEA-709.1 (also known as ISO/CEN EN14908) Control Network Protocol
- Can transition to a managed network

Inexpensive Power Supply

The Power Line Smart Transceivers use +8.5 to +18VDC and +5VDC power supplies and support very low receive mode current consumption. The wide power supply range and very low receive power requirements allow the use of inexpensive power supplies.

Additionally, the Power Line Smart Transceivers incorporate a power management feature that constantly monitors the status of the device's power supply. If during transmission the power supply voltage falls to a level that is insufficient to ensure reliable signaling, the transceiver stops transmitting until the power supply voltage rises to an acceptable level. This unique feature allows the use of a power supply with one-third the current capacity otherwise required. The net result is a reduction in the size, cost, and thermal dissipation of the power supply. Power management is especially useful for high volume, low-cost consumer products such as electrical switches, motion detectors, outlets, light sensors, and dimmers.

Flexible I/O, Simple Configuration

The Power Line Smart Transceivers provide 12 I/O pins which can be configured to operate in one or more of 38 predefined standard input/output modes. Combining a wide range of I/O models with two on-board timer/counters enables the Power Line Smart Transceivers to interface with application circuits using minimal external logic or software development. The Power Line Smart Transceivers also feature a full duplex hardware UART supporting baud rates of up to 115kbps, and an SPI interface that operates up to 625kbps.

External Components

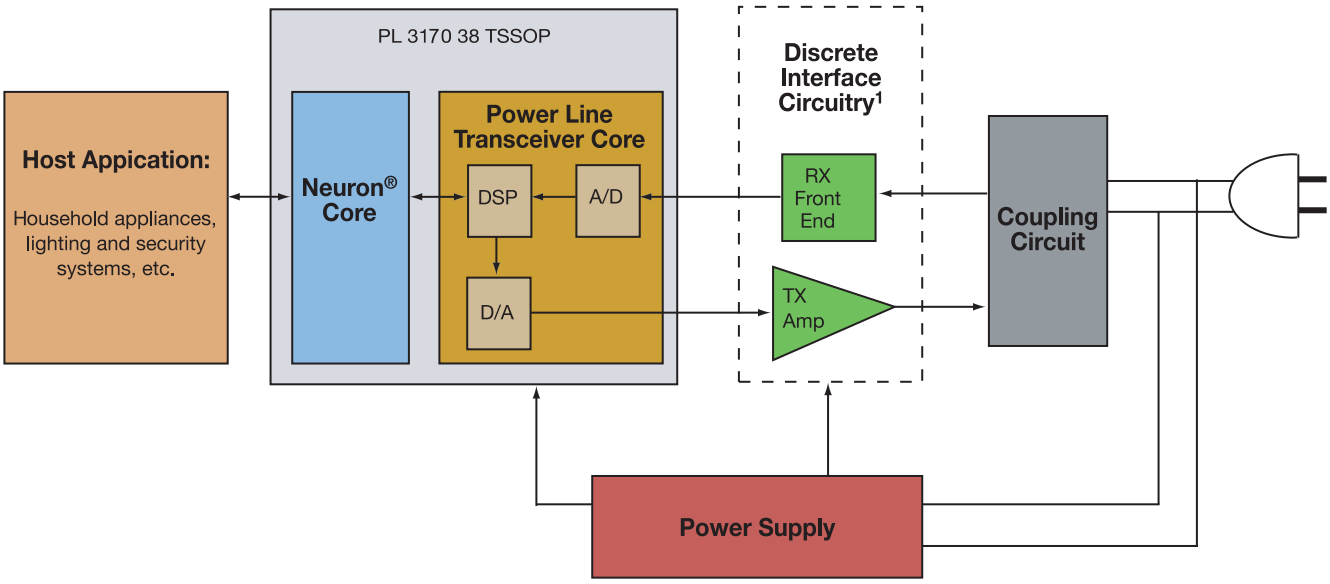
Only a small number of inexpensive external components are required to create a complete Power Line Smart Transceiver-based device (see the PL 3170 Power Line Smart Transceiver Block Diagram). These components include:

• Discrete interface circuitry comprised of roughly fifty components, primarily resistors and capacitors. This circuitry provides "front-end" filtering for the on-chip A/D, and implements the power amplifier that drives the on-chip D/A transmit signal onto the power line. Echelon offers a comprehensive Power Line Development Support Kit* (DSK) with which customers can implement this interface circuitry. Contact your salesperson for details about purchasing a PL DSK.

• Coupling circuit consisting of approximately ten components, mainly capacitors and inductors, which acts as a simple high-pass filter located between the Power Line Smart Transceiver and the power mains. This circuitry provides surge and line transient protection in addition to blocking the low frequency, 50Hz/60Hz AC mains signal. Detailed schematics are provided in the *PL 3120 / PL 3150 / PL 3170 Power Line Smart Transceiver Data Book*.

*Echelon Corporation has developed and patented certain methods of implementing circuitry external to the PL 3120, PL3170 and PL 3150 Power Line Smart Transceiver chips. These patents are licensed pursuant to the Echelon Power Line Smart Transceiver Development Support Kit License Agreement.

PL 3170 Power Line Smart Transceiver Block Diagram



General Specifications

Function	Description
Emissions compliance	Designed to be compliant with FCC, Industry Canada, Japan MPT, and CENELEC EN50065-1 specification for low-voltage signaling
Bit rate	5.4kbps raw bit rate in CENELEC C-band
Communication technique	Dual Frequency BPSK with DSP-enhanced receiver
Carrier frequencies	132kHz (primary) and 115kHz (secondary) in CENELEC C-band
RoHS Compliance	Models 15330R-1000 and 15330R-2500 comply with European Directive 2002/95/EC on Restriction of Hazardous Substances (RoHS) in electrical and electronic equipment.

PL 3170 Power Line Smart Transceiver Pinout Diagram

38 Pin TSSOP

NOTE:

[1] The schematic, bill of materials, and layout plots for the Discrete Interface Circuitry are provided in the PL DSK Power Line Smart Transceiver Development Support Kit.

PL 3170 Power Line Smart Transceiver Pin Descriptions

Pin Name	Type	Pin Functions	PL 3170-E4T10 38 TSSOP Pin No.
XIN	Input	Oscillator connection or external clock input.	29
XOUT	Output	Oscillator connection.	30
$\overline{\text{RESET}}$	Digital I/O (Built-in Pull-up)	Reset pin (active LOW). Note: The maximum external capacitance is 1000pF.	35
$\overline{\text{SERVICE}}$	Digital I/O (Built-in Configurable Pull-up)	Service pin (active LOW).	36
CLKSEL	Digital Input	Tie to V_{DD5}.	34
IO0-IO3	Digital I/O	Large current-sink capacity (20mA). General purpose I/O. The output of timer/counter 1 may be routed to IO0. The output of timer/counter 2 may be routed to IO1.	2, 3, 4, 5
IO4-IO7, IO11	Digital I/O (Built-in Configurable Pull-up)	General purpose I/O. The input of timer/counter 1 may be one of IO4-IO7. The input of timer/counter 2 is IO4.	6, 7, 8, 9, 33
IO8	Digital I/O	General purpose I/O. UART RX. SPI slave clock input. SPI master clock output.	10
IO9	Digital I/O	General purpose I/O. SPI slave data output. SPI master data input.	11
IO10	Digital I/O	General purpose I/O. SPI slave data input. SPI master data output.	126
V_{DD5}	Power	Power input (5V nom). All V_{DD5} pins must be connected together externally.	13, 27, 37
V_{DD5A}	Power	Power input (5V nom). Supplies on-chip analog circuitry.	19
GND	Power	Power input (0V, GND). All GND pins must be connected together externally.	1, 23, 28, 38
ICTMode	Digital Input	In-circuit test mode control. Tie to GND for normal operation.	32
PKD	Digital Output	Packet Detect LED driver.	21
BIU	Digital Output	Band in Use LED driver.	22
RXIN	Analog Input	Receiver input.	15
INTIN,INTOUT	Analog I/O	Integrator input and output.	17, 18
RXC	Analog Input	Receive signal.	16
OOGAS	Analog Input	Comparator to detect when energy storage power supply lacks sufficient energy to transmit a packet. Tie to VCORE if not used.	14
VCORE	Power	Output of internal 1.8V regulator. Requires 0.1µF external capacitor.	20
TXON	Digital Output	High when transmitting. Used to drive LED to show packet transmission.	31
TXDAC	Analog Output	Transmit waveform DAC output.	26
TXSENSE	Analog Input	Transmit amplifier sense feedback.	25
TXBIAS	Analog Output	Transmit amplifier bias generator.	24

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD5}	V_{DD5} Supply Voltage	4.75	5.00	5.25	V
V_{DD5A}	V_{DD5A} Supply Voltage	4.60	5.00	5.25	V
T_A	Ambient Temperature	-40	25	85	ºC
$F_{C\text{-band}}$	XIN Frequency for C-band Operation (10.0000MHz ±200ppm)	9.9980	10.0000	10.0020	MHz

Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Digital Input Low-Level Voltage			0.8	V
V_{IH}	Digital Input High-Level Voltage	2.0			V
V_{OL}	Digital Output Low-Level Voltage				V
	I_{out}<20µA			0.1	
	IO4-IO11, A0-A14, D0-D7, R/$\overline{W}$, $\overline{E}$ (I_{OL} = 1.4mA)			0.4	
	IO0-IO3, $\overline{SERVICE}$, $\overline{RESET}$ (I_{OL}= 20mA)			0.8	
	IO0-IO3, $\overline{SERVICE}$, $\overline{RESET}$ (I_{OL} = 10mA)			0.4	
	PKD, BIU, TXON (I_{OL}= 12mA)			0.5	
V_{OH}	Digital Output High-Level Voltage				V
	$\|I_{out}\|$<20µA	V_{DD5}-0.1			
	IO4-IO11, A0-A14, D0-D7, R/$\overline{W}$, $\overline{E}$ (I_{OH} = -1.4mA)	V_{DD5}-0.5			
	IO0-IO3, $\overline{SERVICE}$, $\overline{RESET}$ (I_{OH} = -1.4mA)	V_{DD5}-0.4			
	PKD, BIU, TXON (I_{OH}= -12mA)	V_{DD5}-0.5			
V_{hys}	Digital Input Hysteresis	175			mV
I_{in}	Input Current (Excluding Pull-ups)[2]	-10		10	µA
I_{pu}	Pull-up Source Current (Vout=0, Output=High-Z)[2]	30		300	µA
I_{DD}	PL 3170 Power Line Smart Transceiver V_{DD5} + V_{DD5A} Supply Current (not including I/O or internal pull-up current)		9	13	mA
V_{LVI}	V_{DD5} LVI Trip Point	4.0		4.45	V

Recommended Operating Conditions for Power Line Smart Transceiver Discrete Interface Circuitry[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ARX}	V_A Supply Voltage - Receive Mode[3]	8.5	12.0	18.0	V
V_{ATX}	V_A Supply Voltage - Transmit Mode[3]	10.8	12.0	18.0	V
T_A	Ambient Temperature	-40	25	85	ºC

Electrical Characteristics of Power Line Smart Transceiver Discrete Interface Circuitry[1] (over recommended operating conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{ARX}	V_A Supply Current - Receive Mode		350	500	µA
I_{ATX}	V_A Supply Current - Transmit Mode		120	250	mA
V_{OTX}	Transmit Output Voltage		7		Vp-p
I_{TXLIM}	Transmit Output Current Limit		1.0		Ap-p
Z_{INRX}	Input Impedance - Receive Mode (with recommended RXCOMP inductor)		500		Ω
Z_{OTX}	Output Impedance - Transmit Mode		0.9		Ω
V_{PMU}	Power Management - Upper V_A Threshold	11.2	12.1	13.0	V
V_{PML}	Power Management - Lower V_A Threshold	7.3	7.9	8.6	V

NOTES:

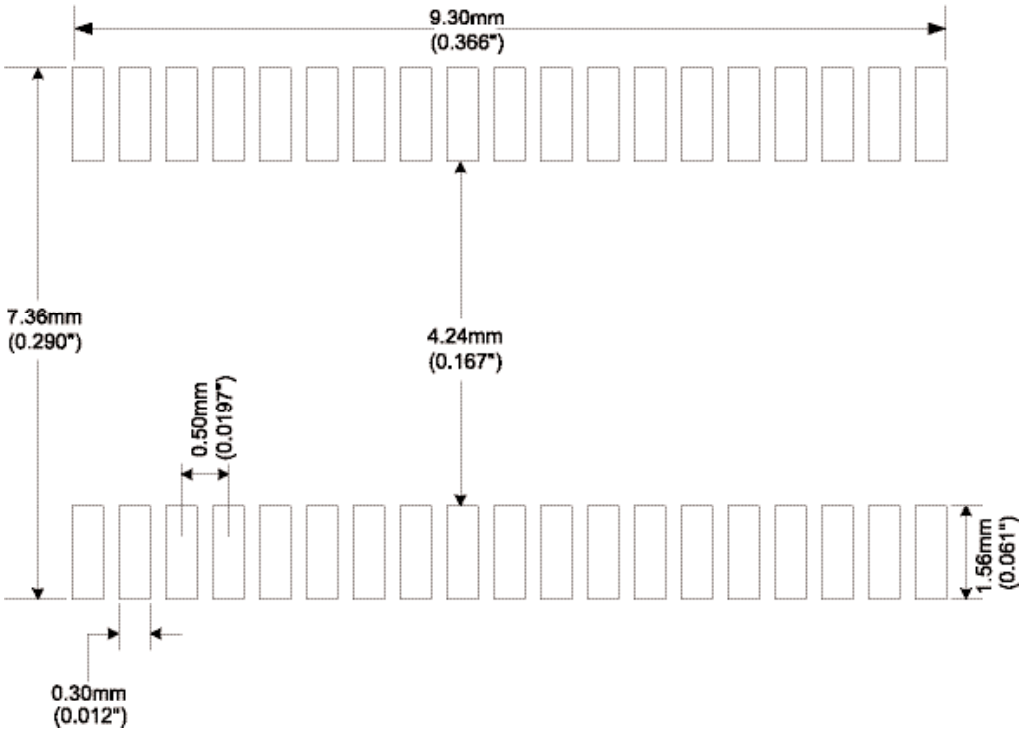
[2] IO4-IO7 and $\overline{SERVICE}$ pins have configurable pull-ups. The $\overline{RESET}$ pin has a permanent pull-up.

[3] Minimum value can be 8.5V under certain conditions (refer to Data Book for details).
Maximum value must also satisfy the following: $V_{ATXAVE} < (150\text{-}T_{AMAX})/(8*D_{MAX})$;
Where: V_{ATXAVE} = Average V_A supply voltage while transmitting
T_{AMAX} = Maximum ambient temperature (ºC)
D_{MAX} = Maximum transmit duty cycle of the device (expressed as decimal number)

Absolute Maximum Ratings[4]

Ambient operating temperature	-40 to 85ºC
Storage temperature	-55 to 125ºC
Voltage on V_{DD5} and V_{DD5A} pins with respect to GND	-0.3 to 6.0V
Voltage on each pin with respect to GND[5]	-0.3 to (V_{DD5} + 0.3V)
Voltage on TXBIAS, TXSENSE, OOGAS pins	-0.3 to 1.89V
Maximum voltage on VCORE pin with respect to GND	1.89V
V_{DD5}, V_{DD5A}, or GND current per pin	±50mA
Input clamp current, I_{IK}[5] (V_I<0 or V_I>V_{DD5})	±10mA
Output clamp current, I_{OK}[5] (V_I<0 or V_I>V_{DD5})	±10mA
Output current per pin[5]	±25mA
Power dissipation	250mW
Reflow soldering temperature profile	Refer to Joint Industry Standard document *IPC/JEDEC J-STD-020C* (July 2004)
Reflow soldering temperature	260ºC (Models 15330R-1000 and 15330R-2500)

Recommended Pad Layout for PL 3170-E4T10 Power Line Smart Transceiver (38 TSSOP)

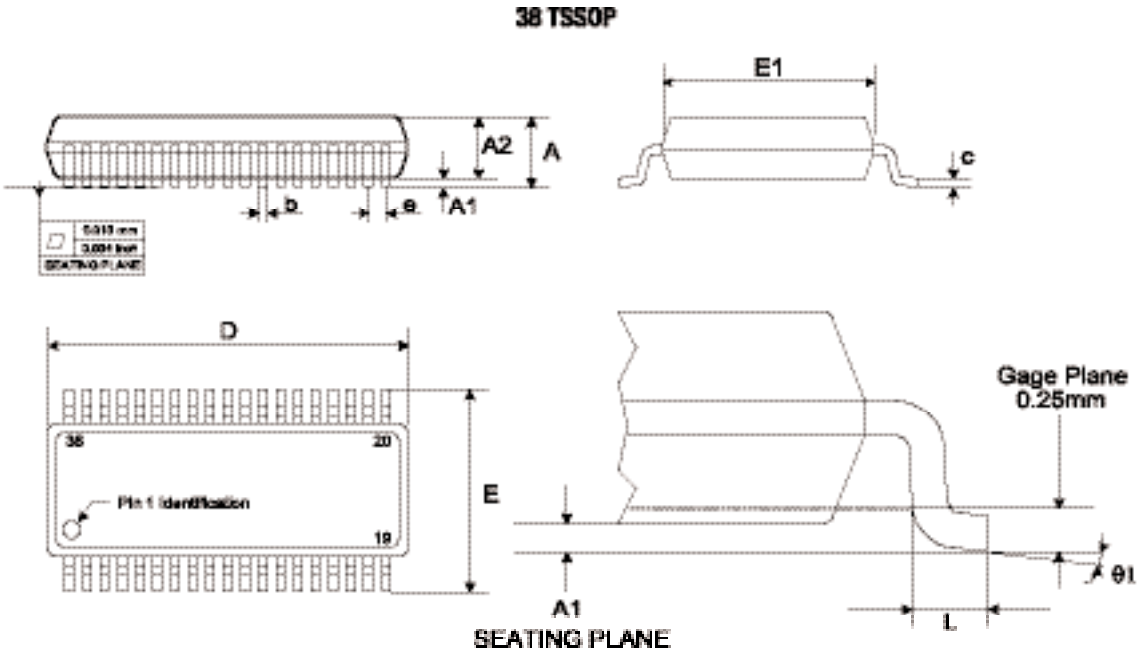


NOTES:

[4] Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation under these conditions is not implied.

[5] Applies to all pins except V_{DD5}, V_{DD5A}, VCORE, TXBIAS, TXSENSE, and OOGAS.

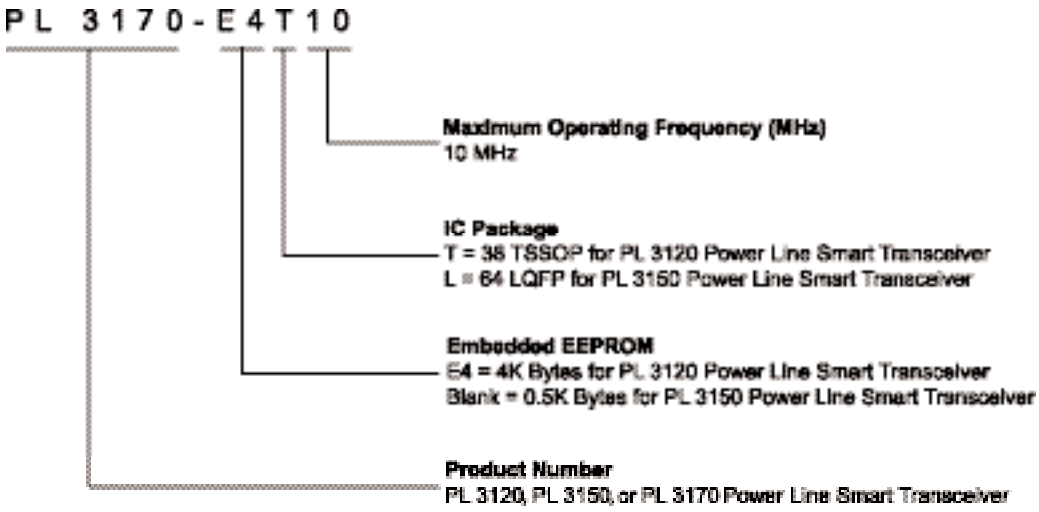
PL 3170-E4T10 Power Line Smart Transceiver Package Diagram



Symbol	mm (prevailing dimensions)			inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.17	-	0.27	0.0067	-	0.011
c	0.09	-	0.20	0.0035	-	0.0079
D	9.60	9.70	9.80	0.378	0.381	0.385
E	6.40 BSC			0.252 BSC		
e	0.50 BSC			0.0197 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
L	0.45	0.60	0.75	0.0177	0.023	0.030
θ1	0°	-	8°	0º	-	8º

Ordering Information

Power Line Smart Transceiver IC Product Number	Model Number	RoHS Compliant	Packaging Type	EEPROM	RAM	ROM	External Memory Interface	IC Package	PL DSK Development Support Kit Model Number
PL 3170-E4T10	15330R-1000	Yes	Tubes	4K Bytes	2K Bytes	24K Bytes	No	38 TSSOP	17050R-21-27
PL 3170-E4T10	15330R-2500	Yes	Tape & Reel	4K Bytes	2K Bytes	24K Bytes	No	38 TSSOP	17050R-21-27



Documentation

The *PL 3120 / PL 3150 /PL 3170 Power Line Smart Transceiver Data Book* may be downloaded from Echelon's web site or ordered through Echelon's literature fulfillment department.

Document	Echelon Part Number
PL 3120 / PL 3150 / PL 3170 Power Line Smart Transceiver Data Book	005-0154-01

003-0431-01-A