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BQ2960XY/BQ2961XY Overvoltage Protection for 2-Series, 3-Series, and 4-Series Cell Li-Ion Batteries with Regulated Output Supply

1 Features

- 2-, 3-, and 4-Series Cell Overvoltage Protection (OVP)
- Fixed Delay Timer to Trigger FET Drive Output (3-s, 4-s, 5.5-s or 6.5-s Options)
- Factory Programmed OVP Threshold (Threshold Range 3.85 V to 4.6 V)
- Output Options: Active High
- High-Accuracy Overvoltage Protection: ±10 mV
- Regulated Supply Output (3.3-V, 2.5-V, 1.8-V Options) with self-disable and/or external enable/disable control
- Low Power Consumption I_{CC} ≈ 4 µA ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- Extra Low Power Consumption with REG output disabled, I_{CC} ~ 1.2 µA
- Low Leakage Current Per Cell Input < 100 nA
- Small Package Footprint
  - 8-Pin WSON (2 mm x 2 mm)

2 Applications

- Notebook PC
- Ultrabooks
- Medical
- UPS Battery Backup

3 Description

The bq296xyz family is a high accuracy, low power overvoltage protector with a 1-mA regulated output supply for Li-Ion battery pack applications.

Each cell in a 2-series to 4-series cell stack is individually monitored for an overvoltage condition. An internally fixed-delay timer is initiated upon detection of an overvoltage condition on any cell; upon expiration of the delay timer, an output pin is triggered into an active state to indicate that an overvoltage condition has occurred.

The regulated output supply delivers up to 1-mA (max) output current to drive always-on circuits, such as a real-time clock (RTC) oscillator. The bq296xyz family has a self-disable function to turn off the regulated output if any cell voltage falls below a certain threshold, thereby preventing drain on the battery, and provides an external control to enable or disable the regulated output.

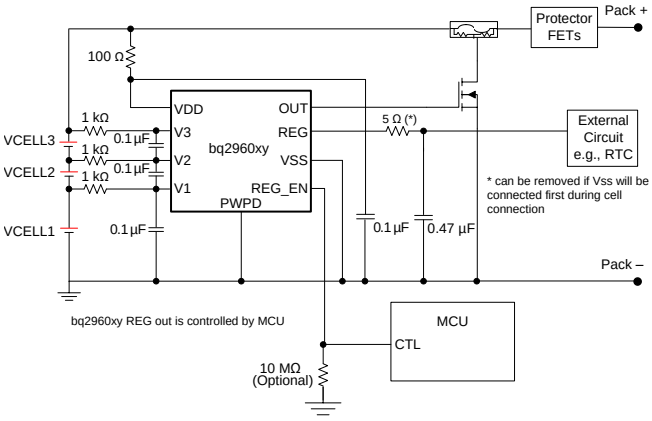
Device Information(1)(2)

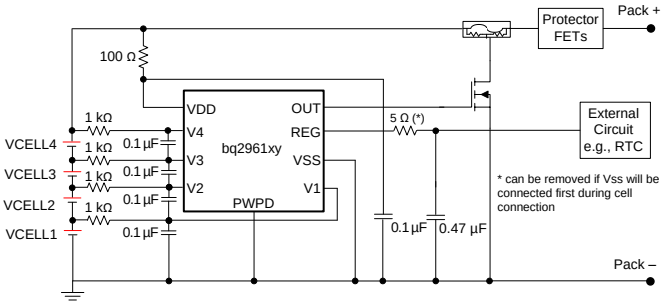
PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq2960xy	WSON (8)	2.00 mm × 2.00 mm
bq2961xy		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) The bq2960xy is a 2- to 3-S device and bq2961xy is a 2- to 4-S device.

4 Simplified Schematic





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5 Revision History

Changes from Original (May 2015) to Revision A **Page**

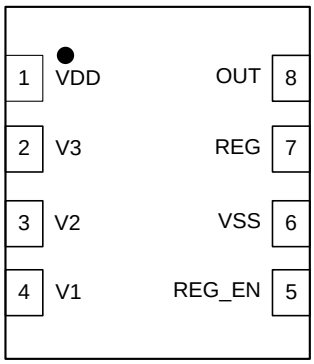
- Changed the device listing in the data sheet header information to: bq2961 ... 1
- Changed bq296106, '107, '111 From: Preview To: Released status ... 3
- Added bq296112 to *Device Comparison Table* ... 3
- Added bq296113 to *Device Comparison Table* ... 3
- Added Available the bq2961xy configuration range to *Device Comparison Table* ... 3

6 Device Comparison Table

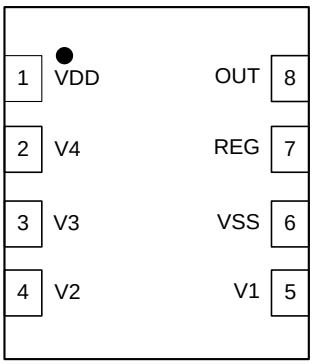
PART NUMBER	STATUS	OVP (V)	OVP DELAY (s)	UV (V)	LDO (V)
bq296100	Preview	4.35	6.5	2.5	3.3
bq296101	Preview	4.40	6.5	2.5	3.3
bq296102	Preview	4.45	6.5	2.5	3.3
bq296103	Released	4.50	6.5	2.5	3.3
bq296104	Preview	4.35	6.5	2.8	3.3
bq296105	Preview	4.40	6.5	2.8	3.3
bq296106	Released	4.45	6.5	2.8	3.3
bq296107	Released	4.50	6.5	2.8	3.3
bq296108	Preview	4.50	6.5	2.4	3.3
bq296109	Preview	4.325	3.0	2.5	3.3
bq296110	Preview	4.45	3.0	2.5	3.3
bq296111	Released	4.45	4.0	2.5	3.3
bq296112	Released	4.50	3.0	2.5	3.3
bq296113	Released	4.35	3.0	2.5	3.3
bq2961xy	Future Option, contact TI	3.85V - 4.60V in 50mV step	3.0, 4.0, 5.5, 6.5	2.0V - 2.8V in 50mV step	1.8, 2.5, 3.3

7 Pin Configuration and Functions

2s-to-3s bq2960xy
(Top View)



2s-to-4s bq2961xy
(Top View)



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	BQ2960XY	BQ2961XY		
OUT	8	8	OA	Analog Output drive for overvoltage fault signal, CMOS Output High or Open Drain Active Low.
PWPD	9	9	P	TI recommends connecting the exposed pad to VSS on PCB.
REG	7	7	OA	Regulated Supply Output. Requires an external ceramic capacitor for stability.
REG_EN	5	—	IA	Regulated Supply Output Enable. A "high" to enable REG output and "low" to disable REG output.
V1	4	5	IA	Sense input for positive voltage of the lowest cell from the bottom of the stack.
V2	3	4	IA	Sense input for positive voltage of the second cell from the bottom of the stack.
V3	2	3	IA	Sense input for positive voltage of the third cell from the bottom of the stack.
V4	—	2	IA	Sense input for positive voltage of the fourth cell from the bottom of the stack.
VDD	1	1	P	Power supply input
VSS	6	6	P	Electrically connected to integrated circuit ground and negative terminal of the lowest cell in the stack.

(1) IA = Analog input, OA = Analog Output, P = Power connection

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD – VSS	–0.3	30	V
Input voltage range	V4 – V3, V3 – V2, V2 – V1, V1 – VSS	–0.3	30	
	REG – VSS	–0.3	3.6	
	REG_EN – VSS	–0.3	28	
Output voltage range	OUT – VSS	–0.3	30	
Continuous total power dissipation, P_{TOT}		See *Thermal Information*.		
Lead temperature (soldering, 10 s), T_{SOLDER}		300	300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (1)	Supply voltage, V_{DD} (1), bq2960xy	3		15	V
	Supply voltage, V_{DD} (1), bq2961xy	3		20	
	Supply voltage, V_{DD} with REG output on	4			
Input voltage range	V_n - V_{n-1} , V1 – VSS	0		5	V
	REG_EN	0		15	V
Operating ambient temperature range, T_A		–40		110	°C

(1) See *Typical Application*.

8.4 Thermal Information

THERMAL METRIC(1)		bq2960xy DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	10	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

8.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to 110°C, and V_{DD} = 3 V to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Protection Thresholds						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	R_{IN} = 1 kΩ	Applicable Voltage: 3.85 V to 4.6 V in 50 mV steps			V
V_{HYS}	OV Detection Hysteresis		250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		40	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV
		T_A = 110°C	–54		54	mV
Supply and Leakage Current						
I_{DD}	Supply Current	$(V_n – V_{n-1})$ = 3.8 V and $(V1 – V_{SS}) > V_{UVREG}$, VDD = top V_n voltage, I_{REG} = 0 mA, T_A = 0°C to 60°C		4	6	µA
		$(V_n – V_{n-1})$ = 3.8 V and $(V1 – V_{SS}) > V_{UVREG}$, VDD = top V_n voltage, I_{REG} = 0 mA, T_A = –40°C to 110°C			8	µA
		$(V_n – V_{n-1})$ = 3.8 V and $(V1 – V_{SS}) < V_{UVREG}$, VDD = top V_n voltage, T_A = 0°C to 60°C		1	2	µA
		$(V_n – V_{n-1})$ = 3.8 V and $(V1 – V_{SS}) < V_{UVREG}$, VDD = top V_n voltage, T_A = –40°C to 110°C			4	µA
I_{IN}	Input Current at V_x Pins	$(V_n – V_{n-1}) = (V1 – V_{SS})$ = 3.8 V, VDD = top V_n voltage, T_A = 25°C	–0.1		0.1	µA
Output Drive OUT, CMOS Active High						
V_{OUT}	Output Drive Voltage, Active High	$(V_n – V_{n-1})$ or $(V1 – V_{SS}) > V_{OV}$, I_{OH} = 100 µA, VDD = top V_n voltage	6			V
		If three of four cells are short circuited, only one cell remains powered and > V_{OV}, VDD = V_n (the remaining cell voltage), I_{OH} = 100 µA		VDD – 0.3		V
		$(V_n – V_{n-1})$ and $(V1 – V_{SS}) < V_{OV}$, VDD = sum of the cell stack voltage, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH}	OUT Source Current (during OV)	$(V_n – V_{n-1})$, (V3 – V2), or $(V1 – V_{SS}) > V_{OV}$, VDD = top V_n voltage, forced OUT = 0 V, measured out of OUT pin			4.5	mA
I_{OUTL}	OUT Sink Current (no OV)	$(V_n – V_{n-1})$ and $(V1 – V_{SS}) < V_{OV}$, VDD = top V_n voltage, forced OUT = VDD, measured into OUT pin. Pull-up resistor R_{PU} = 5 kΩ to VDD	0.5		14	mA
Internal Fixed Delay Timer						
t_{DELAY}	OV Delay Time(1)	Internal Fixed Delay, 3 second delay option	2.4	3	3.6	s
		Internal Fixed Delay, 4 second delay option	3.2	4	4.8	s
		Internal Fixed Delay, 5.5 second delay option	4.4	5.5	6.6	s
		Internal Fixed Delay, 6.5 second delay option	5.2	6.5	7.8	s
t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode OV Delay Time	Internal Fixed delay		15		ms

(1) Specified by design. Not 100% tested in production.

Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to 110°C, and V_{DD} = 3 V to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulated Supply Output, REG						
V_{REG}	REG Supply	VDD ≥ 4 V, I_{REG} = 0 µA to 1 mA, C_{REG} = 0.47 µF where V_{REG} = 3.3 V	3.2	3.3	3.4	V
		VDD ≥ 4 V, I_{REG} = 0 µA to 1 mA, C_{REG} = 0.47 µF where V_{REG} = 2.5 V	2.425	2.5	2.575	V
		VDD ≥ 4 V, I_{REG} = 0 µA to 1 mA, C_{REG} = 0.47 µF where V_{REG} = 1.8 V	1.746	1.8	1.854	V
I_{REG}	REG Current Output	VDD ≥ 4 V, C_{REG} = 0.47 µF	0		1	mA
$I_{REG\_SC\_Limit}$	REG Output Short Circuit Current Limit	REG = V_{SS}, C_{REG} = 0.47 µF	4			mA
R_{REG_PD}	REG pull-down resistor	REG is disabled	20	30	45	kΩ
Regulated Supply Output Enable, REG_EN						
V_{IH}	High-level Input		1.6			V
V_{IL}	Low-level Input				0.4	V
I_{LKG}	Input Leakage Current	V_{IH} < 6 V			0.1	µA
Regulated Supply Undervoltage Self-disable						
V_{UVREG}	Undervoltage detection	Factory Configuration: 2.0 V to 2.8 V in 50 mV steps, T_A = 25 °C	–50		50	mV
V_{UVHYS}	Undervoltage Detection Hysteresis		250	300	400	mV
$t_{UVDELAY}$	Undervoltage Detection Delay		4.5	6	7.5	s
V_{UVQUAL}	Cell voltage to qualify for UV detection			0.5		V

8.6 Typical Characteristics

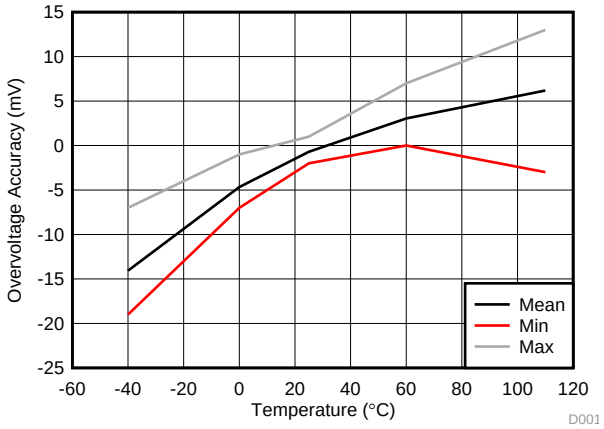


Figure 1. Overvoltage Threshold (V_{OV}) vs Temperature

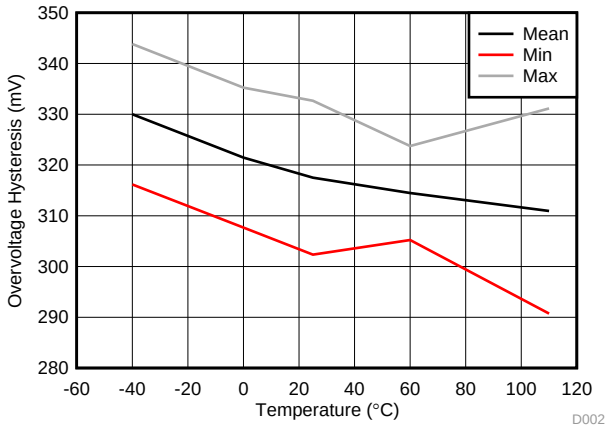


Figure 2. Hysteresis V_{HYS} vs Temperature

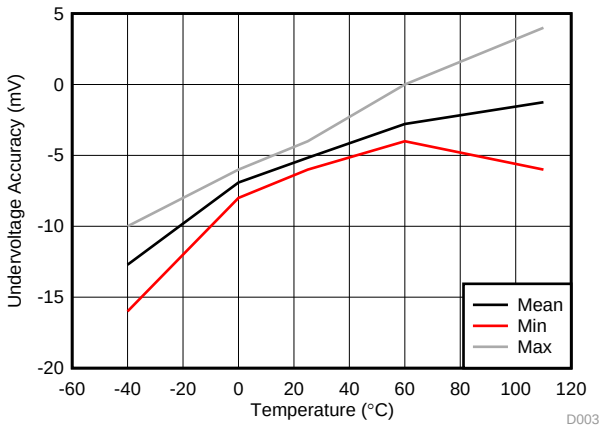


Figure 3. Undervoltage Accuracy

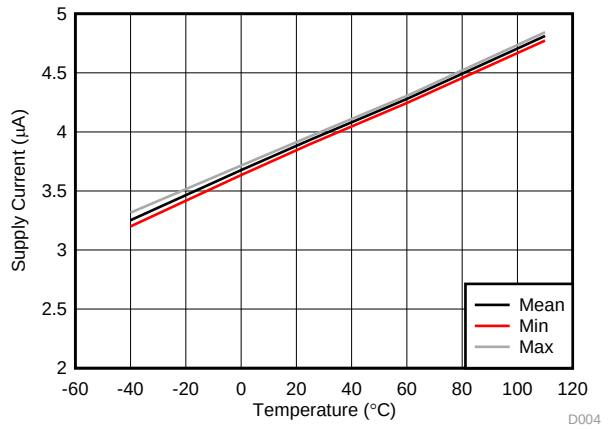


Figure 4. I_{DD} with Regulator On

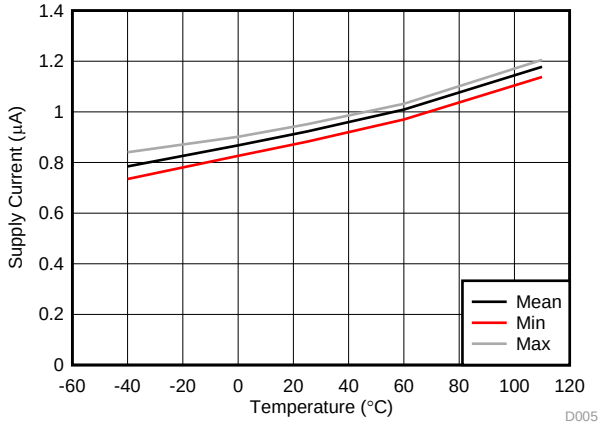


Figure 5. I_{DD} with Regulator Off

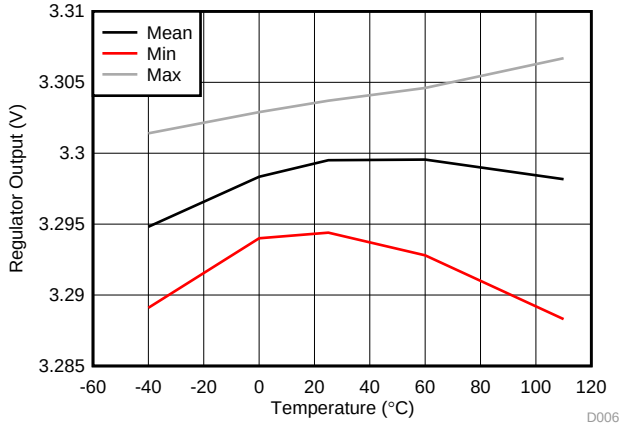


Figure 6. Regulator Output Without Load

Typical Characteristics (continued)

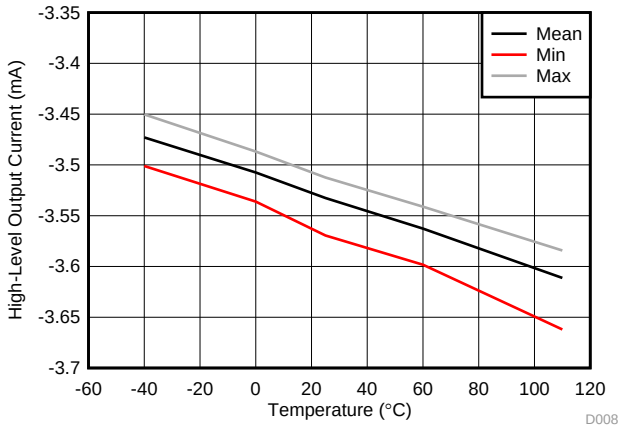


Figure 7. I_{OUTH} vs Temperature

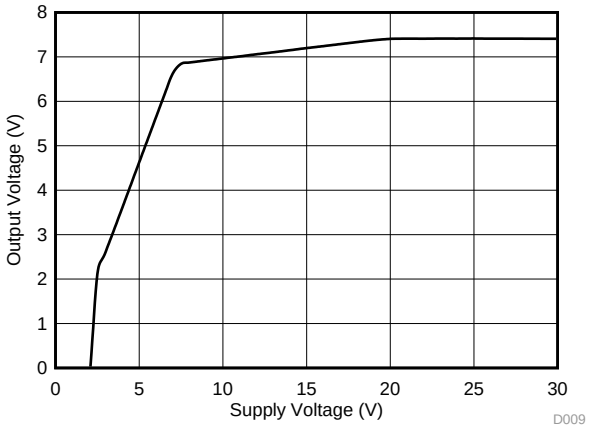


Figure 8. V_{OUT} vs V_{DD}

9 Detailed Description

9.1 Overview

The bq2960xy and bq2961xy are second-level overvoltage (OV) protectors with a regulated output. Each cell is monitored independently by comparing the actual cell voltage to an overvoltage threshold V_{OV}. The overvoltage threshold is preprogrammed at the factory with a range between 3.85 V to 4.65 V.

The regulated output is enabled unless any of the cell voltages fall below the V_{UVREG} threshold. This threshold is preprogrammed at the factory with a range between 2 V to 2.8 V. For bq2960xy family, an external control pin, REG_EN, is available to enable or disable the regulated output in addition to the V_{UVREG} detection.

Table 1. Programmable Parameters

OVERVOLTAGE RANGE (V)	OVERVOLTAGE DELAY (s)	UNDERVOLTAGE RANGE (V)	REGULATOR (V)
3.85 to 4.6 in 50 mV step	3, 4, 5.5, 6.5	2.0 to 2.8 in 50 mV step	1.8, 2.5, 3.3

9.2 Functional Block Diagram

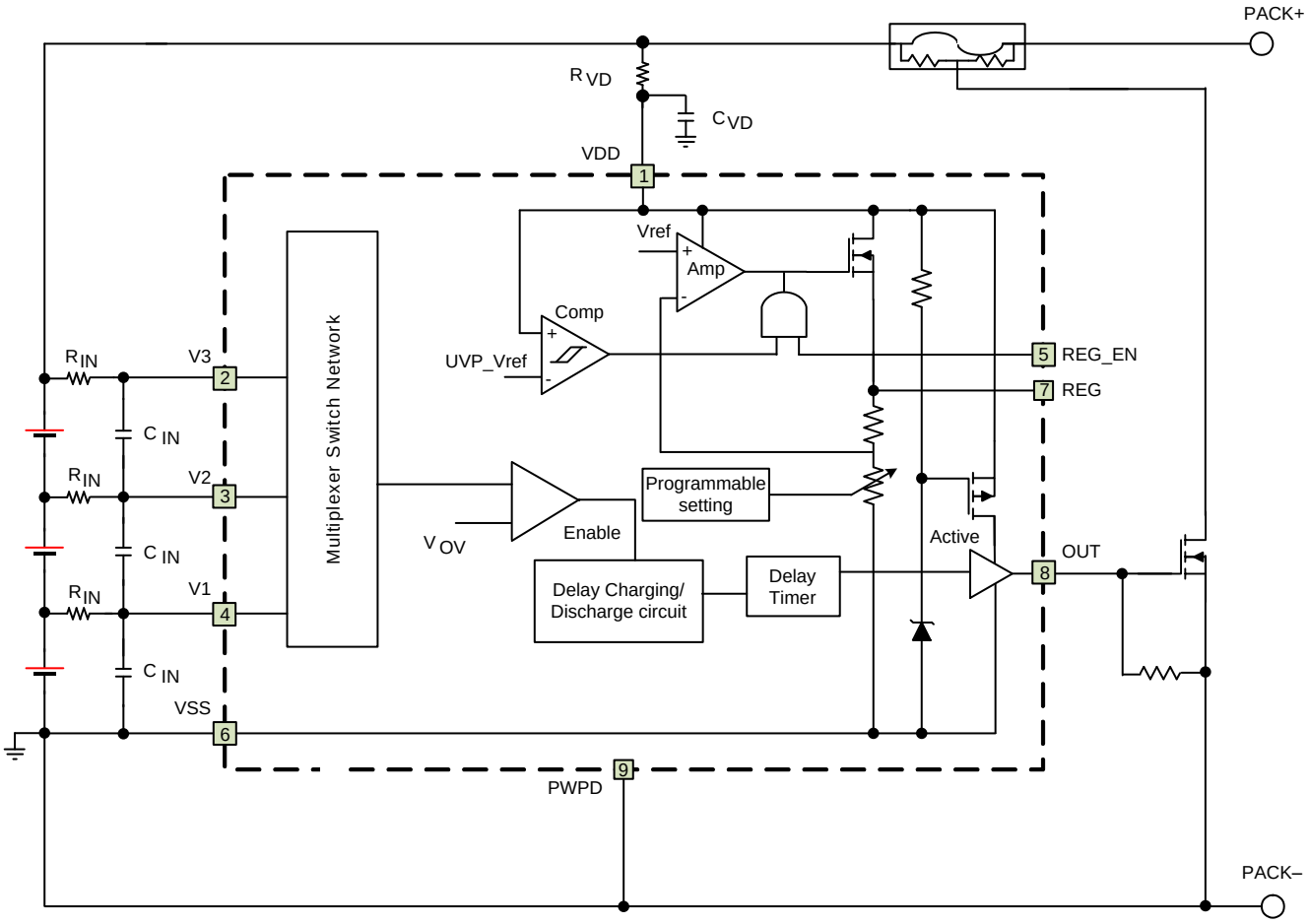


Figure 9. bq2960xy Block Diagram

Functional Block Diagram (continued)

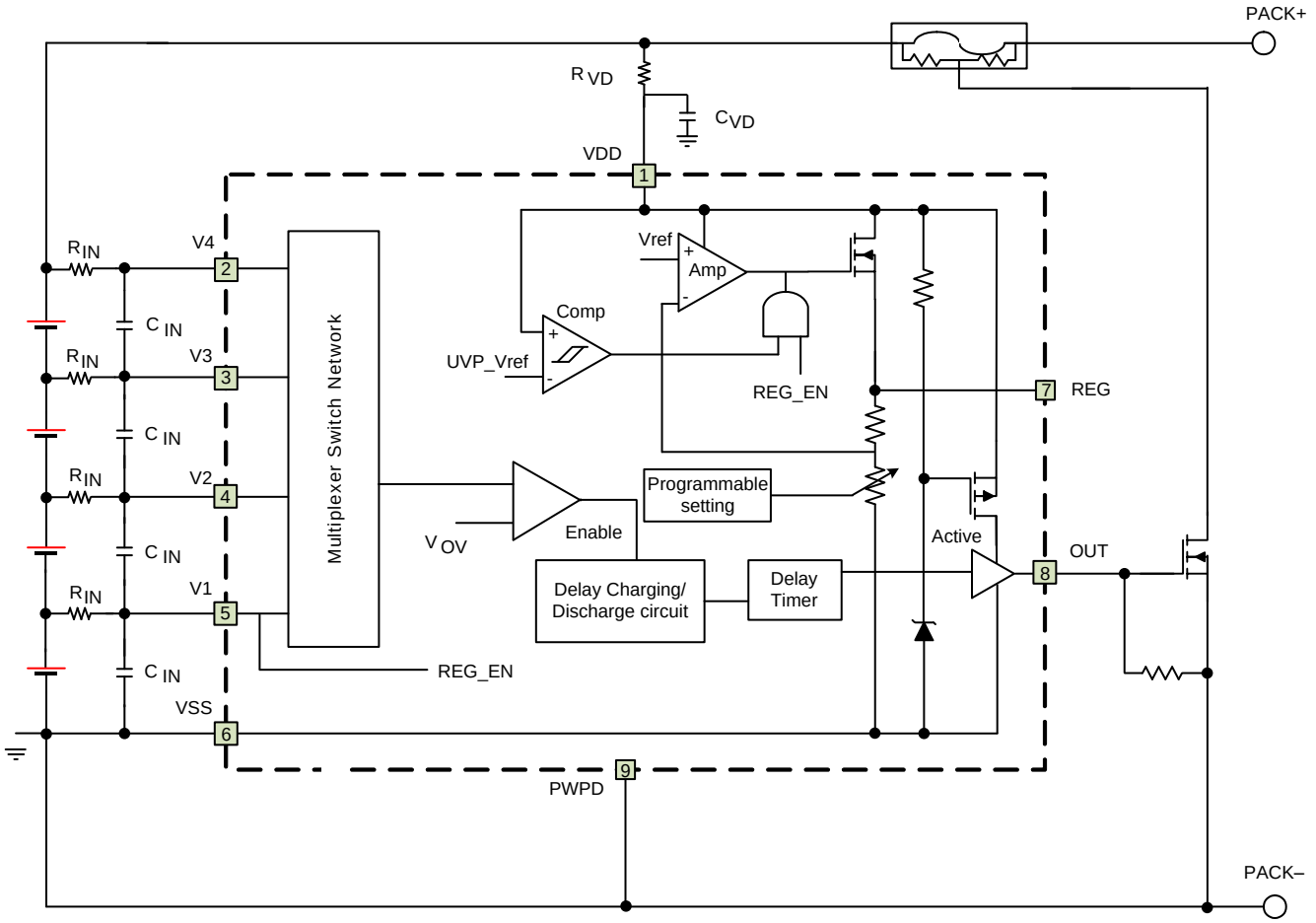


Figure 10. bq2961xy Block Diagram

9.3 Feature Description

9.3.1 Pin Details

9.3.1.1 Input Sense Voltage, Vx

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

9.3.1.2 Output Drive, OUT

This terminal serves as the fault signal output in Active High.

9.3.1.3 Supply Input, VDD

This terminal is the unregulated input power source for the device. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

9.3.1.4 Regulated Supply Output, REG

This terminal is connected to an external capacitor and provides a regulated supply to power a circuit such as a Real Time Clock integrated circuit, or functions requiring a well-regulated supply. Maximum current load on this pin cannot exceed 1 mA.

Feature Description (continued)

The REG output has protection for overcurrent, using a current limit protection circuit, and also detects and protects for excessive power dissipation due to short circuit of the external load. This pin requires a ceramic 1-µF capacitor connection to VSS for improved stability, noise immunity, and ESD performance of the supply output. This capacitor must be placed close to the REG and VSS pins for connection.

9.3.1.5 Regulated Supply Output Enable, REG_EN (bq2960xy Only)

This terminal is a high voltage input drain to enable and disable the regulated supply output, REG terminal. When the VREG_EN > V_{IH}, the REG terminal output is enabled including the cell undervoltage detection function to self-disable the regulated supply. When the VREG_EN < V_{IL}, the REG terminal output, the cell undervoltage detection and the regulated supply self-disable functions are disabled.

To keep the REG output enabled at all times, the recommendation is to connect the REG_EN to the V1 termination. There is a 6-V clamp to protect the REG_EN terminal from a high voltage input. By connecting REG_EN to V1, the clamp circuit is not active.

When the REG output is enabled, VREG_EN > V_{IH}, the REG output can be self-disabled if any of the cell voltages are < V_{UVREG}. The self-disable function is used to reduce power consumption when the battery pack is deeply depleted.

9.3.2 Overvoltage Sensing for OUT

In the bq296xxx device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, an internal timer circuit is activated. This timer circuit causes a factory pre-programmed fixed delay before the OUT terminal goes from inactive to active state.

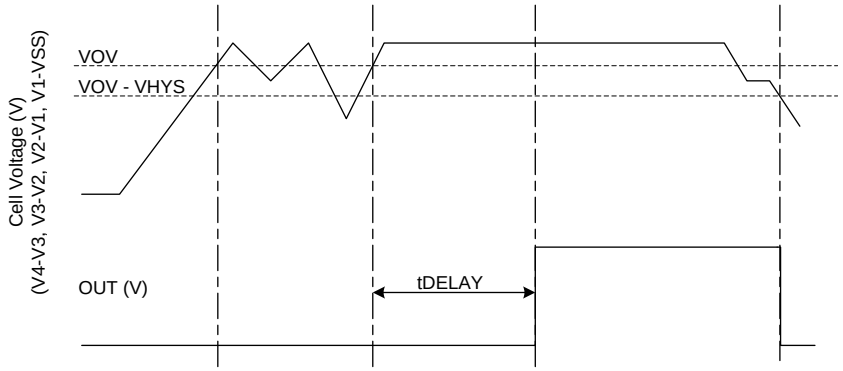


Figure 11. Timing for Overvoltage Sensing for OUT

9.3.3 Regulated Output Voltage and REG_EN Pin

There are three factory-preprogrammed options for the regulated output voltage, 3.3 V, 2.5 V, and 1.8 V. At power up, the regulated output is on by default. If any cell voltage is below V_{UVREG} at device power up, the regulated output will remain on until the t_{UV_DELAY} time has passed, the regulated out turns off after the delay time.

During discharge, if any cell voltage falls below the V_{UVREG} threshold for t_{UV_DELAY} time, the regulated output is self-disabled. The regulated output turns on again when all the cell voltages are above V_{UVREG} + V_{UVHYS}.

Feature Description (continued)

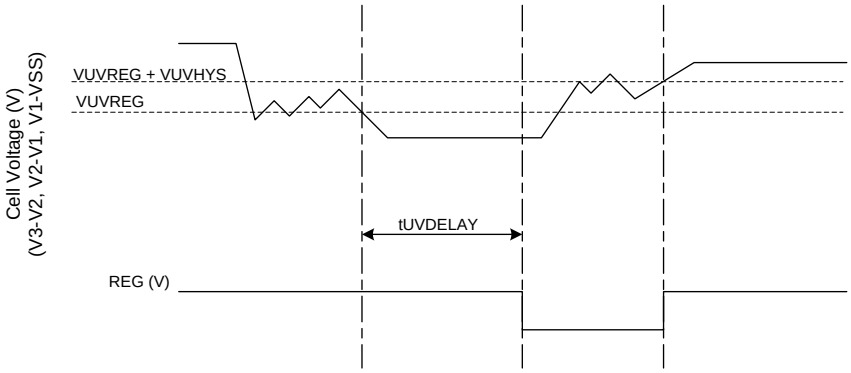


Figure 12. REG Output Timing

For bq2960xy family, an external REG_EN pin is available to enable and disable the regulated output function. To enable both the regulated output and the undervoltage self-disable features, the REG_EN pin must be above V_{IH}. A microcontroller can be used to control the REG_EN pin. Alternatively, connecting the REG_EN pin to the bottom cell is another option to enable the regulated output function always.

Feature Description (continued)

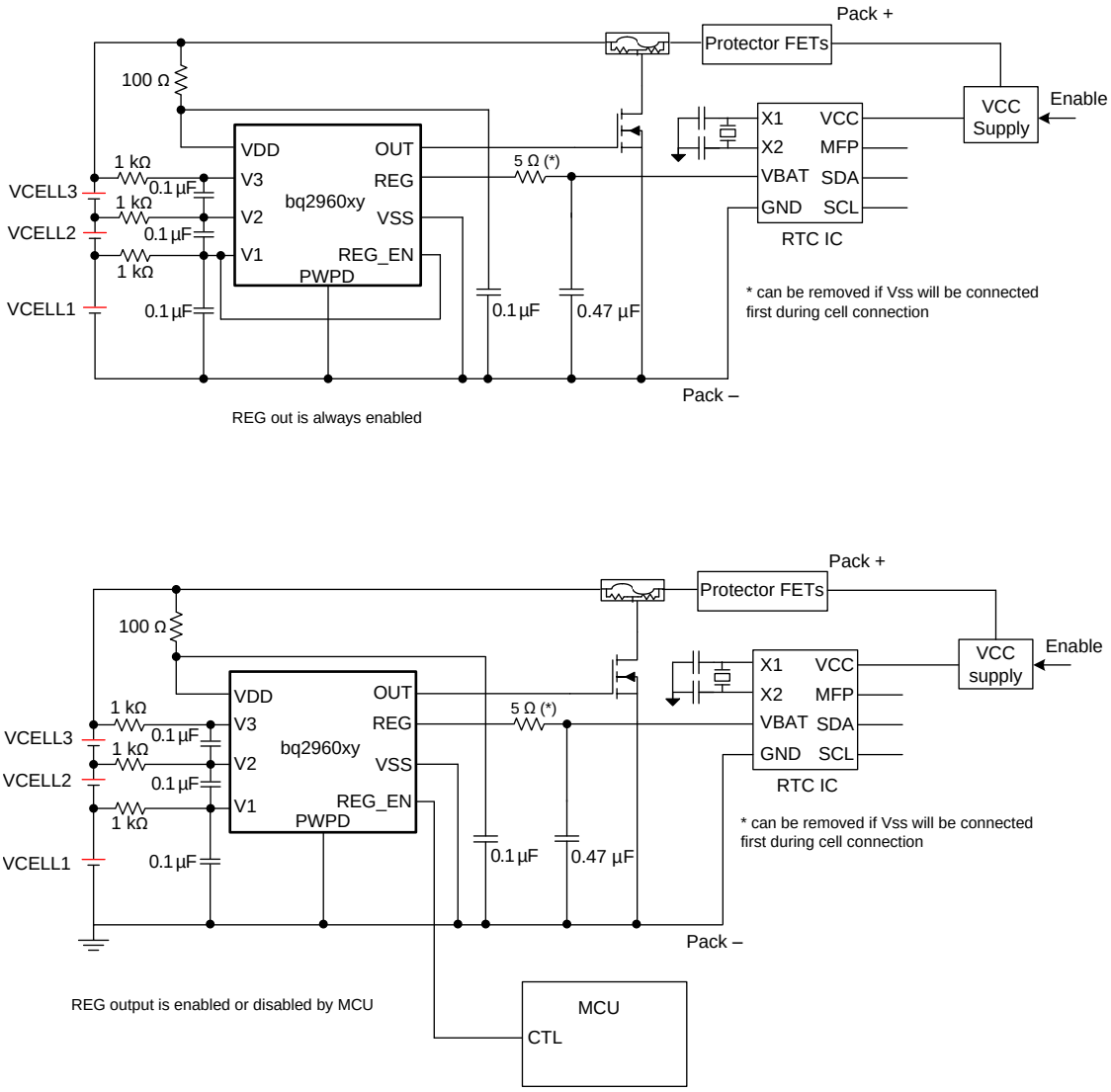


Figure 13. bq2960xy Application Schematic

9.4 Device Functional Modes

9.4.1 NORMAL Mode

When all of the cell voltages are below the V_{OV} threshold AND above V_{UVREG} threshold, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1), (V3–V2), and (V4–V3). The OUT pin is inactive in this mode. The regulated output is always enabled for bq2961xy. For bq2960xy, the regulated output is on only if the voltage on the REG_EN pin is above V_{IH}.

9.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceed the overvoltage threshold, V_{OV}, for configured OV delay time. The OUT pin is activated after a delay time preprogrammed at the factory. The OUT pin will pull high internally. Then an external FET is turned on, shorting the fuse to ground, which allows the battery and/or charger power to blow the fuse. When all of the cell voltages fall below (V_{OV} – V_{HYS}), the device returns to NORMAL mode. The regulated output (if enabled) remains on in this mode.

Device Functional Modes (continued)

9.4.3 UNDERVOLTAGE Mode

The UNDERVOLTAGE mode is detected if any of the cell voltage across (V1–VSS), (V2–V1), (V3–V2), or (V4–V3) is below the V_{UVREG} threshold for t_{UV_DELAY} time. In this mode, the regulated output is disabled. To return to the NORMAL mode, all the cell voltages must be above (V_{UVREG} + V_{UVHYS}).

For a low cell configuration, V_n pin may be shorted to the ($V_{n\ -\ 1}$) pin. The device ignores any differential cell voltage below V_{UVQUAL} threshold for undervoltage detection.

9.4.4 CUSTOMER TEST MODE

The Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay-timer parameter once the circuit is implemented into the battery pack. To enter CTM, the VDD pin should be set at least 10 V higher than V3 (see Figure 14). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to VC3 voltage differential of 10 V, so that the decrease in the value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the device into CTM. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1) and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 14 shows the timing for the Customer Test Mode.

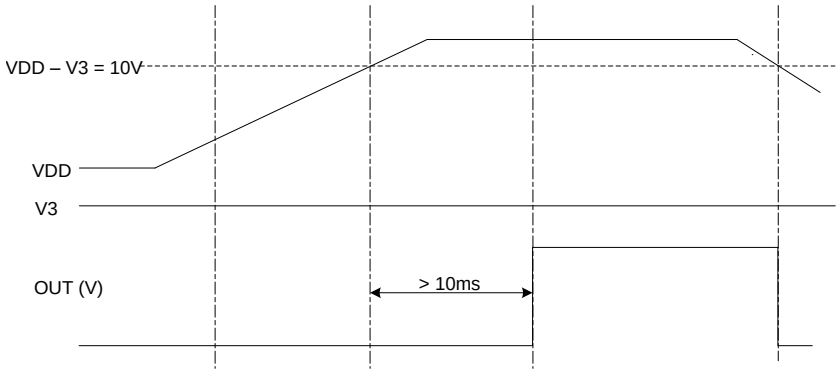


Figure 14. Timing for Customer Test Mode

Figure 15 shows the measurement for current consumption of the product for both VDD and Vx.

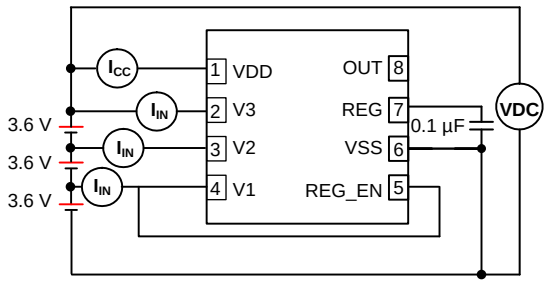


Figure 15. Configuration for Integrated Circuit Current Consumption Test

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The bq2960xy and bq2961xy devices are a family of second-level protectors used for overvoltage protection of the battery pack in the application. A regulated output is available to drive a small circuit with maximum I_{REG} loading. The device OUT pin is active high, which drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery and/or charger power to blow the fuse and cut the power path.

10.2 Typical Application

Figure 13 shows the recommended reference design components.

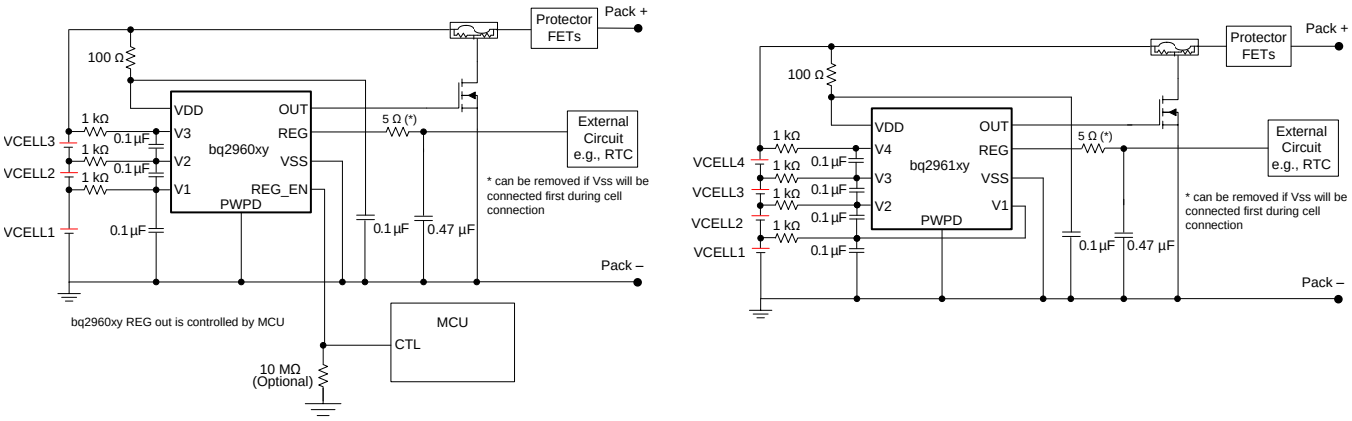


Figure 16. Application Schematic

10.2.1 Design Requirements

NOTE

Changes to the ranges stated in Table 2 will impact the accuracy of the cell measurements.

Table 2. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	4700	Ω
Voltage monitor filter capacitance	C_{IN}	0.01	0.1	1.0	µF
Supply voltage filter resistance	R_{VD}	0.1	—	1	KΩ
Supply voltage filter capacitance	C_{VD}	—	0.1	1.0	µF
REG output capacitance	C_{REG}	0.47	1	—	µF

NOTE

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than the recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

10.2.2 Detailed Design Procedure

NOTE

The device VSS must be connected first during PCB test or cell attachment. Failure to do so can damage the REG pin.

1. If VSS pin cannot be connected first, it is required to add a resistor of a minimum of 5 ohms to a maximum of 10 ohms (a 5-ohm resistor is used in the reference schematic, Figure 17) in series with the REG capacitor. When VSS is floating, the REG capacitor always charges up to the VDD voltage. When VSS is finally connected, the REG capacitor will be discharged. Adding a small resistor in series reduces the current strength and avoids any potential damage to the REG pin. The 5-ohm resistor can be placed in series with the REG connect circuit (as shown in Figure 17) or in series of the REG capacitor (as shown in Figure 18). Placing the resistor in series with the REG circuit results in a small drop of VREG (for example: max loading of 1 mA with a 5-ohm resistor will drop 5 mV on VREG), but such a connection can protect again rush current discharge from both REG capacitor or external filter capacitor connected to the REG pin. Placing the resistor in series with the REG capacitor is an alternative to avoid additional drop in VREG if the filer capacitor used by the external circuit is much smaller than the REG capacitor.
2. After VSS is connected, the device allows random cell connect to the Vx pin.
3. Cell should be connected to the lower V_n pin; the unused V_n pin should be shorted to the (V_{n-1}) pin. See Figure 17 for details.

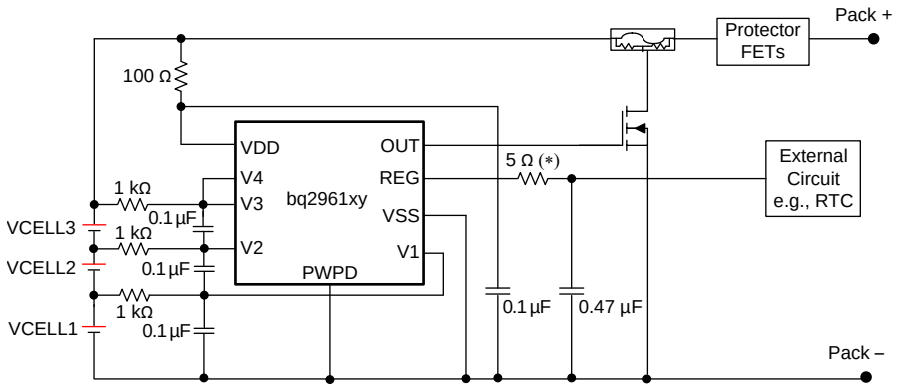
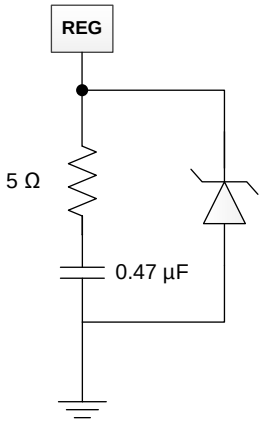


Figure 17. 3-Series bq2961xy Schematic

4. A zener diode can be added to the REG pin to VSS as shown in Figure 18. This is recommended to protect the circuit connected to the REG pin if floating VSS in the field is a risk concern. When VSS is floating (during cell connection when VSS is not connected first or in system fault with BAT– wire broken), the REG voltage always pulls up to VDD. In a 4-S configuration, the REG voltage can reach approximately 16 V with VSS floating. Adding a zener diode clamps the REG voltage to a safe level for the external circuits connected to the REG pin. Having the zener diode can also protect the external circuits if REG pin is shorted to OUT pin or any other high-voltage output terminal. If a zener diode is used, it is recommended to put the diode on the battery side with the bq296xxx device to allow protection on both the REG pin as well as the circuit connected to REG under floating VSS condition. The resistor in series with the REG pin is not required in this case.

The 5-Ω resistor limits the rush current discharge from the capacitor during cell connection when Vss is not connected first.

This resistor is not required if Vss is connected first in the cell connection sequence.



Loss of Vss connection or REG shorted to high voltage can bring the REG above the regulated range. This optional zener clamp can protect the downstream circuit under such an event.

Figure 18. 5-V Zener Diode

5. For 2- to 3-series applications, if an external control for the regulated output is required, select the bq2960xy family. Otherwise, select the bq2961xy family.

10.2.3 Application Curves

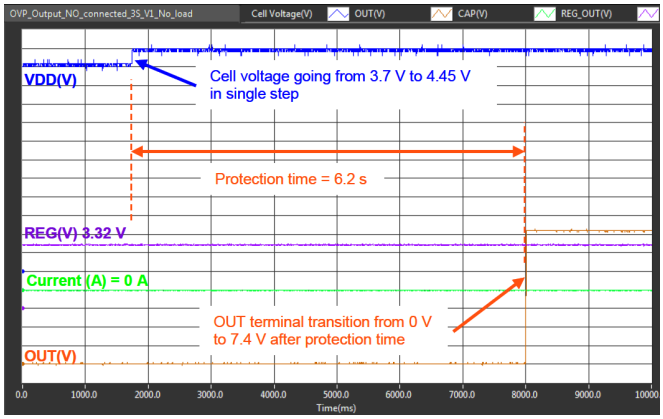


Figure 19. Overvoltage Protection

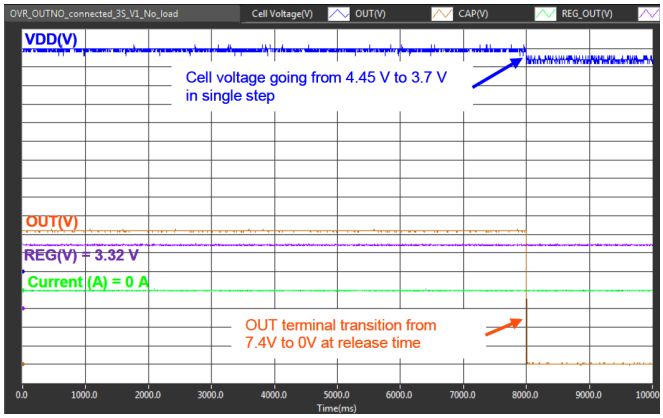


Figure 20. Overvoltage Protection Release

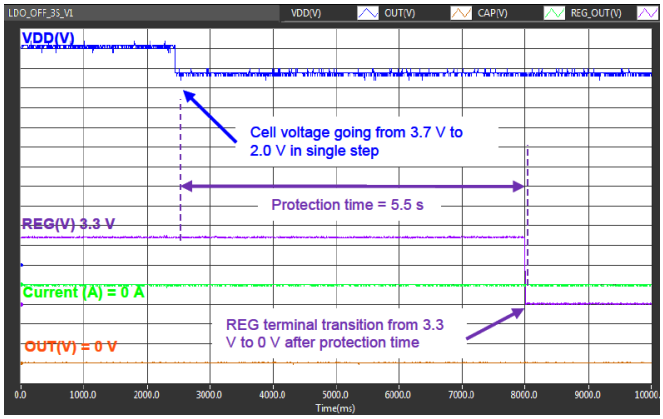


Figure 21. Undervoltage Detection to Turn off Regulator

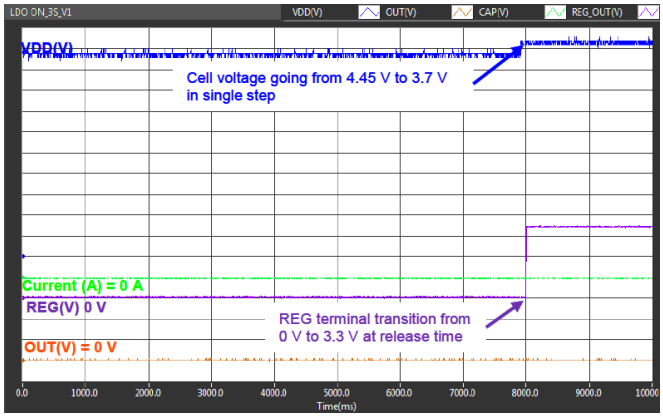


Figure 22. Undervoltage Release to Switch on Regulator

10.2.4 Other Schematics

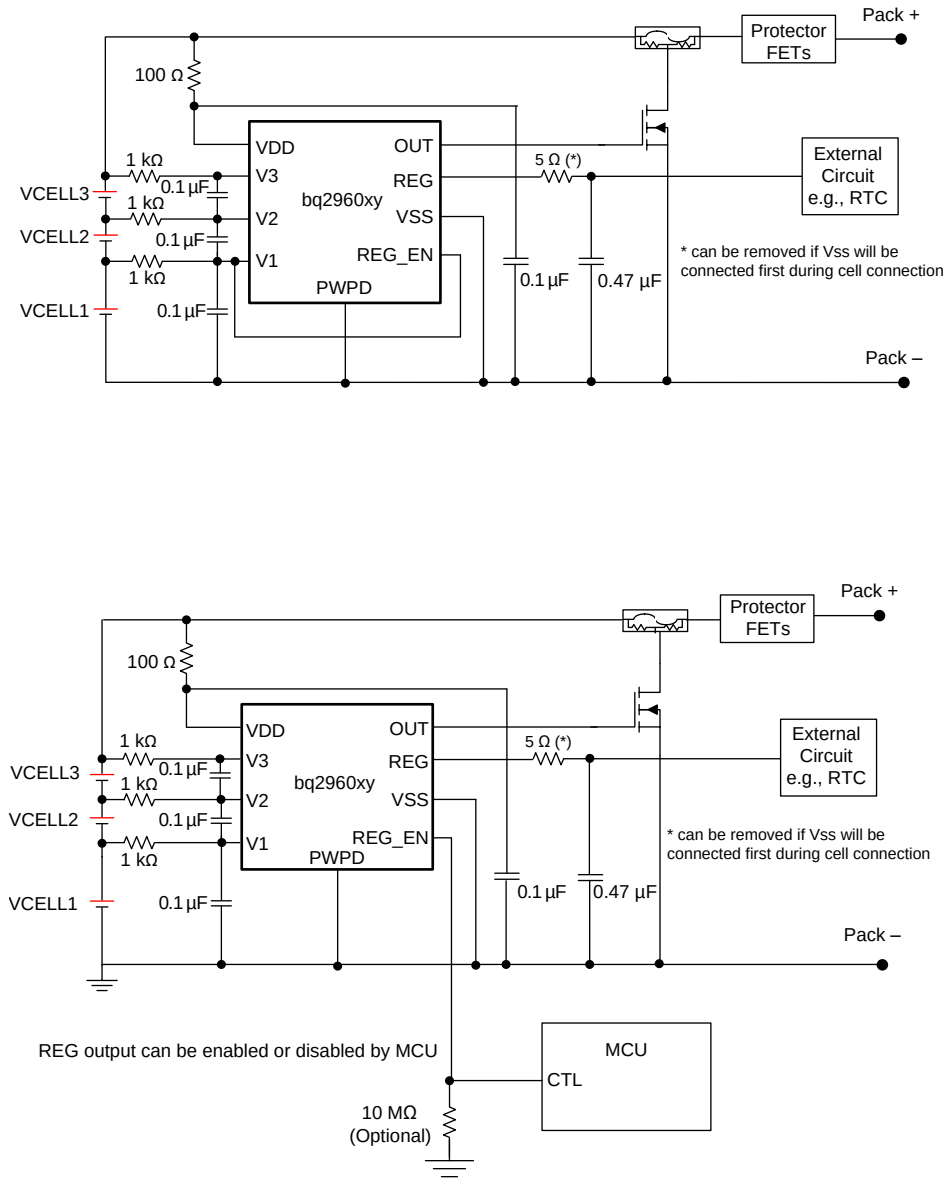


Figure 23. bq2960xy Schematic with REG Output Always Enabled

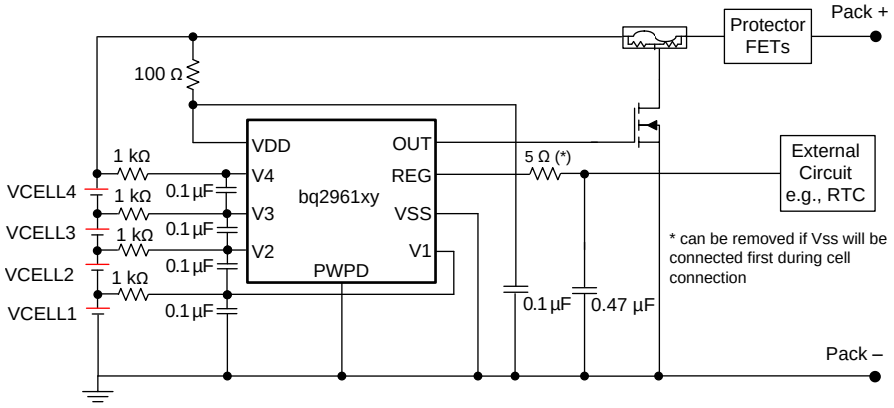


Figure 24. bq2961xy Schematic

11 Power Supply Recommendations

The maximum power is 15 V for bq2960xy and 20 V for bq2961xy on VDD.

NOTE

Connect VSS first during power up.

12 Layout

12.1 Layout Guidelines

Use the following layout guidelines.

1. Ensure the RC filters for the Vx pins and VDD pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for REG should be placed close to the device terminals.
3. Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack– is sufficient to withstand the current during a fuse blown event.

12.2 Layout Example

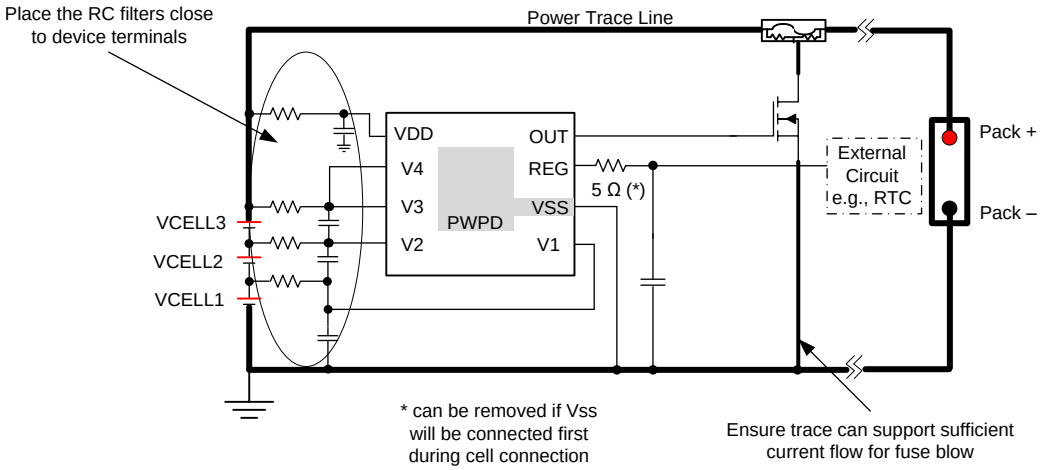


Figure 25. Layout Example

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296103DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	Samples
BQ296103DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	Samples
BQ296106DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	
BQ296106DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	
BQ296107DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	
BQ296107DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	
BQ296111DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	
BQ296111DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	
BQ296112DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	
BQ296112DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	
BQ296113DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	
BQ296113DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

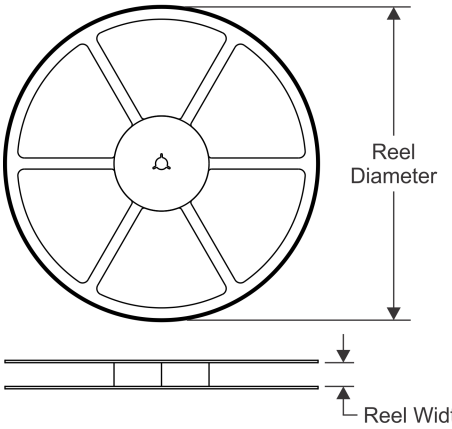
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

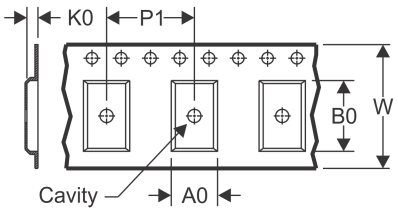
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

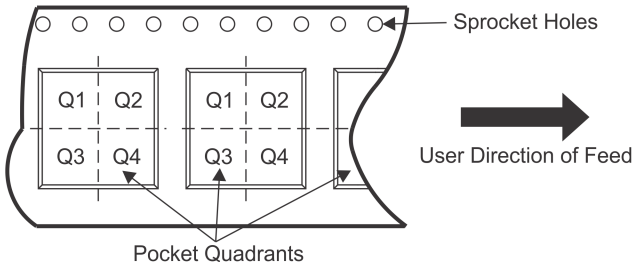


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

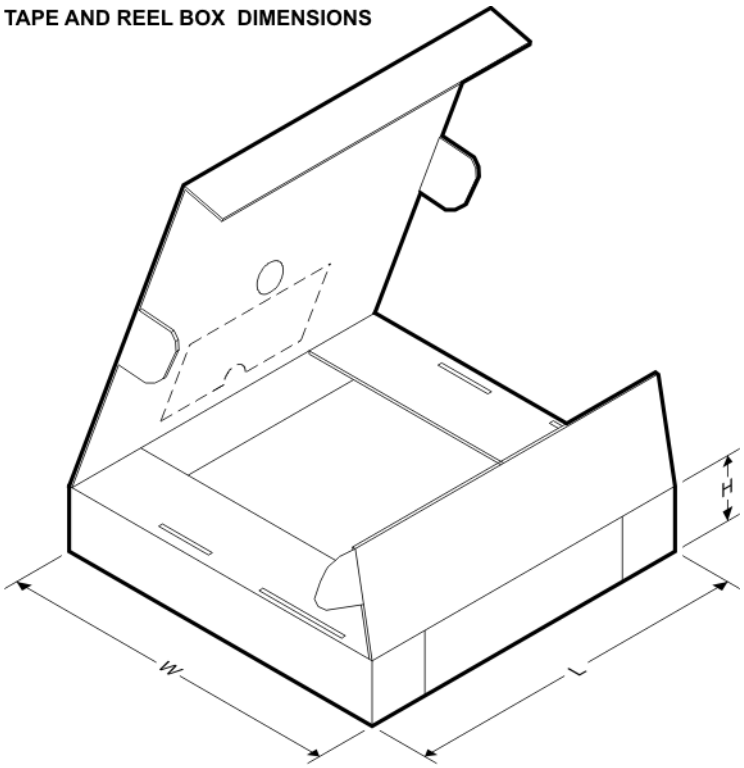
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296103DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

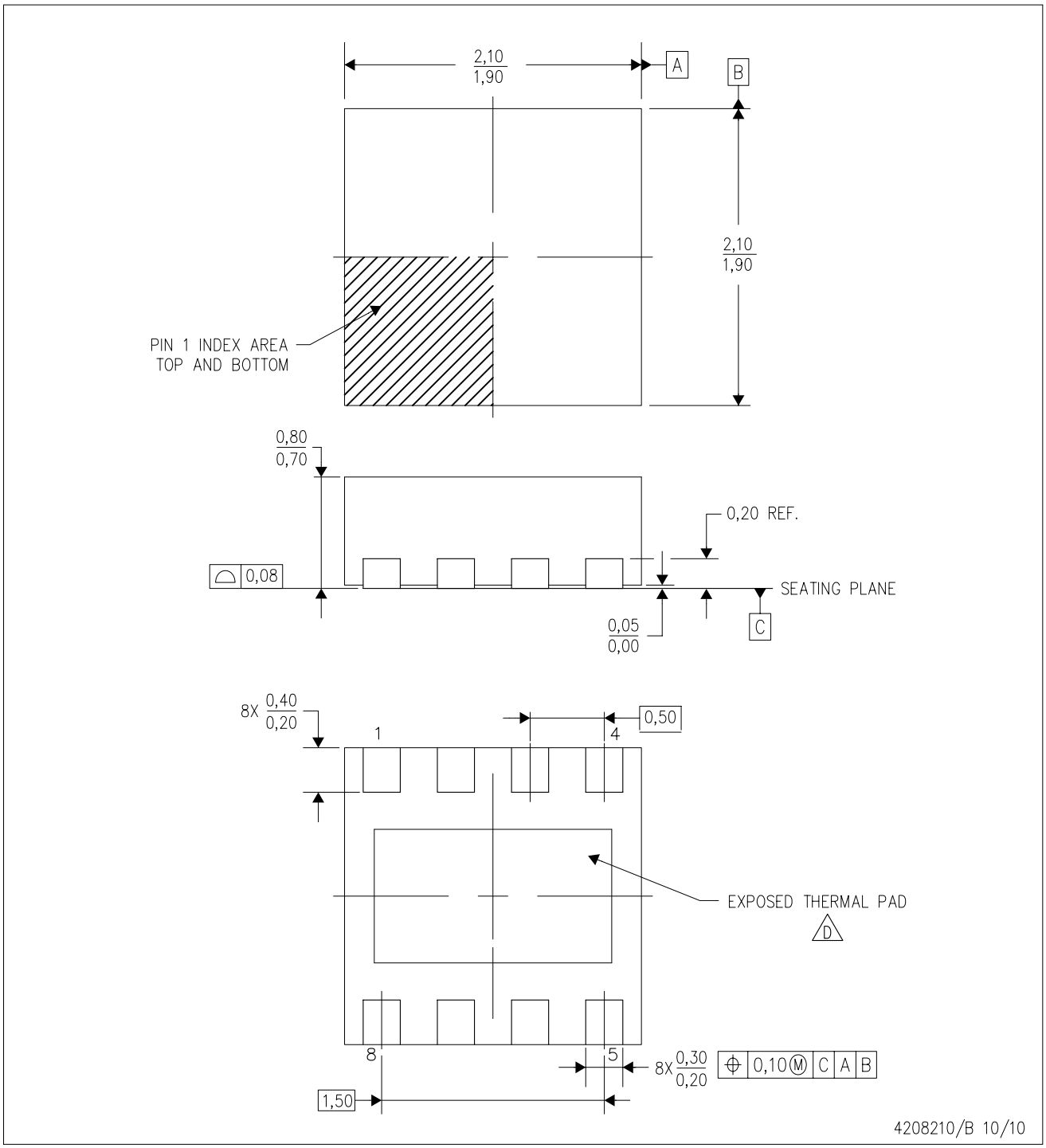
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296103DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296103DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296107DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

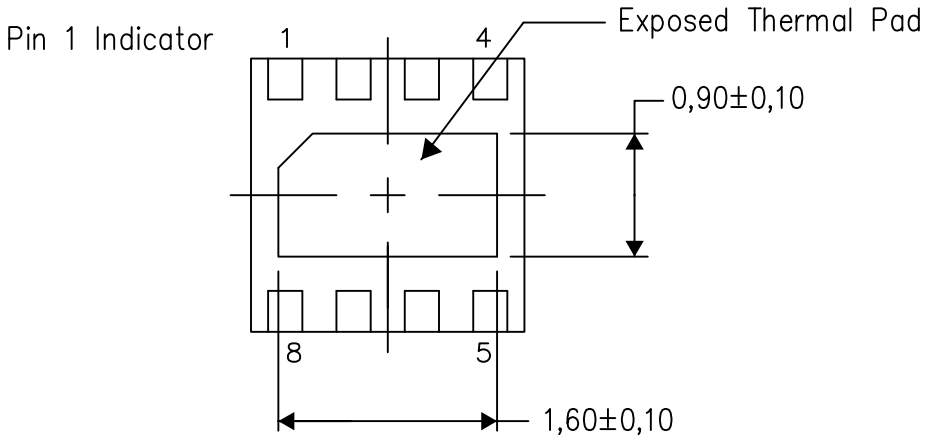
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



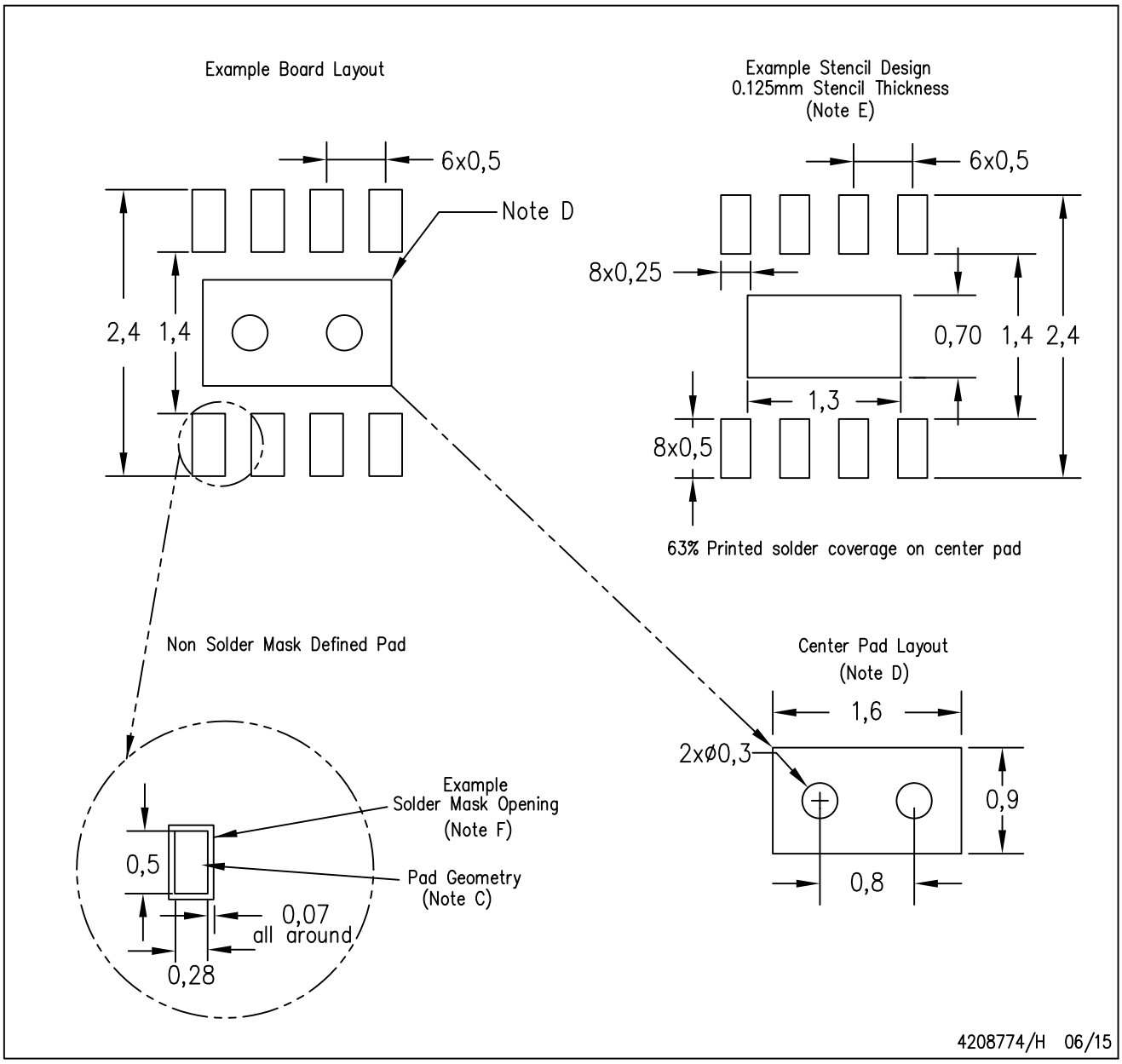
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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